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ECL Products	

100114

Quint Differential Line Driver

FEATURES

•Typical supply current ($-I_{EE}$): 73mA

DESCRIPTION

The 100114 contains five receivers with differential inputs (D_n, $\overline{D}_n$) and complementary outputs (Q_n, $\overline{Q}_n$). The inputs allow each receiver to be used in an inverting, non–inverting, or differential fashion. An internal reference voltage generator provides V_{BB} for single–ended operation. An external supply can also be used as the reference voltage. When used in the differential mode, common mode rejection makes this device tolerant of ground offsets and transients between signal source and the receiver.

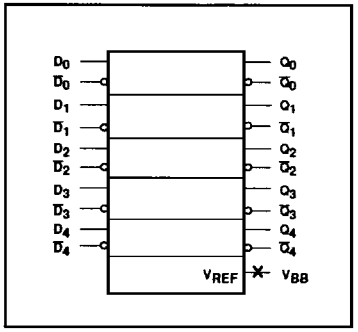
If both receiver inputs are left open or tied to the same voltage, the true output Q_n will be at a low logic level, and the complementary output $\overline{Q}_n$ will be high.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_4$,	True data Inputs
$\overline{D}_0 - \overline{D}_4$,	Complementary data inputs
$Q_0 - Q_4$	True data outputs
$\overline{Q}_0 - \overline{Q}_4$	Complementary data outputs
V_{BB}	Reference voltage output

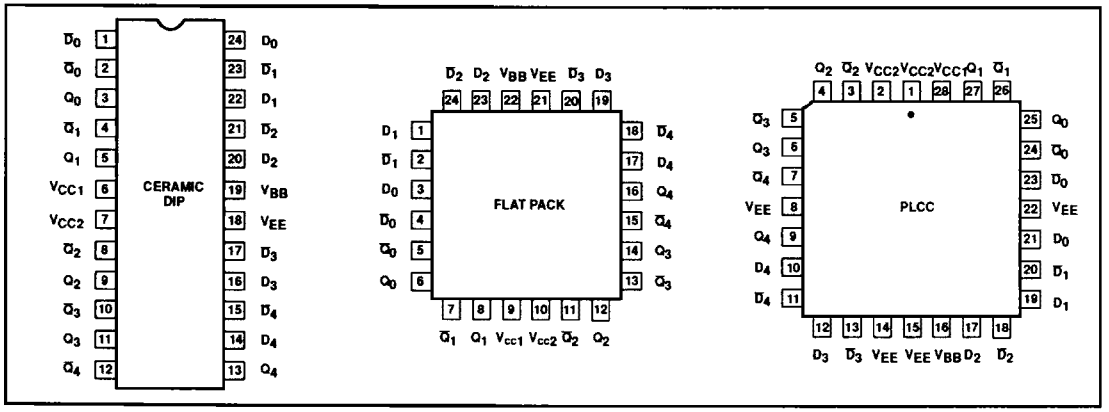
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100114F
24–Pin Ceramic Flat Pack	100114Y
28–Pin PLCC	100114A

PIN CONFIGURATIONS



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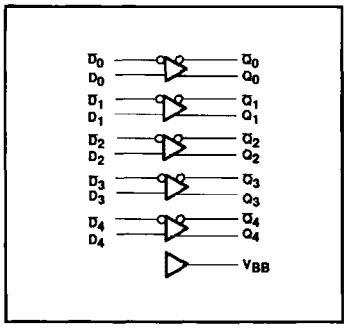
LOGIC DIAGRAM

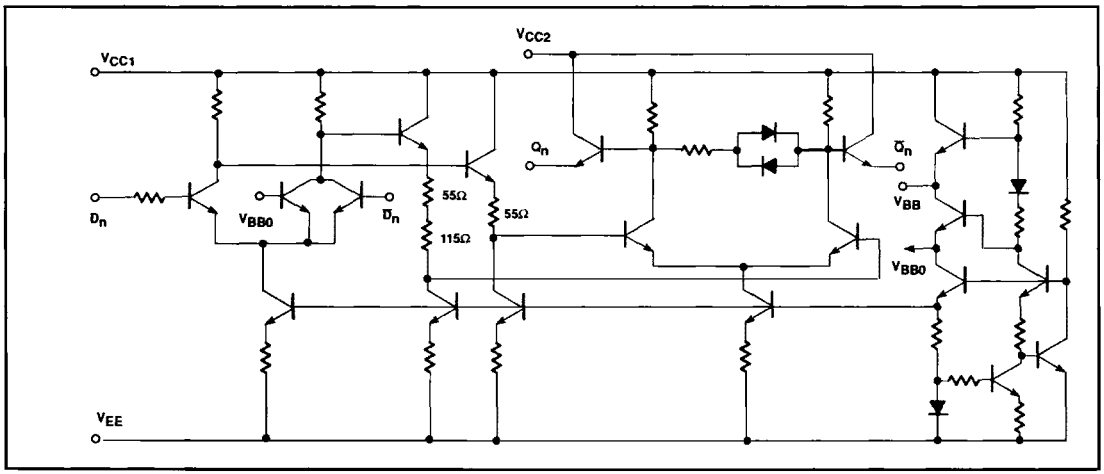


FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS	
D_n	$\overline{D}_n$	Q_n	$\overline{Q}_n$
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$V_{ID} \geq 0V$		L	H
$V_{ID} \leq -V_{DIFFMIN}$		H	L
$-V_{DIFFMIN} < V_{ID} < 0V$		*	*
open	open	L	H
V_{CC}	V_{CC}	L	H
V_{EE}	V_{EE}	L	H

NOTES:
H = High voltage level
L = Low voltage level
* = Indeterminate state
V_{BB} = Threshold level provided by reference voltage output of 100114.
V_{ID} = The voltage at $\overline{D}_n$ minus the voltage at D_n

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}[2]	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}[2]	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
V_{CM}[3]	Common mode voltage	V_{EE} = –4.2V				
		V_{EE} = –4.5V	0		1.0	V
		V_{EE} = –4.8V				
V_{DIFF}[4]	Differential input voltage	V_{EE} = –4.2V				
		V_{EE} = –4.5V	150			V
		V_{EE} = –4.8V				
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTES:
1. When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.
2. For input voltages outside the specified V_{IH} and V_{IL} ranges, the output voltage specifications will hold true. However, the AC performance will be according to specification only if two conditions are met: First, either D_n or $\overline{D}_n$ must be above –2300mV at all times. Second, both D_n and $\overline{D}_n$ must be below –230mV.
3. V_{CM} is added or subtracted with respect to V_{BB}. For common–mode applications, the total voltage applied to D_n or $\overline{D}_n$ should be no less than V_{BB}–V_{CM} (max) and no greater than V_{BB} + V_{CM} (max).
4. V_{DIFF} (min) is the minimum voltage difference by which D_n must exceed $\overline{D}_n$ such that output Q_n will assume a high logic level. See Function Table.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
V_{BB}	Reference output voltage	All D_n open, all $\overline{D}_n$ connected to V_{BB} pin.		V_{EE} = –4.5V	–1380	–1320	–1260	mV
				V_{EE} = –4.8V to –4.2V	–1396	–1320	–1244	mV
I_{IH}	High level input current	One D_n input under test at V_{IHMAX}. All other D_n inputs at V_{ILMIN}. All $\overline{D}_n$ inputs at V_{BB}.					65	µA
$-I_{CBO}$	Input leakage current	One D_n input under test at V_{EE}. All other D_n inputs at V_{ILMIN}. All $\overline{D}_n$ inputs at V_{BB}.					10	µA
$-I_{EE}$	V_{EE} supply current	Inputs open			51	73	106	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.20 2.20	0.60 0.60	2.20 2.20	0.70 0.70	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.20 2.20	0.60 0.60	2.20 2.20	0.70 0.70	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.00 2.00	0.60 0.60	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.00 2.00	0.60 0.60	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

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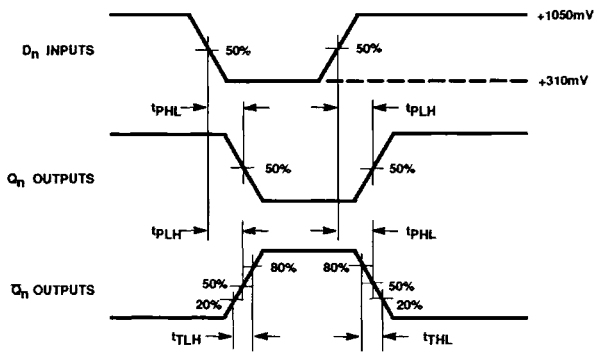
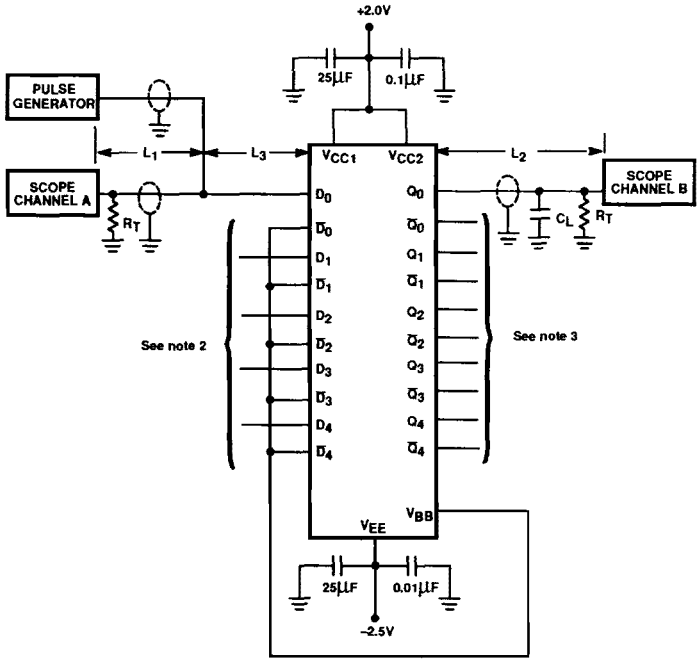
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
1. All power and signal voltages shifted up 2.0V for AC bench test purposes.
2. AC measurements are for single-ended operation of the device ($\overline{D}_n = V_{BB}$)

AC TEST CIRCUIT



NOTES:
1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a 2 High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.