



T-45-19-13

SP8716/8/9A

520MHz ULTRA LOW CURRENT TWO MODULUS DIVIDERS

The SP8716A ÷ 40/41, SP8718A ÷ 64/65 and SP8719A ÷ 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -55°C to +125°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the maximum loop delay.

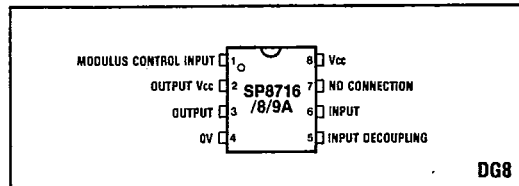


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -55°C to +125°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATING

Supply voltage (pin 2 or 8):	8V
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

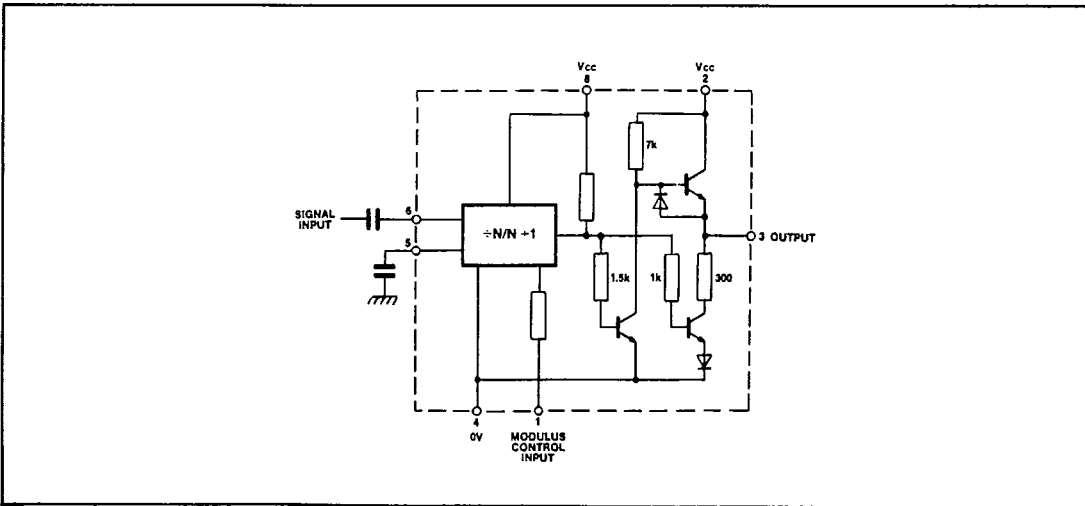


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: $V_{CC} = +4.95$ to $5.45V$, Temperature: $T_{amb} = -55^{\circ}C$ to $+125^{\circ}C$

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 125-350mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	$C_L = 3pF$; pins 2, 8 linked	1
Output high voltage	V_{OH}	($V_{CC} - 1.2$)	1.2	V	$I_L = -0.2mA$	1
Output low voltage	V_{OL}		1	V	$I_L = 0.2mA$	1
Control input high voltage	V_{INH}	3.3	8	V	$\neq N$	1
Control input low voltage	V_{INL}	0	1.7	V	$+N + 1$	1
Control input high current	I_{INH}		0.41	mA	$V_{INH} = 8V$	1
Control input low current	I_{INL}	-0.20		mA	$V_{INL} = 0V$	1
Clock to output delay	t_p		28	ns	$C_L = 10pF$	2
Set-up time	t_s	10		ns	$C_L = 10pF$	2
Release time	t_r	10		ns	$C_L = 10pF$	2

NOTES

1. Tested at $25^{\circ}C$ only.
2. Guaranteed but not tested.

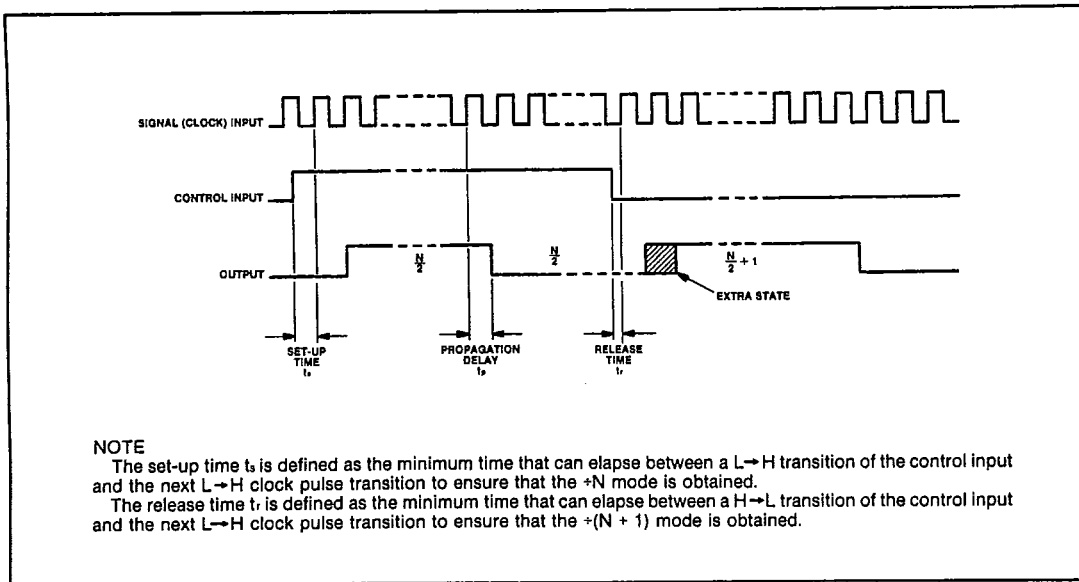
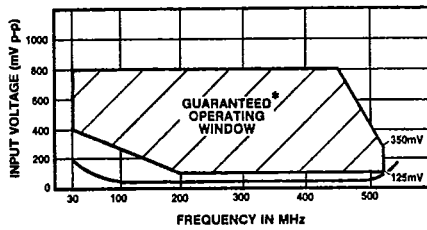


Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than $100V/\mu s$.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

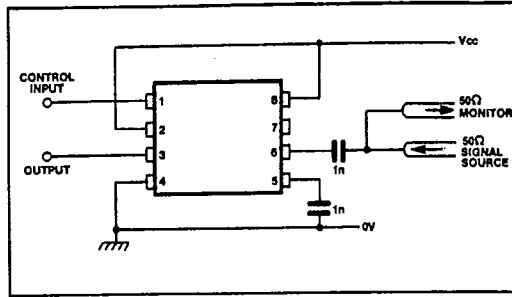


Fig.5 Toggle frequency test circuit

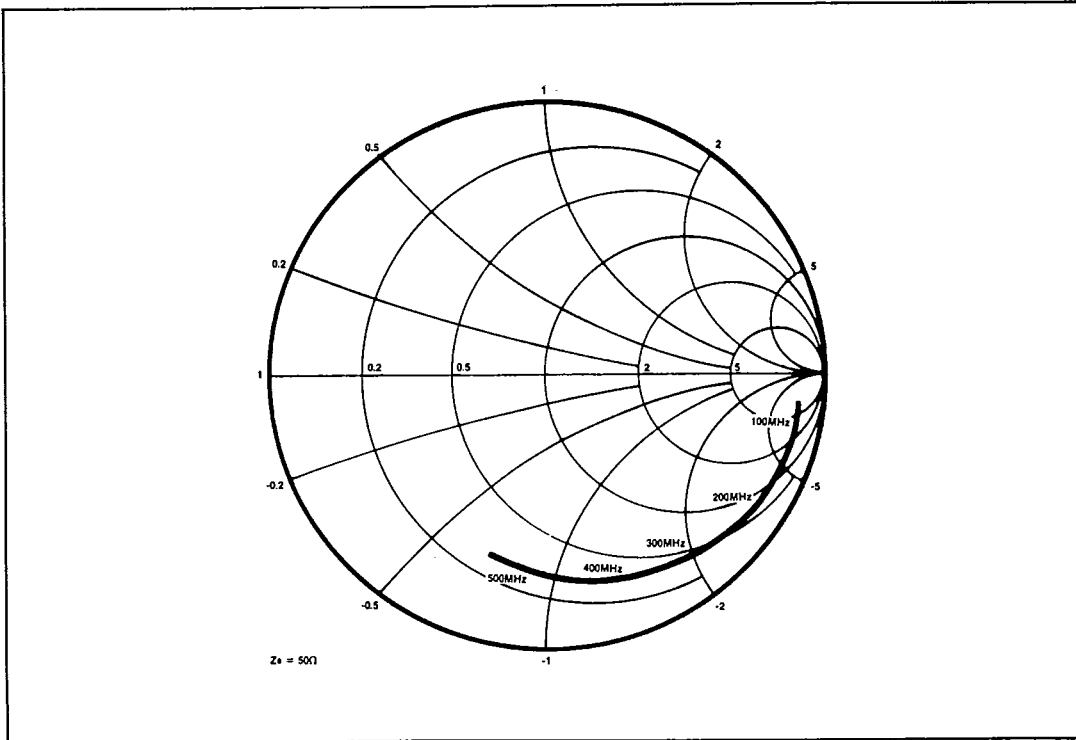


Fig.6 Typical input impedance