Intel® IXF1110 10-Port Gigabit Ethernet Media Access Controller

Datasheet

The Intel® IXF1110 is a 10-port Ethernet Media Access Controller (MAC) that supports IEEE 802.3 1000 Mbps applications. The device supports a System Packet Interface Level 4 Phase 2 (SPI4-2) system interface to the network processor or ASIC, and implements an internal Serializer/Deserializer (SerDes) to allow direct connection to optical modules. The integration of the SerDes functionality reduces PCB real-estate and system-cost requirements.

Applications

In general, the IXF1110 is appropriate for high-end switching applications where MAC and SerDes functions are not integrated into the system ASIC.

- High-End Optical Ethernet Switches
- Multi-Service Optical Ethernet Switches
- High-End Ethernet LAN/WAN Routers

Product Features

- SerDes interface with optical module connections for Ethernet physical connectivity
  - —Integrated termination
  - —I^2C Read/Write capability
- System Packet Interface Level 4 Phase 2 (SPI4-2)
  - —Capable of data transfers from 10.24 Gbps up to 12.8 Gbps
  - —Supports dynamic phase alignment
  - —Integrated termination
- Ten independent 1000 Mbps full-duplex Ethernet MAC ports
- 32-bit CPU interface
- Operating Temperature Range:

MIN	MAX
0 °C	+70 °C

- RMON statistics
- JTAG boundary scan
- Compliant with IEEE 802.3x Standard for flow control
- Jumbo frame support for 9.6 KB packets
- .18 µ CMOS process technology
- Supports IEEE 802.3 fiber auto-negotiation, including forced mode
- SFP MSA compatible
- Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per port
- Independent enable/disable of any port
- Detection of overly large packets
- Error counters for dropped and errored packets
- CRC calculation and error detection
- Programmable options:
  - —Filter packets with errors
  - —Filter, broadcast, multicast, and unicast address packets
  - —Automatically pad transmitted packets less than the minimum frame size
- 552-Ceramic Ball Grid Array (CBGA)
- 1.8 V and 2.5 V operation
- Power consumption: 490 mW per-port typical
- Product Ordering Number (MM): HFIXF1110CC.B2: 860817

Document Number: 250210
Revision Number: 008
Revision Date: August 10, 2004

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked “reserved” or “undefined.” Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® IXF1110 MAC may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

AnyPoint, AppChoice, BoardWatch, BunnyPeople, CablePort, Celeron, Chips, CT Media, Dialogic, DM3, EtherExpress, ETOX, FlashFile, i386, i486, i960, iCOMP, InstantIP, Intel, Intel Centrino, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel Create & Share, Intel GigaBlade, Intel InBusiness, Intel Inside, Intel Inside logo, Intel NetBurst, Intel NetMerge, Intel NetStructure, Intel Play, Intel Play logo, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel TeamStation, Intel Xeon, Intel XScale, IPLink, Itanium, MCS, MMX, MMX logo, Optimizer logo, OverDrive, Paragon, PC Dads, PC Parents, PDCharm, Pentium, Pentium II Xeon, Pentium III Xeon, Performance at Your Command, RemoteExpress, SmartDie, Solutions960, Sound Mark, StorageExpress, The Computer Inside., The Journey Inside, TokenExpress, VoiceBrick, VTune, and Xircom are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2004, Intel Corporation

Contents

1.0 Introduction 13
1.1 What You Will Find in This Document 13
1.2 Related Documents 14
2.0 General Description 15
3.0 Ball Assignments and Ball List Tables 17
3.1 Ball List Tables 18
3.1.1 Balls Listed in Alphanumeric Order by Signal Name 18
3.1.2 Balls Listed in Alphanumeric Order by Ball Location 24
4.0 Ball Assignments and Signal Descriptions 30
4.1 Naming Conventions 30
4.1.1 Signal Name Conventions 30
4.1.2 Register Address Conventions 30
4.2 Interface Signal Groups 31
5.0 Functional Descriptions 43
5.1 Media Access Controller 43
5.1.1 General Description 43
5.1.2 MAC Functions 43
5.1.2.1 Padding of Undersized Frames on Transmit 43
5.1.2.2 Automatic CRC Generation 44
5.1.2.3 Filtering of Receive Packets 44
5.1.3 Flow Control 46
5.1.3.1 802.3x Flow Control (Full-Duplex Operation) 46
5.1.4 Fiber Operation 50
5.1.5 Auto-Negotiation 51
5.1.5.1 Determining If Link Is Established in Auto-Negotiation Mode 51
5.1.6 Forced Mode Operation 52
5.1.6.1 Determining If Link Is Established in Forced Mode 52
5.1.7 Jumbo Packet Support 52
5.1.8 RMON Statistics Support 53
5.1.8.1 RMON Statistics 53
5.1.8.2 Conventions 55
5.1.8.3 Additional Statistics 55
5.2 System Packet Interface Level 4 Phase 2 57
5.2.1 Data Path 58
5.2.1.1 Control Words 59
5.2.1.2 EOP Abort 61
5.2.1.3 DIP4 62
5.2.2 Start-Up Parameters 63
5.2.2.1 CALENDAR_LEN 63
5.2.2.2 CALENDAR_M 64
5.2.2.3 DIP2_Thr 64
5.2.2.4 Loss_Of_Sync 64
5.2.2.5 DATA_MAX_T 64
5.2.2.6 REP_T 64

Document Number: 250210
Revision Number: 008
Revision Date: August 10, 2004

5.2.2.7 DIP4_UnLock 64
5.2.2.8 DIP4_Lock 64
5.2.2.9 MaxBurst1 65
5.2.2.10MaxBurst2 65
5.2.3 Dynamic Phase Alignment Training Sequence (Data Path De-skew) 65
5.2.3.1 Training at Start-up 65
5.2.3.2 Periodic Training 65
5.2.3.3 Training in a Practical Implementation 66
5.2.4 FIFO Status Channel 66
5.2.5 DC Parameters 70
5.3 SerDes Interface 70
5.3.1 Introduction 70
5.3.2 Features 70
5.3.3 Functional Description 71
5.3.3.1 Transmitter Operational Overview 71
5.3.3.2 Transmitter Programmable Driver-Power Levels 71
5.3.3.3 Receiver Operational Overview 72
5.3.3.4 Selective Power-Down 72
5.3.4 Timing and Electrical Characteristics 72
5.4 Optical Module Interface 72
5.4.1 Introduction 72
5.4.2 IXF1110 Supported Optical Module Interface Signals. 72
5.4.3 Functional Descriptions 73
5.4.3.1 High-Speed Serial Interface 73
5.4.3.2 Low-Speed Status Signaling Interface 73
5.4.4 I^2C Module Configuration Interface 75
5.4.4.1 General Description 76
5.4.4.2 I^2C Protocol Specifics 78
5.4.4.3 Port Protocol Operation 78
5.4.4.4 Clock and Data Transitions 78
5.4.4.5 AC Timing Characteristics 82
5.5 LED Interface 82
5.5.1 Introduction 82
5.5.2 Modes of Operation 82
5.5.2.1 Mode 0 83
5.5.2.2 Mode 1 83
5.5.3 LED Interface Signal Description 83
5.5.4 Mode 0: Detailed Operation 83
5.5.5 Mode 1: Detailed Operation 84
5.5.6 Power-On, Reset, and Initialization 85
5.5.6.1 Enabling the LED Interface 85
5.5.7 LED Data Decodes 86
5.5.7.1 LED Signaling Behavior 86
5.6 CPU Interface 87
5.6.1 General Description 87
5.6.2 Functional Description 88
5.6.2.1 Read Access 89
5.6.2.2 Write Access 90
5.6.2.3 Timing parameters 91
5.6.3 Endian 91
5.7 JTAG (Boundary Scan) 91

5.7.1 TAP Interface (JTAG) 91
5.7.2 TAP State Machine 92
5.7.3 Instruction Register and Supported Instructions 92
5.7.4 ID Register 92
5.7.5 Boundary Scan Register 93
5.7.6 Bypass Register 93
5.8 Clocks 93
5.8.1 System Interface Reference Clocks 93
5.8.1.1 CLK125 93
5.8.1.2 CLK50 93
5.8.2 SPI4-2 Receive and Transmit Data Path Clocks 94
5.8.3 JTAG Clock 94
5.8.4 I^2C Clock 94
5.8.5 LED Clock 94

6.0 Applications 95

6.1 Power Supply Sequencing 95
6.1.1 Power-Up Sequence 95
6.1.2 Power-Down Sequence 95
6.2 Analog Power Filtering 96
6.3 TX FIFO and RX FIFO Operation 96
6.3.1 TX FIFO 97
6.3.1.1 MAC Transfer Threshold 97
6.3.1.2 TXFIFO relation to SPI4-2 Transmit FIFO Status (TSTAT) 98
6.3.1.3 TX FIFO Drain (IXF1110 Version) 98
6.3.2 RX FIFO 99
6.4 Reset and Initialization 100
6.4.1 SPI4-2 Initialization 100
6.4.1.1 RX SPI4-2 100
6.4.1.2 TX SPI4-2 101
6.4.1.3 SerDes 101
6.4.1.4 CPU 101
6.5 SerDes Power-Down Capabilities 101
6.5.1 Placing the SerDes Port in Power-Down Mode 101
6.5.2 Bringing the SerDes Port Out of Power-Down Mode 102
6.6 IXF1110 Unused Ports 102
6.7 Optical Module Connections to the IXF1110 102
6.7.1 SFP-to-IXF1110 Connection 102

7.0 Electrical Specifications 105

7.1 DC Specifications 107
7.2 Undershoot/Overshoot Specifications 108
7.3 CPU Timing Specification 109
7.4 JTAG Timing Specification 111
7.5 Transmit Pause Control Timing Specifications 112
7.6 Optical Module Interrupt and I^2C Timing Specification 113
7.7 System Timing Specifications 116
7.8 LED Timing Specifications 117
7.9 SerDes Timing Specification 118
7.10 SPI4-2 Timing Specifications 120

8.0 Register Definitions 122
8.1 Introduction 122
8.2 Document Structure 122
8.3 Graphical Representation 122
8.4 Per Port Registers 124
8.5 Memory Map 124
8.5.1 MAC Control Registers 132
8.5.2 MAC RX Statistics Register Overview 140
8.5.3 MAC TX Statistics Register Overview 144
8.5.4 Global Status and Configuration Register Overview 148
8.5.5 Global RX Block Register Overview 153
8.5.6 TX Block Register Overview 162
8.5.7 SPI4-2 Block Register Overview 172
8.5.8 SerDes Register Overview 174
8.5.9 Optical Module Interface Block Register Overview 176
9.0 Package Overview 178
9.1 Features 178
9.2 IXF1110 Package Specifics 178
9.2.1 Markings 179
10.0 Product Ordering Information 182

Figures

1 Intel® IXF1110 MAC Block Diagram 15
2 Intel® IXF1110 MAC System Block Diagram 16
3 552-Ball CBGA Assignments (Top View) 17
4 Interface Diagram 31
5 Packet Buffering FIFO 47
6 Ethernet Frame Format 47
7 PAUSE Frame Format 48
8 Transmit Pause Control Interface 50
9 SPI4-2 Interfacing with the Network Processor or Forwarding Engine 57
10 Data Path State 59
11 Per-Port State Diagram with Transitions at Control Words 61
12 DIP-4 Calculation Boundaries 62
13 DIP-4 Calculation Algorithm 63
14 FIFO Status State Diagram 67
15 Example of DIP-2 Encoding 68
16 Data Validity Timing 79
17 Start and Stop Definition Timing 79
18 Acknowledge Timing 80
19 Random Read 81
20 Byte Write 82
21 Mode 0 Timing 84
22 Mode 1 Timing 85
23 CPU Interface Inputs/Outputs 88
24 Read Timing – Asynchronous Interface 90
25 Write Timing – Asynchronous Interface 90
26 Power Sequencing 95

27 Analog Power Supply Filter Network 96
28 Packet Buffering FIFO 97
29 SFP-to-IXF1110 Connection 103
30 CPU Port Read Timing 109
31 CPU Port Write Timing 109
32 JTAG Timing 111
33 Transmit Pause Control Interface 112
34 Optical Module Interrupt Timing 113
35 I^2C Bus Timing 114
36 I^2C Write Cycle 114
37 Hardware Reset Timing 116
38 LED Timing 117
39 SerDes Timing 118
40 SPI4-2 Transmit FIFO Status Bus Timing 120
41 SPI4-2 Receive FIFO Status Bus Timing 121
42 Memory Overview 123
43 Register Overview 124
44 Intel® IXF1110 MAC 552-Ceramic Ball Grid Array (CBGA) Package Specifications 180
45 Intel®IXF1110 MAC CBGA Package Side View Diagram 181
46 Intel® IXF1110 MAC Ordering Information - Sample 182

Tables

1 Ball List in Alphanumeric Order by Signal Name 18
2 Ball List in Alphanumeric Order by Ball Location 24
3 SPI4-2 Interface Signal Descriptions 32
4 SerDes Interface Signal Descriptions 34
5 CPU Interface Signal Descriptions 35
6 Pause Control Interface Signal Descriptions 36
7 Optical Module Interface Signal Descriptions 37
8 LED Interface Signal Descriptions 38
9 JTAG Interface Signal Descriptions 39
10 System Interface Signal Descriptions 39
11 Power Supply Signal Descriptions 40
12 Unused Balls/Reserved 42
13 Pause Packets Drop Enable Behavior 45
14 CRC Errored Packets Drop Enable Behavior 46
15 Valid Decodes for TXPAUSEADD[3:0] 49
16 RMON Additional Statistics Registers 54
17 SPI4-2 Interface Signal Summary 57
18 Control Word Format 60
19 Control Word Definitions 60
20 FIFO Status Format 69
21 SerDes Driver TX Power Levels 71
22 IXF1110-to-SFP Connections 73
23 LED Signal Descriptions 83
24 Mode 0 Clock Cycle to Data Bit Relationship 84
25 Mode 1 Clock Cycle to Data Bit Relationship 85
26 LED Data Decodes 86
27 LED Behavior 87

28 CPU Interface Signals 88
29 Recommended JTAG Termination 91
30 Supported Boundary Scan Instructions 92
31 Power Sequencing 96
32 Analog Power Balls 96
33 SFP-to-IXF1110 Connection 103
34 Absolute Maximum Ratings 105
35 Operating Conditions 106
36 2.5 V LVTTL and CMOS I/O Electrical Characteristics 107
37 LVDS I/O Electrical Characteristics 107
38 Undershoot/Overshoot Limits 108
39 CPU Timing Parameters 109
40 JTAG Timing Parameters 111
41 Transmit Pause Control Interface Parameters 112
42 Optical Module Interrupt Timing Parameters 113
43 I^2C AC Timing Characteristics 114
44 Hardware Reset Timing Parameters 116
45 LED Timing Parameters 117
46 Transmitter Characteristics 118
47 Receiver Characteristics 119
48 SPI4-2 Transmit FIFO Status Bus Timing Parameters 120
49 SPI4-2 Receive FIFO Status Bus Timing Parameters 121
50 SPI4-2 LVDS Rise/Fall Times 121
51 MAC Control Register Map 124
52 MAC RX Statistics Register Map 125
53 MAC TX Statistics Register Map 126
54 Global Status and Configuration Register Map 127
55 RX Block Register Map 128
56 TX Block Register Map 129
57 SPI4-2 Block Register Map 130
58 SerDes Block Register Map 130
59 Optical Module Interface Block Register Map 131
60 Station Address Low ($ Port_Index + 0x00) 132
61 Station Address High ($ Port_Index + 0x01) 132
62 FDFC Type ($ Port_Index + 0x03) 132
63 FC TX Timer Value ($ Port_Index + 0x07) 132
64 FDFC Address Low ($ Port_Index + 0x08) 133
65 FDFC Address High ($ Port_Index + 0x09) 133
66 IPG Transmit Time ($ Port_Index + 0x0C) 133
67 Pause Threshold ($ Port_Index + 0x0E) 134
68 Max Frame Size ($ Port_Index + 0x0F) 134
69 FC Enable ($ Port_Index + 0x12) 135
70 Discard Unknown Control Frame ($ Port_Index + 0x15) 135
71 RX Config Word ($ Port_Index + 0x16) 135
72 TX Config Word ($ Port_Index + 0x17) 136
73 Diverse Config ($ Port_Index + 0x18) 137
74 RX Packet Filter Control ($ Port_Index + 0x19) 138
75 Port Multicast Address Low ($ Port_Index + 0x1A) 139
76 Port Multicast Address High ($ Port_Index + 0x1B) 139
77 MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) 140

78 MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) 144
79 Port Enable ($ 0x500) 148
80 Link LED Enable ($ 0x502) 149
81 Core Clock Soft Reset ($ 0x504) 149
82 MAC Soft Reset ($ 0x505) 150
83 CPU Interface ($ 0x508) 150
84 LED Control ($ 0x509) 151
85 LED Flash Rate ($ 0x50A) 151
86 LED Fault Disable ($ 0x50B) 151
87 JTAG ID Revision ($ 0x50C) 152
88 RX FIFO High Watermark Ports 0 to 9 ($ 0x580 - 0x589) 153
89 RX FIFO Low Watermark Ports 0 to 9 ($ 0x58A - 0x593) 154
90 RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D) 156
91 RX FIFO Port Reset ($ 0x59E) 158
92 RX FIFO Errored Frame Drop Enable ($ 0x59F) 159
93 RX FIFO Overflow Event ($ 0x5A0) 160
94 TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609) 162
95 TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613) 163
96 TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) 165
97 TX FIFO Overflow Event ($ 0x61E) 167
98 TX FIFO Drain ($0x620) 168
99 TX FIFO Info Out-of-Sequence ($ 0x621) 169
100 TX FIFO Number of Frames Removed Ports 0-9 ($ 0x622 - 0x62B) 170
101 SPI4-2 RX Burst Size ($ 0x700) 172
102 SPI4-2 RX Training ($ 0x701) 172
103 SPI4-2 RX Calendar ($ 0x702) 173
104 SPI4-2 TX Synchronization ($ 0x703) 174
105 SerDes Tx Driver Power Level Ports 0-6 ($ 0x784) 174
106 SerDes Tx Driver Power Level Ports 7-9 ($ 0x785) 175
107 SerDes TX and RX Power-Down Ports 0-9 ($ 0x787) 175
108 Optical Module Status Ports 0-9 ($ 0x799) 176
109 Optical Module Control Ports 0-9 ($ 0x79A) 176
110 I^2C Control Ports 0-9 ($ 0x79B) 176
111 I^2C Data Ports 0-9 ($ 0x79C) 177
112 Intel® IXF1110 MAC Product Information 182

Revision History

Revision Number: 008 Revision Date: August 10, 2004	
Page #	**Description**
All	Globally replaced the following: “AVDD” to “AVDD1P8_1, AVDD1P8_2” and “AVDD2” to “AVDD2P5_1, AVDD2P5_2”.
All	Globally replaced the following: “AIDD” to “AIDD1P8_1, AIDD1P8_2” and “AIDD2” to “AIDD2P5_1, AIDD2P5_2”.
32	Corrected ball number for RDAT15_P from K1 to K12 in Table 3 “SPI4-2 Interface Signal Descriptions”.
124	Removed Short Runts Threshold Register ($ Port_Index 0x14) and changed to Reserved in “Table 51 “MAC Control Register Map”.

Revision Number: 007 Revision Date: May 5, 2004	
Page #	**Description**
1	Changed product ordering number to reflect B2 [HFIXF1110CC.B2: 860817].
41	Modified Table 11 “Power Supply Signal Descriptions” [changed AVDD to AVDD1P8_1/2 and AVDD2 to AVDD2P5_1/2].
42	Added note under Section 5.1.2.1, “Padding of Undersized Frames on Transmit”.
42	Modified Section 5.1.2.3.1, “Filter on Unicast Packet Match” [added text to end of paragraph].
45	Added Section 5.1.3, “Flow Control”.
66	Modified third and fourth paragraphs of Section 5.2.2.2, “CALENDAR_M”.
97	Added Section 6.2, “Analog Power Filtering” (IXF1110 only)
116	Modified Section 6.3.1, “TX FIFO” [added note].
99	Added Section 6.3.1.3, “TX FIFO Drain (IXF1110 Version)”.
110	Added Table 48 “SPI4-2 LVDS Rise/Fall Times”.
126	Modified Table 72 “RX Packet Filter Control ($ Port_Index + 0x19)” (removed table note from the bit 4 description].
170	Modified Table 114 “SPI4-2 RX Calendar ($ 0x702)” [changed Register bits 3:0 to Reserved].
154	Modified Table 88 “JTAG ID Revision ($ 0x50C)” [added table note 2].
163	Added Table 105 “TX FIFO Drain ($0x620)”.
176	Modified Table 116 “Intel® IXF1010 MAC Product Information” [changed part number and MM number to reflect B2].

Revision Number: 006 Revision Date: December 30, 2003	
Page #	**Description**
NA	Deleted old Table 19: 1x9-to-IXF1110 Connection
136	Modified text under Section 6.5, “SerDes Power-Down Capabilities (IXF1110 Only)”.
NA	Changed Table 98: TX FIFO Port Reset Register (Addr: 0x620) to Reserved.

Revision Number: 005 (Sheet 1 of 2) Revision Date: November 24, 2003	
Page #	**Description**
1	Added product ordering and operating temperature range information, and changed SFF-8053, Revision 5.5 Compatible to SFP MSA compatible.
17	Deleted old Figures 6, 7, and 8 (Revision 004) and replaced with Figure 6 “Intel® IXF1110 552-Ball CBGA Assignments (Top View)”
18	Added new Section 3.1, “Intel® IXF1110 Ball List Tables” including Table 1 “Intel® IXF1110 Ball List in Alphanumeric Order by Signal Name” and Table 2 “Intel® IXF1110 Ball List in Alphanumeric Order by Ball Location”.
30	Modified Figure 4 “Intel® IXF1110 Interface Diagram”.
31	Broke up old Table 3 into Table 3 “Intel® IXF1110 SPI4-2 Interface Signal Descriptions” through Table 12 “Intel® IXF1110 System Interface Signal Descriptions”.
34	Modified Table 5 “Intel® IXF1110 CPU Interface Signal Descriptions”.
36	Modified Table 7 “Intel® IXF1110 Optical Module Interface Signal Descriptions”.
43	Added note under Section 5.1.2.3.5, “Filter PAUSE Packets”.
43	Added note under Section 5.1.2.3.6, “Filter CRC Errored Packets”.
44	Added third note to Section 5.1.3, “Fiber Operation”.
46	Modified text and added note under Section 5.1.4, “Fiber Auto-Negotiation”.
46	Modified Section 5.1.5, “Forced Mode Operation”
52	Modified Figure 6 “Intel® IXF1110 SPI4-2 Interfacing with the Network Processor or Forwarding Engine”.
52	Added Table 17 “Intel® IXF1110 SPI4-2 Interface Signal Summary”.
56	Added new Section 5.2.1.2, “EOP Abort”.
65	Globally modified SFF-8053, Revision 5.5 Compatible to SFP MSA compatible under Section 5.3, “SerDes Interface”.
66	Modified Section 5.3.3, “Functional Description”.
66	Added Section 5.5.4.1 “Transmitter Programmable Driver-Power Levels”.
67	Added Table 21 “Intel® IXF1110 SerDes Driver TX Power Levels”.
68	Changed Gigabit Interface Converter section to Section 5.6, “Optical Module Interface”. Globally changed GBIC to Optical Module.
69	Modified Section 5.4.3.2.1, “MOD_DEF_9:0”.
69	Modified Section 5.6.3.2.2, “TX_FAULT_9:0”.
70	Modified Section 5.6.3.2.3, “RX_LOS_9:0”.
86	Added note to “UPX_RDY” under Section 5.8.2, “Functional Description”.
95	Added note under Section 6.2.1, “TX FIFO”.
95	Added note under Section 6.2.1.1, “MAC Transfer Threshold”.
104	Modified/added Power Consumption Max to Table 49 “Intel® IXF1110 Operating Conditions”.
105	Modified Table 36 “Intel® IXF1110 2.5 V LVTTL and CMOS I/O Electrical Characteristics”.
105	Added Section 7.2, “Undershoot/Overshoot Specifications”.
107	Modified Table 39 “Intel® IXF1110 CPU Timing Parameters”.
115	Modified Table 46 “Intel® IXF1110 Transmitter Characteristics”.

Revision Number: 005 (Sheet 2 of 2) Revision Date: November 24, 2003	
Page #	**Description**
116	Modified Table 47 “Intel® IXF1110 Receiver Characteristics” (added Common Mode Voltage Spec).
119	Added caution note under Section 8.0, “Register Definitions”.
124	Modified Table 53 “Intel® IXFIXF1110 Global Status and Configuration Register Map”.
130	Modified Table 65 “IPG Transmit Time Register (Addr: Port_Index + 0x0C)”.
131	Modified Table 66 “Pause Threshold Register (Addr: Port_Index + 0x0E)”.
132	Modified Table 68 “FC Enable Register (Addr: Port_Index + 0x12)”.
132	Modified Table 69 “Short Runts Threshold Register (Addr: Port_Index + 0x14)”.
132	Modified Table 71 “RX Config Word Register (Addr: Port_Index + 0x16)”.
133	Modified Table 72 “TX Config Word Register (Addr: Port_Index + 0x17)”.
134	Modified Table 73 “Diverse Config Register (Addr: Port_Index + 0x18)”.
135	Modified Table 74 “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” (removed note 2 from bit 4, modified bit 5 description).
137	Modified Table 77 “MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)”.
146	Added Table 81 “Core Clock Soft Reset Register (Addr: 0x504)”.
147	Added Table 82 “MAC Soft Reset Register (Addr: 0x505)”.
155	Added Table 91 “RX FIFO Port Reset Register (Addr: 0x59E)”.
165	Added Section 98, “TX FIFO Port Reset Register (Addr: 0x620)”.
167	Modified Table 100 “TX FIFO Number of Frames Removed Ports 0-9 (Addr: 0x622 - 0x62B)”.
170	Modified Table 103 “SPI4-2 RX Calendar Register (Addr: 0x702)”.
171	Modified Table 104 “SPI4-2 TX Synchronization Register (Addr: 0x703) (B0 Silicon Revision)”.
173	Added Table 106 “SerDes Tx Driver Power Level Ports 0-6 Register (Addr: 0x784)”.
173	Added Table 107 “SerDes Tx Driver Power Level Ports 7-9 Register (Addr: 0x785)”.

1.0 Introduction

This document describes the functionality and operation of the Intel® IXF1110 10-Port Gigabit Ethernet Media Access Controller.

1.1 What You Will Find in This Document

This document contains the following sections:

- Section 2.0, “General Description” on page 15
  Intel® IXF1110 MAC block diagram system architecture.
- Section 3.0, “Ball Assignments and Ball List Tables” on page 17
  Intel® IXF1110 MAC ball grid diagram with two ball list tables (by pin number and signal name)
- Section 4.0, “Ball Assignments and Signal Descriptions” on page 30
  Signal naming methodology and signal descriptions.
- Section 5.0, “Functional Descriptions” on page 43
  Detailed information about the operation of the Intel® IXF1110 MAC including general features, and interface types and descriptions.
- Section 6.0, “Applications” on page 95
  Discusses the following:
  - “Power Supply Sequencing”
  - “TX FIFO and RX FIFO Operation”
  - “Reset and Initialization”
  - “Optical Module Connections to the IXF1110”
- Section 7.0, “Electrical Specifications” on page 105
  Information on the product-operating parameters, electrical specifications, and timing parameters.
- Section 8.0, “Register Definitions” on page 122
  Memory map/detailed descriptions and default values for the register set.
- Section 9.0, “Package Overview” on page 178
  Intel® IXF1110 MAC packaging information.
- Section 10.0, “Product Ordering Information” on page 182
  Provides a table with part-number information and diagram to order the Intel® IXF1110 MAC.

1.2 Related Documents

Title	Document Number
Intel® IXF1110 MAC Specification Update	251436
Intel® IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Design and Layout Guide	250676
Intel® IXF1110 Demo Board Development Kit Manual	250807
Intel® SPI4 Phase 2 Performance in Gigabit Ethernet Media Access Controllers Application Note	250643
Interfacing with the Intel® IXF1010 and Intel® IXF1110 10-Port Gigabit Ethernet Media Access Controllers Application Note	250856
Intel® IXF1110 Thermal Design Considerations Application Note	250289
Flow Control in the Intel® IXF1010 and Intel® IXF1110 10-Port Gigabit Ethernet Media Access Controllers Application Note	250236

2.0 General Description

The Intel® IXF1110 is a 10-port 1000 Mbps Ethernet Media Access Controller (MAC). The 10 Gigabit interface to the network processor is supported through a System Packet Interface Level 4 Phase 2 (SPI4-2), and the media interface is an integrated Serializer/Deserializer (SerDes).

Figure 1 illustrates the IXF1110 block diagram.Figure 2 represents the IXF1110 system block diagram.

Figure 1. Intel® IXF1110 MAC Block Diagram

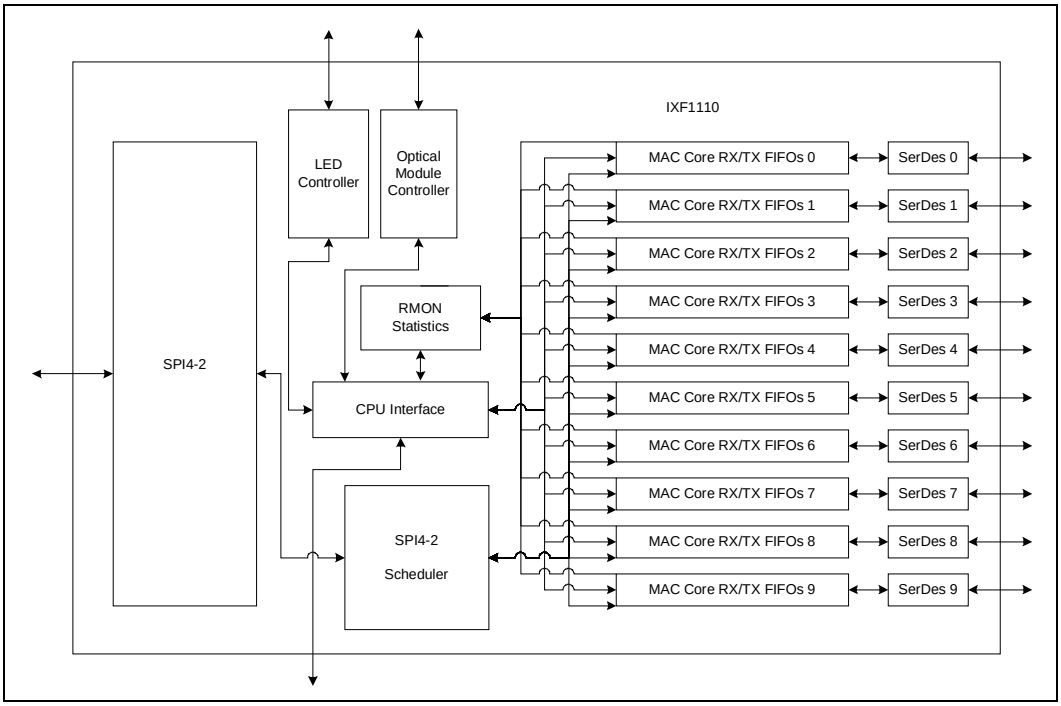
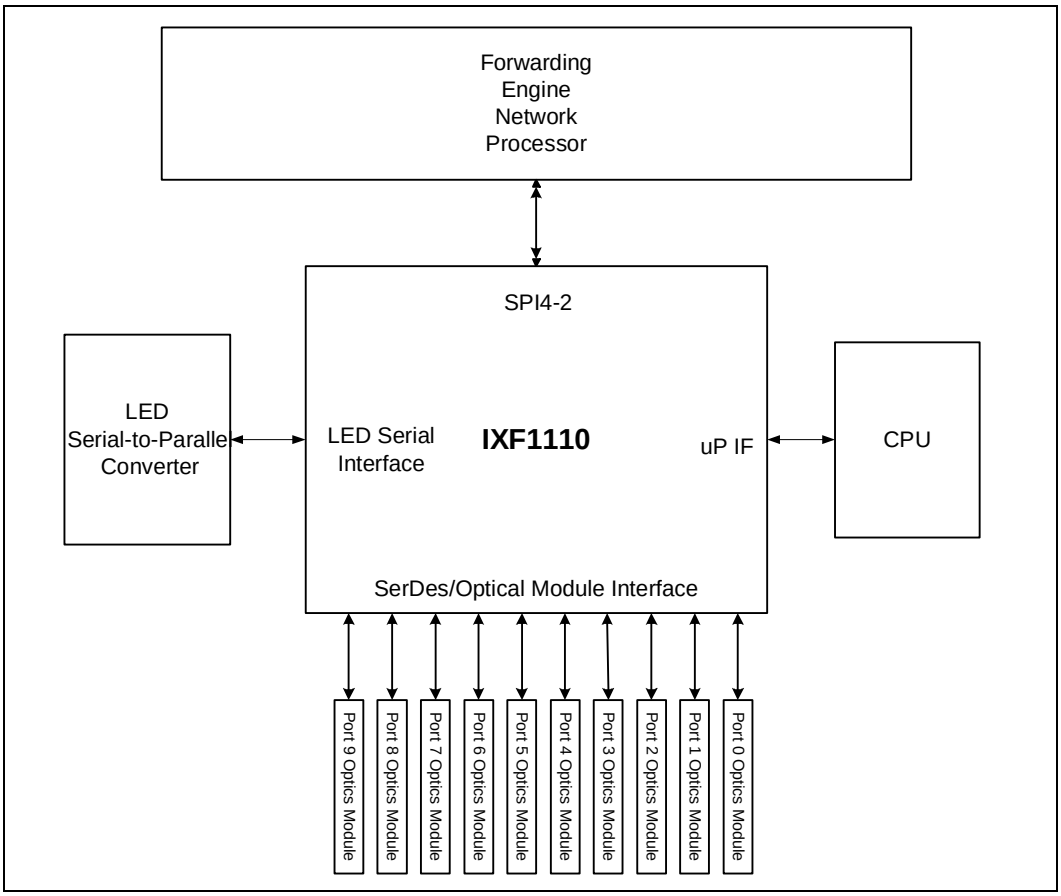


Figure 2. Intel® IXF1110 MAC System Block Diagram



3.0 Ball Assignments and Ball List Tables

Figure 3 illustrates the IXF1110 552-Ball CBGA assignments. Table 1 and Table 2 provide ball list tables in alphanumeric order by signal name and ball location under Section 3.1, "Ball List Tables" on page 18.

Figure 3. 552-Ball CBGA Assignments (Top View)

	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	AD1	AC1	AB1	AA1	Y1	W1	V1	U1	T1	R1	L1	N1	M1	L1	K1	J1	H1	G1	F1	E1	D1	C1	B1	A1	1
2	AD2	AC2	AB2	AA2	Y2	W2	V2	U2	T2	R2	P2	N2	M2	L2	K2	J2	H2	G2	F2	E2	D2	C2	B2	A2	2
3	AD3	AC3	AB3	AA3	Y3	W3	V3	U3	T3	R3	P3	N3	M3	L3	K3	J3	H3	G3	F3	E3	D3	C3	B3	A3	3
4	AD4	AC4	AB4	AA4	Y4	W4	V4	U4	T4	R4	P4	N4	M4	L4	K4	J4	H4	G4	F4	E4	D4	C4	B4	A4	4
5	AD5	AC5	AB5	AA5	Y5	W5	V5	U5	T5	R5	P5	N5	M5	L5	K5	J5	H5	G5	F5	E5	D5	C5	B5	A5	5
6	AD6	AC6	AB6	AA6	Y6	W6	V6	U6	T6	R6	P6	N6	M6	L6	K6	J6	H6	G6	F6	E6	D6	C6	B6	A6	6
7	AD7	AC7	AB7	AA7	Y7	W7	V7	U7	T7	R7	P7	N7	M7	L7	K7	J7	H7	G7	F7	E7	D7	C7	B7	A7	7
8	AD8	AC8	AB8	AA8	Y8	W8	V8	U8	T8	R8	P8	N8	M8	L8	K8	J8	H8	G8	F8	E8	D8	C8	B8	A8	8
9	AD9	AC9	AB9	AA9	Y9	W9	V9	U9	T9	R9	P9	N9	M9	L9	K9	J9	H9	G9	F9	E9	D9	C9	B9	A9	9
10	AD10	AC10	AB10	AA10	Y10	W10	V10	U10	T10	R10	P10	N10	M10	L10	K10	J10	H10	G10	F10	E10	D10	C10	B10	A10	10
11	AD11	AC11	AB11	AA11	Y11	W11	V11	U11	T11	R11	P11	N11	M11	L11	K11	J11	H11	G11	F11	E11	D11	C11	B11	A11	11
12	AD12	AC12	AB12	AA12	Y12	W12	V12	U12	T12	R12	P12	N12	M12	L12	K12	J12	H12	G12	F12	E12	D12	C12	B12	A12	12
13	AD13	AC13	AB13	AA13	Y13	W13	V13	U13	T13	R13	P13	N13	M13	L13	K13	J13	H13	G13	F13	E13	D13	C13	B13	A13	13
14	AD14	AC14	AB14	AA14	Y14	W14	V14	U14	T14	R14	P14	N14	M14	L14	K14	J14	H14	G14	F14	E14	D14	C14	B14	A14	14
15	AD15	AC15	AB15	AA15	Y15	W15	V15	U15	T15	R15	P15	N15	M15	L15	K15	J15	H15	G15	F15	E15	D15	C15	B15	A15	15
16	AD16	AC16	AB16	AA16	Y16	W16	V16	U16	T16	R16	P16	N16	M16	L16	K16	J16	H16	G16	F16	E16	D16	C16	B16	A16	16
17	AD17	AC17	AB17	AA17	Y17	W17	V17	U17	T17	R17	P17	N17	M17	L17	K17	J17	H17	G17	F17	E17	D17	C17	B17	A17	17
18	AD18	AC18	AB18	AA18	Y18	W18	V18	U18	T18	R18	P18	N18	M18	L18	K18	J18	H18	G18	F18	E18	D18	C18	B18	A18	18
19	AD19	AC19	AB19	AA19	Y19	W19	V19	U19	T19	R19	P19	N19	M19	L19	K19	J19	H19	G19	F19	E19	D19	C19	B19	A19	19
20	AD20	AC20	AB20	AA20	Y20	W20	V20	U20	T20	R20	P20	N20	M20	L20	K20	J20	H20	G20	F20	E20	D20	C20	B20	A20	20
21	AD21	AC21	AB21	AA21	Y21	W21	V21	U21	T21	R21	P21	N21	M21	L21	K21	J21	H21	G21	F21	E21	D21	C21	B21	A21	21
22	AD22	AC22	AB22	AA22	Y22	W22	V22	U22	T22	R22	P22	N22	M22	L22	K22	J22	H22	G22	F22	E22	D22	C22	B22	A22	22
23	AD23	AC23	AB23	AA23	Y23	W23	V23	U23	T23	R23	P23	N23	M23	L23	K23	J23	H23	G23	F23	E23	D23	C23	B23	A23	23
24	AD24	AC24	AB24	AA24	Y24	W24	V24	U24	T24	R24	P24	N24	M24	L24	K24	J24	H24	G24	F24	E24	D24	C24	B24	A24	24
	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

B2510-01

3.1 Ball List Tables

Ball list tables are provided in alphanumeric order by signal name (Table 1) and by ball location order (Table 2).

Note: Intel recommends that all unconnected balls be tied to their inactive states through external pull-ups or pull-downs.

3.1.1 Balls Listed in Alphanumeric Order by Signal Name

Table 1 shows the ball locations and signal names arranged in alphanumeric order by signal name.

Table 1. Ball List in Alphanumeric Order by Signal Name

Signal	Ball
AVDD1P8_1	D1
AVDD1P8_1	E24
AVDD1P8_2	P7
AVDD1P8_2	P18
AVDD1P8_2	V6
AVDD1P8_2	V11
AVDD1P8_2	V14
AVDD1P8_2	V18
AVDD2P5_1	Y1
AVDD2P5_2	N3
AVDD2P5_2	N22
AVDD2P5_2	P3
AVDD2P5_2	P22
AVDD2P5_2	V10
AVDD2P5_2	V15
CLK125	AA5
CLK50	C21
GND	B6
GND	B10
GND	B15
GND	B19
GND	C4
GND	D4
GND	D5
GND	D8
GND	D12
GND	D13
GND	D17
GND	D21
GND	D22
GND	D24
GND	E1
GND	F2
GND	F6
GND	F10
GND	F15
GND	F19
GND	F23
GND	G10
GND	H4
GND	H8
GND	H12
GND	H13
GND	H17
GND	H21
GND	J10
GND	J15
GND	J21
GND	J23
GND	K2
GND	K6
GND	K9
GND	K11
GND	K14
GND	K16
GND	K19
GND	K20
GND	K23
GND	K24
GND	L3
GND	L6
GND	L10
GND	L12
GND	L13
GND	L15
GND	L24
GND	M3
GND	M4
GND	M8
GND	M11
GND	M14
GND	M17
GND	M18
GND	M21
GND	N4
GND	N8
GND	N11
GND	N14
GND	N17
GND	N21
GND	P1
GND	P10
GND	P12
GND	P13

Signal	Ball
GND	P15
GND	P21
GND	P23
GND	P24
GND	R1
GND	R2
GND	R3
GND	R6
GND	R9
GND	R10
GND	R11
GND	R14
GND	R16
GND	R19
GND	R23
GND	R24
GND	T7
GND	T8
GND	T9
GND	T10
GND	T15
GND	T17
GND	T18
GND	T19
GND	T21
GND	T23
GND	U4
GND	U7
GND	U8
GND	U12
GND	U13
GND	U16
GND	U17
GND	U21
GND	V2
GND	V3
GND	V13
GND	V16
GND	W2

Signal	Ball
GND	W3
GND	W5
GND	W6
GND	W7
GND	W10
GND	W15
GND	W19
GND	W20
GND	W23
GND	Y2
GND	Y3
GND	Y8
GND	Y12
GND	Y13
GND	Y15
GND	Y16
GND	Y18
GND	AA1
GND	AA3
GND	AA4
GND	AA7
GND	AA8
GND	AA12
GND	AA13
GND	AA14
GND	AA17
GND	AA21
GND	AB6
GND	AB7
GND	AB10
GND	AB17
GND	AB21
GND	AB23
GND	AC6
GND	AC7
GND	AC10
GND	AC11
GND	AC15
GND	AC19

Signal	Ball
GND	AC20
GND	AD21
I^2C_CLK	L19
I^2C_DATA_0	G22
I^2C_DATA_1	G23
I^2C_DATA_2	J24
I^2C_DATA_3	F22
I^2C_DATA_4	E23
I^2C_DATA_5	H24
I^2C_DATA_6	G20
I^2C_DATA_7	E22
I^2C_DATA_8	G24
I^2C_DATA_9	F24
LED_CLK	A19
LED_DATA	A20
LED_LATCH	K18
MOD_DEF_0	N24
MOD_DEF_1	Y21
MOD_DEF_2	AA16
MOD_DEF_3	M20
MOD_DEF_4	AC14
MOD_DEF_5	U11
MOD_DEF_6	T4
MOD_DEF_7	AB2
MOD_DEF_8	R7
MOD_DEF_9	L1
MOD_DEF_INT	G15
NC	A5
NC	A6
NC	C10
NC	C15
NC	G7
NC	G8
NC	H22
NC	J22
NC	K7
NC	L21
NC	L23
NC	M1

Signal	Ball
NC	M7
NC	N1
NC	N5
NC	N7
NC	N20
NC	P4
NC	P5
NC	P6
NC	P17
NC	P19
NC	P20
NC	R5
NC	R13
NC	R18
NC	R20
NC	R22
NC	T1
NC	T6
NC	U1
NC	V1
NC	V8
NC	V9
NC	V19
NC	W1
NC	W16
NC	W18
NC	Y7
NC	Y10
NC	Y11
NC	Y14
NC	AA11
NC	AA20
NC	AA22
NC	AB3
NC	AB5
NC	AB8
NC	AB18
NC	AB19
NC	AB20

Signal	Ball
NC	AB22
NC	AD4
NC	AD5
NC	AD6
NC	AD7
NC	AD8
NC	AD17
NC	AD19
NC	AD20
No Ball	A2
No Ball	A3
No Ball	A22
No Ball	A23
No Ball	A24
No Ball	B1
No Ball	B2
No Ball	B23
No Ball	B24
No Ball	C1
No Ball	C24
No Ball	AB1
No Ball	AB24
No Ball	AC1
No Ball	AC2
No Ball	AC23
No Ball	AC24
No Ball	AD1
No Ball	AD2
No Ball	AD3
No Ball	AD22
No Ball	AD23
No Ball	AD24
No Pad	A1
RCTL_N	H18
RCTL_P	H16
RDAT0_N	E20
RDAT0_P	E19
RDAT1_N	C20
RDAT1_P	B20

Signal	Ball
RDAT2_N	G19
RDAT2_P	F18
RDAT3_N	H20
RDAT3_P	G21
RDAT4_N	J19
RDAT4_P	J18
RDAT5_N	L18
RDAT5_P	L17
RDAT6_N	E17
RDAT6_P	E16
RDAT7_N	N15
RDAT7_P	M15
RDAT8_N	D16
RDAT8_P	C16
RDAT9_N	E18
RDAT9_P	D18
RDAT10_N	G18
RDAT10_P	G17
RDAT11_N	K15
RDAT11_P	J16
RDAT12_N	A14
RDAT12_P	A13
RDAT13_N	E14
RDAT13_P	E13
RDAT14_N	G16
RDAT14_P	F16
RDAT15_N	K13
RDAT15_P	K12
RDCLK_N	C19
RDCLK_P	C18
RSCLK	J17
RSTAT0	L20
RSTAT1	J20
RX_LOS_0	L22
RX_LOS_1	V17
RX_LOS_2	AD18
RX_LOS_3	R12
RX_LOS_4	AB15
RX_LOS_5	V12

Signal	Ball
RX_LOS_6	Y9
RX_LOS_7	AC3
RX_LOS_8	T2
RX_LOS_9	P2
RX_LOS_INT	B14
RX_N_0	U22
RX_N_1	U20
RX_N_2	T24
RX_N_3	V24
RX_N_4	AB14
RX_N_5	AD14
RX_N_6	AC16
RX_N_7	AD15
RX_N_8	V4
RX_N_9	Y5
RX_P_0	T22
RX_P_1	T20
RX_P_2	U24
RX_P_3	W24
RX_P_4	AB13
RX_P_5	AD13
RX_P_6	AB16
RX_P_7	AD16
RX_P_8	V5
RX_P_9	Y6
SYS_RES_L	Y4
TCK	AA24
TCTL_N	N10
TCTL_P	M10
TDAT0_N	J5
TDAT0_P	J6
TDAT1_N	J3
TDAT1_P	H3
TDAT2_P	B5
TDAT3_N	H9
TDAT3_P	G9
TDAT4_P	F7
TDAT4_P	G6
TDAT5_N	H5

Signal	Ball
TDAT5_P	G5
TDAT6_N	L7
TDAT6_P	L8
TDAT7_N	C6
TDAT7_P	C7
TDAT8_N	M5
TDAT8_P	L5
TDAT9_N	C8
TDAT9_P	B7
TDAT10_N	F9
TDAT10_P	E9
TDAT11_N	E7
TDAT11_P	E8
TDAT12_N	J8
TDAT12_P	H7
TDAT13_N	K10
TDAT13_P	J9
TDAT14_N	D9
TDAT14_P	C9
TDAT15_N	H11
TDAT15_P	G11
TDAT2_N	C5
TDCLK-	E4
TDCLK_P	D3
TDI	AC18
TDO	Y24
TMS	T16
TRST_L	N18
TSCLK	C11
TSTAT0	E5
TSTAT1	E6
TX_DISABLE_0	K22
TX_DISABLE_1	M22
TX_DISABLE_2	AC22
TX_DISABLE_3	U18
TX_DISABLE_4	U14
TX_DISABLE_5	AA18
TX_DISABLE_6	U9
TX_DISABLE_7	AA9

Signal	Ball
TX_DISABLE_8	V7
TX_DISABLE_9	L4
TX_FAULT_0	M24
TX_FAULT_1	V23
TX_FAULT_2	Y17
TX_FAULT_3	R15
TX_FAULT_4	W14
TX_FAULT_5	W11
TX_FAULT_6	W9
TX_FAULT_7	AC5
TX_FAULT_8	P8
TX_FAULT_9	L2
TX_FAULT_INT	B11
TX_N_0	V21
TX_N_1	Y20
TX_N_2	W22
TX_N_3	Y22
TX_N_4	AB11
TX_N_5	AD11
TX_N_6	AC9
TX_N_7	AD10
TX_N_8	U3
TX_N_9	U5
TX_P_0	V20
TX_P_1	Y19
TX_P_2	V22
TX_P_3	Y23
TX_P_4	AB12
TX_P_5	AD12
TX_P_6	AB9
TX_P_7	AD9
TX_P_8	T3
TX_P_9	T5
TXPAUSEADD0	G3
TXPAUSEADD1	G2
TXPAUSEADD2	J2
TXPAUSEADD3	K1
TXPAUSEFR	J7
UPX_ADD0	J1

Signal	Ball
UPX_ADD2	F3
UPX_ADD3	H1
UPX_ADD4	E3
UPX_ADD5	E2
UPX_ADD6	G1
UPX_ADD7	C3
UPX_ADD8	F5
UPX_ADD9	F1
UPX_ADD1	G4
UPX_ADD10	C2
UPX_CS_L	F20
UPX_DATA0	B3
UPX_DATA1	A4
UPX_DATA2	B9
UPX_DATA3	A7
UPX_DATA4	C12
UPX_DATA5	E11
UPX_DATA6	C13
UPX_DATA7	A8
UPX_DATA8	A10
UPX_DATA9	A9
UPX_DATA10	E12
UPX_DATA11	A11
UPX_DATA12	G12
UPX_DATA13	E10
UPX_DATA14	F11
UPX_DATA15	D7
UPX_DATA16	D14
UPX_DATA17	C14
UPX_DATA18	F14
UPX_DATA19	A12
UPX_DATA20	A15
UPX_DATA21	G13
UPX_DATA22	B16
UPX_DATA23	E15
UPX_DATA24	G14
UPX_DATA25	A16
UPX_DATA26	C17
UPX_DATA27	A17

Signal	Ball
UPX_DATA28	B18
UPX_DATA29	A21
UPX_DATA30	B22
UPX_DATA31	C23
UPX_RD_L	H14
UPX_RDY_L	C22
UPX_WR_L	A18
VDD	D6
VDD	D10
VDD	D11
VDD	D15
VDD	D19
VDD	D20
VDD	E21
VDD	F4
VDD	F21
VDD	H10
VDD	H15
VDD	J4
VDD	J11
VDD	J14
VDD	K3
VDD	K4
VDD	K5
VDD	K8
VDD	K17
VDD	K21
VDD	L9
VDD	L11
VDD	L14
VDD	L16
VDD	P9
VDD	P11
VDD	P14
VDD	P16
VDD	R4
VDD	R8
VDD	R17
VDD	R21

Signal	Ball
VDD	T11
VDD	T14
VDD	U10
VDD	U15
VDD	W4
VDD	W21
VDD	AA6
VDD	AA10
VDD	AA15
VDD	AA19
VDD	AB4
VDD2	B4
VDD2	B8
VDD2	B12
VDD2	B13
VDD2	B17
VDD2	B21
VDD2	D2
VDD2	D23
VDD2	F8
VDD2	F12
VDD2	F13
VDD2	F17
VDD2	H2
VDD2	H6
VDD2	H19
VDD2	H23
VDD2	J12
VDD2	J13
VDD2	M2
VDD2	M6
VDD2	M9
VDD2	M12
VDD2	M13
VDD2	M16
VDD2	M19
VDD2	M23
VDD2	N2
VDD2	N6

Signal	Ball
VDD2	N9
VDD2	N12
VDD2	N13
VDD2	N16
VDD2	N19
VDD2	N23
VDD2	T12
VDD2	T13
VDD2	U2
VDD2	U6
VDD2	U19
VDD2	U23
VDD2	W8
VDD2	W12
VDD2	W13
VDD2	W17
VDD2	AA2
VDD2	AA23
VDD2	AC4
VDD2	AC8
VDD2	AC12
VDD2	AC13
VDD2	AC17
VDD2	AC21

3.1.2 Balls Listed in Alphanumeric Order by Ball Location

Table 2 shows the ball locations and signal names arranged in alphanumeric order by ball location.

Note: Intel recommends that all unconnected balls be tied to their inactive states through external pull-ups or pull-downs.

Table 2. Ball List in Alphanumeric Order by Ball Location

Ball	Signal
A1	No Pad
A2	No Ball
A3	No Ball
A4	UPX_DATA1
A5	NC
A6	NC
A7	UPX_DATA3
A8	UPX_DATA7
A9	UPX_DATA9
A10	UPX_DATA8
A11	UPX_DATA11
A12	UPX_DATA19
A13	RDAT12_P
A14	RDAT12_N
A15	UPX_DATA20
A16	UPX_DATA25
A17	UPX_DATA27
A18	UPX_WR_L
A19	LED_CLK
A20	LED_DATA
A21	UPX_DATA29
A22	No Ball
A23	No Ball
A24	No Ball
B1	No Ball
B2	No Ball
B3	UPX_DATA0
B4	VDD2
B5	TDAT2_P
B6	GND
B7	TDAT9_P
B8	VDD2
B9	UPX_DATA2
B10	GND
B11	TX_FAULT_INT
B12	VDD2
B13	VDD2
B14	RX_LOS_INT
B15	GND
B16	UPX_DATA22
B17	VDD2
B18	UPX_DATA28
B19	GND
B20	RDAT1_P
B21	VDD2
B22	UPX_DATA30
B23	No Ball
B24	No Ball
C1	No Ball
C2	UPX_ADD10
C3	UPX_ADD7
C4	GND
C5	TDAT2_N
C6	TDAT7_N
C7	TDAT7_P
C8	TDAT9_N
C9	TDAT14_P
C10	NC
C11	TSCLK
C12	UPX_DATA4
C13	UPX_DATA6
C14	UPX_DATA17
C15	NC
C16	RDAT8_P
C17	UPX_DATA26
C18	RDCLK_P
C19	RDCLK_N
C20	RDAT1_N
C21	CLK50
C22	UPX_RDY_L
C23	UPX_DATA31
C24	No Ball
D1	AVDD1P8_1
D2	VDD2
D3	TDCLK_P
D4	GND
D5	GND
D6	VDD
D7	UPX_DATA15
D8	GND
D9	TDAT14_N
D10	VDD
D11	VDD
D12	GND
D13	GND
D14	UPX_DATA16
D15	VDD
D16	RDAT8_N
D17	GND
D18	RDAT9_P
D19	VDD
D20	VDD
D21	GND
D22	GND
D23	VDD2
D24	GND

Ball	Signal
E1	GND
E2	UPX_ADD5
E3	UPX_ADD4
E4	TDCLK-
E5	TSTAT0
E6	TSTAT1
E7	TDAT11_N
E8	TDAT11_P
E9	TDAT10_P
E10	UPX_DATA13
E11	UPX_DATA5
E12	UPX_DATA10
E13	RDAT13_P
E14	RDAT13_N
E15	UPX_DATA23
E16	RDAT6_P
E17	RDAT6_N
E18	RDAT9_N
E19	RDAT0_P
E20	RDAT0_N
E21	VDD
E22	I^2C_DATA_7
E23	I^2C_DATA_4
E24	AVDD1P8_1
F1	UPX_ADD9
F2	GND
F3	UPX_ADD2
F4	VDD
F5	UPX_ADD8
F6	GND
F7	TDAT4_P
F8	VDD2
F9	TDAT10_N
F10	GND
F11	UPX_DATA14
F12	VDD2
F13	VDD2
F14	UPX_DATA18
F15	GND

Ball	Signal
F16	RDAT14_P
F17	VDD2
F18	RDAT2_P
F19	GND
F20	UPX_CS_L
F21	VDD
F22	I^2C_DATA_3
F23	GND
F24	I^2C_DATA_9
G1	UPX_ADD6
G2	TXPAUSEADD1
G3	TXPAUSEADD0
G4	UPX_ADD1
G5	TDAT5_P
G6	TDAT4_P
G7	NC
G8	NC
G9	TDAT3_P
G10	GND
G11	TDAT15_P
G12	UPX_DATA12
G13	UPX_DATA21
G14	UPX_DATA24
G15	MOD_DEF_INT
G16	RDAT14_N
G17	RDAT10_P
G18	RDAT10_N
G19	RDAT2_N
G20	I^2C_DATA_6
G21	RDAT3_P
G22	I^2C_DATA_0
G23	I^2C_DATA_1
G24	I^2C_DATA_8
H1	UPX_ADD3
H2	VDD2
H3	TDAT1_P
H4	GND
H5	TDAT5_N
H6	VDD2

Ball	Signal
H7	TDAT12_P
H8	GND
H9	TDAT3_N
H10	VDD
H11	TDAT15_N
H12	GND
H13	GND
H14	UPX_RD_L
H15	VDD
H16	RCTL_P
H17	GND
H18	RCTL_N
H19	VDD2
H20	RDAT3_N
H21	GND
H22	NC
H23	VDD2
H24	I^2C_DATA_5
J1	UPX_ADD0
J2	TXPAUSEADD2
J3	TDAT1_N
J4	VDD
J5	TDAT0_N
J6	TDAT0_P
J7	TXPAUSEFR
J8	TDAT12_N
J9	TDAT13_P
J10	GND
J11	VDD
J12	VDD2
J13	VDD2
J14	VDD
J15	GND
J16	RDAT11_P
J17	RSCLK
J18	RDAT4_P
J19	RDAT4_N
J20	RSTAT1
J21	GND

Ball	Signal
J22	NC
J23	GND
J24	I^2C_DATA_2
K1	TXPAUSEADD3
K2	GND
K3	VDD
K4	VDD
K5	VDD
K6	GND
K7	NC
K8	VDD
K9	GND
K10	TDAT13_N
K11	GND
K12	RDAT15_P
K13	RDAT15_N
K14	GND
K15	RDAT11_N
K16	GND
K17	VDD
K18	LED_LATCH
K19	GND
K20	GND
K21	VDD
K22	TX_DISABLE_0
K23	GND
K24	GND
L1	MOD_DEF_9
L2	TX_FAULT_9
L3	GND
L4	TX_DISABLE_9
L5	TDAT8_P
L6	GND
L7	TDAT6_N
L8	TDAT6_P
L9	VDD
L10	GND
L11	VDD
L12	GND

Ball	Signal
L13	GND
L14	VDD
L15	GND
L16	VDD
L17	RDAT5_P
L18	RDAT5_N
L19	I^2C_CLK
L20	RSTAT0
L21	NC
L22	RX_LOS_0
L23	NC
L24	GND
M1	NC
M2	VDD2
M3	GND
M4	GND
M5	TDAT8_N
M6	VDD2
M7	NC
M8	GND
M9	VDD2
M10	TCTL_P
M11	GND
M12	VDD2
M13	VDD2
M14	GND
M15	RDAT7_P
M16	VDD2
M17	GND
M18	GND
M19	VDD2
M20	MOD_DEF_3
M21	GND
M22	TX_DISABLE_1
M23	VDD2
M24	TX_FAULT_0
N1	NC
N2	VDD2
N3	AVDD2P5_2

Ball	Signal
N4	GND
N5	NC
N6	VDD2
N7	NC
N8	GND
N9	VDD2
N10	TCTL_N
N11	GND
N12	VDD2
N13	VDD2
N14	GND
N15	RDAT7_N
N16	VDD2
N17	GND
N18	TRST_L
N19	VDD2
N20	NC
N21	GND
N22	AVDD2P5_2
N23	VDD2
N24	MOD_DEF_0
P1	GND
P2	RX_LOS_9
P3	AVDD2P5_2
P4	NC
P5	NC
P6	NC
P7	AVDD1P8_2
P8	TX_FAULT_8
P9	VDD
P10	GND
P11	VDD
P12	GND
P13	GND
P14	VDD
P15	GND
P16	VDD
P17	NC
P18	AVDD1P8_2

Ball	Signal
P19	NC
P20	NC
P21	GND
P22	AVDD2P5_2
P23	GND
P24	GND
R1	GND
R2	GND
R3	GND
R4	VDD
R5	NC
R6	GND
R7	MOD_DEF_8
R8	VDD
R9	GND
R10	GND
R11	GND
R12	RX_LOS_3
R13	NC
R14	GND
R15	TX_FAULT_3
R16	GND
R17	VDD
R18	NC
R19	GND
R20	NC
R21	VDD
R22	NC
R23	GND
R24	GND
T1	NC
T2	RX_LOS_8
T3	TX_P_8
T4	MOD_DEF_6
T5	TX_P_9
T6	NC
T7	GND
T8	GND
T9	GND

Ball	Signal
T10	GND
T11	VDD
T12	VDD2
T13	VDD2
T14	VDD
T15	GND
T16	TMS
T17	GND
T18	GND
T19	GND
T20	RX_P_1
T21	GND
T22	RX_P_0
T23	GND
T24	RX_N_2
U1	NC
U2	VDD2
U3	TX_N_8
U4	GND
U5	TX_N_9
U6	VDD2
U7	GND
U8	GND
U9	TX_DISABLE_6
U10	VDD
U11	MOD_DEF_5
U12	GND
U13	GND
U14	TX_DISABLE_4
U15	VDD
U16	GND
U17	GND
U18	TX_DISABLE_3
U19	VDD2
U20	RX_N_1
U21	GND
U22	RX_N_0
U23	VDD2
U24	RX_P_2

Ball	Signal
V1	NC
V2	GND
V3	GND
V4	RX_N_8
V5	RX_P_8
V6	AVDD1P8_2
V7	TX_DISABLE_8
V8	NC
V9	NC
V10	AVDD2P5_2
V11	AVDD1P8_2
V12	RX_LOS_5
V13	GND
V14	AVDD1P8_2
V15	AVDD2P5_2
V16	GND
V17	RX_LOS_1
V18	AVDD1P8_2
V19	NC
V20	TX_P_0
V21	TX_N_0
V22	TX_P_2
V23	TX_FAULT_1
V24	RX_N_3
W1	NC
W2	GND
W3	GND
W4	VDD
W5	GND
W6	GND
W7	GND
W8	VDD2
W9	TX_FAULT_6
W10	GND
W11	TX_FAULT_5
W12	VDD2
W13	VDD2
W14	TX_FAULT_4
W15	GND

Ball	Signal
W16	NC
W17	VDD2
W18	NC
W19	GND
W20	GND
W21	VDD
W22	TX_N_2
W23	GND
W24	RX_P_3
Y1	AVDD2P5_1
Y2	GND
Y3	GND
Y4	SYS_RES_L
Y5	RX_N_9
Y6	RX_P_9
Y7	NC
Y8	GND
Y9	RX_LOS_6
Y10	NC
Y11	NC
Y12	GND
Y13	GND
Y14	NC
Y15	GND
Y16	GND
Y17	TX_FAULT_2
Y18	GND
Y19	TX_P_1
Y20	TX_N_1
Y21	MOD_DEF_1
Y22	TX_N_3
Y23	TX_P_3
Y24	TDO
AA1	GND
AA2	VDD2
AA3	GND
AA4	GND
AA5	CLK125
AA6	VDD

Ball	Signal
AA7	GND
AA8	GND
AA9	TX_DISABLE_7
AA10	VDD
AA11	NC
AA12	GND
AA13	GND
AA14	GND
AA15	VDD
AA16	MOD_DEF_2
AA17	GND
AA18	TX_DISABLE_5
AA19	VDD
AA20	NC
AA21	GND
AA22	NC
AA23	VDD2
AA24	TCK
AB1	No Ball
AB2	MOD_DEF_7
AB3	NC
AB4	VDD
AB5	NC
AB6	GND
AB7	GND
AB8	NC
AB9	TX_P_6
AB10	GND
AB11	TX_N_4
AB12	TX_P_4
AB13	RX_P_4
AB14	RX_N_4
AB15	RX_LOS_4
AB16	RX_P_6
AB17	GND
AB18	NC
AB19	NC
AB20	NC
AB21	GND

Ball	Signal
AB22	NC
AB23	GND
AB24	No Ball
AC1	No Ball
AC2	No Ball
AC3	RX_LOS_7
AC4	VDD2
AC5	TX_FAULT_7
AC6	GND
AC7	GND
AC8	VDD2
AC9	TX_N_6
AC10	GND
AC11	GND
AC12	VDD2
AC13	VDD2
AC14	MOD_DEF_4
AC15	GND
AC16	RX_N_6
AC17	VDD2
AC18	TDI
AC19	GND
AC20	GND
AC21	VDD2
AC22	TX_DISABLE_2
AC23	No Ball
AC24	No Ball
AD1	No Ball
AD2	No Ball
AD3	No Ball
AD4	NC
AD5	NC
AD6	NC
AD7	NC
AD8	NC
AD9	TX_P_7
AD10	TX_N_7
AD11	TX_N_5
AD12	TX_P_5

Ball	Signal
AD13	RX_P_5
AD14	RX_N_5
AD15	RX_N_7
AD16	RX_P_7
AD17	NC
AD18	RX_LOS_2
AD19	NC
AD20	NC
AD21	GND
AD22	No Ball
AD23	No Ball
AD24	No Ball

4.0 Ball Assignments and Signal Descriptions

4.1 Naming Conventions

4.1.1 Signal Name Conventions

Signal names begin with a Signal Mnemonic, and can also contain one or more of the following designations: a differential pair designation, a serial designation, and an active Low designation. Signal naming conventions are as follows:

Differential Pair + Port Designation. The positive and negative components of differential pairs tied to a specific port are designated by the Signal Mnemonic, immediately followed by an underscore and either P (positive component) or N (negative component), and an underscore followed by the port designation. For example, SerDes interface signals for port 0 are identified as TX_P_0 and TX_N_0.

Serial Designation. A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by a bracketed serial designation. For example, the set of 11 CPU Address Bus signals is identified as UPX_ADD[10:0].

Port Designation. Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, Optical module I^2C Serial Data signals would be identified as I^2C_DATA_0, I^2C_DATA_1, etc.

Active Low Designation. A control input or indicator output that is active Low is designated by a final suffix consisting of an underscore followed by an upper case “L”. For example, the CPU cycle complete identifier is shown as UPX_RDY_L.

4.1.2 Register Address Conventions

Registers located in on-chip memory are accessed using a register address, which is provided in Hex notation. A Register Address is indicated by the dollar sign ($), followed by the memory location in Hex.

4.2 Interface Signal Groups

This section describes the IXF1110 signals in groups according to the associated interface or function. Figure 4 and Table 3, “SPI4-2 Interface Signal Descriptions” through Table 12, “Unused Balls/Reserved” describe the signals used by the IXF1110.

Figure 4. Interface Diagram

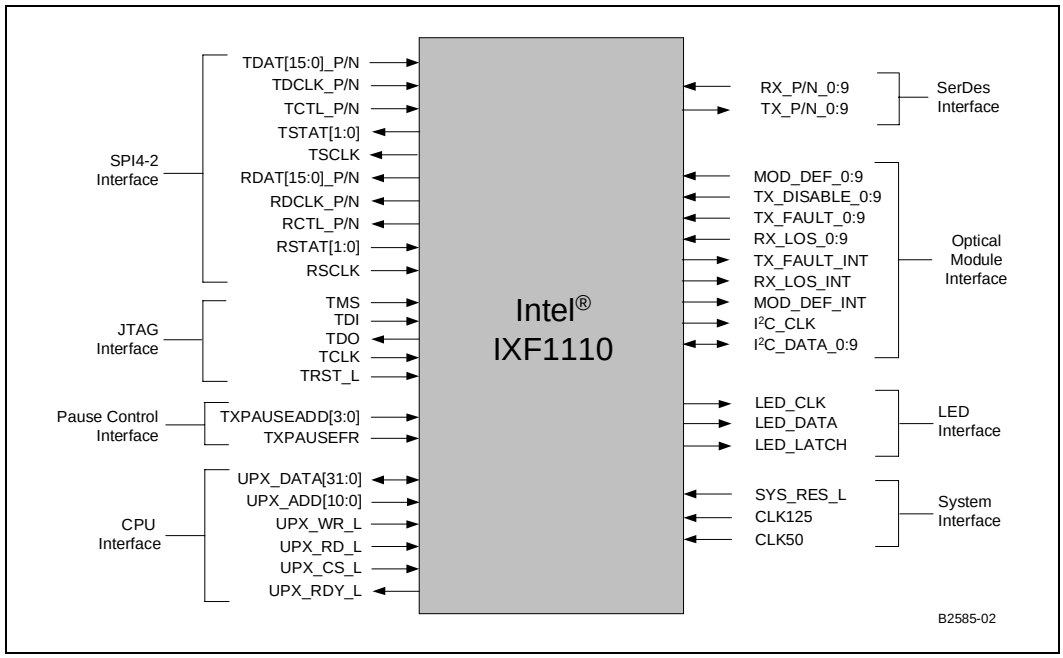


Table 3. SPI4-2 Interface Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
TDAT15_P, TDAT15_N TDAT14_P, TDAT14_N TDAT13_P, TDAT13_N TDAT12_P, TDAT12_N TDAT11_P, TDAT11_N TDAT10_P, TDAT10_N TDAT9_P, TDAT9_N TDAT8_P, TDAT8_N TDAT7_P, TDAT7_N TDAT6_P, TDAT6_N TDAT5_P, TDAT5_N TDAT4_P, TDAT4_N TDAT3_P, TDAT3_N TDAT2_P, TDAT2_N TDAT1_P, TDAT1_N TDAT0_P, TDAT0_N	G11 H11 C9 D9 J9 K10 H7 J8 E8 E7 E9 F9 B7 C8 L5 M5 C7 C6 L8 L7 G5 H5 F7 G6 G9 H9 B5 C5 H3 J3 J6 J5	Input	LVDS	**Transmit Data Bus:** Carries payload data and in-band control words to the IXF1110 link-layer device. Internally terminated differentially with 100 Ω.
TDCLK_P TDCLK_N	D3 E4	Input	LVDS	**Transmit Data Clock:** Clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω. **NOTE:** If TDCLK is applied to the IXF1110 after the device has come out of reset, the system designer must ensure the TDCLK is stable when applied. Failure to due so can result in the IXF1110 training on a non-stable clock, causing DIP4 errors and data corruption.
TCTL_P TCTL_N	M10 N10	Input	LVDS	**Transmit Control:** TCTL is High when a control word is present on TDAT[15:0]. Otherwise, TCTL is Low. Internally terminated differentially with 100 Ω.
TSCLK	C11	Output	2.5 V LVTTL	**Transmit Status Clock:** Clock associated with TSTAT [1:0]. Frequency is equal to one-quarter TDCLK.
TSTAT1 TSTAT0	E6 E5	Output	2.5 V LVTTL	**Transmit FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.

Table 3. SPI4-2 Interface Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
RDAT15_P, RDAT15_N RDAT14_P, RDAT14_N RDAT13_P, RDAT13_N RDAT12_P, RDAT12_N RDAT11_P, RDAT11_N RDAT10_P, RDAT10_N RDAT9_P, RDAT9_N RDAT8_P, RDAT8_N RDAT7_P, RDAT7_N RDAT6_P, RDAT6_N RDAT5_P, RDAT5_N RDAT4_P, RDAT4_N RDAT3_P, RDAT3_N RDAT2_P, RDAT2_N- RDAT1_P, RDAT1_N RDAT0_P, RDAT0_N	K12 K13 F16 G16 E13 E14 A13 A14 J16 K15 G17 G18 D18 E18 C16 D16 M15 N15 E16 E17 L17 L18 J18 J19 G21 H20 F18 G19 B20 C20 E19 E20	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1110 link-layer device. Internally terminated differentially with 100 Ω.
RDCLK_P RDCLK_N	C18 C19	Output	LVDS	**Receive Data Clock:** Clock associated with RDAT[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock. The frequency range is 320-400 Mhz. Frequency is always a multiplied- by-8 version of the CLK50 reference clock. Internally terminated differentially with 100 Ω.
RCTL_P RCTL_N	H16 H18	Output	LVDS	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low. Internally terminated differentially with 100 Ω.
RSCLK	J17	Input	2.5 V LVTTL	**Receive Status Clock:** The clock associated with RSTAT[1:0].
RSTAT1 RSTAT0	J20 L20	Input	2.5 V LVTTL	**Receive FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.

Table 4. SerDes Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
TX_P_0, TX_N_0 TX_P_1, TX_N_1 TX_P_2, TX_N_2 TX_P_3, TX_N_3 TX_P_4, TX_N_4 TX_P_5, TX_N_5 TX_P_6, TX_N_6 TX_P_7, TX_N_7 TX_P_8, TX_N_8 TX_P_9, TX_N_9	V20 V21 Y19 Y20 V22 W22 Y23 Y22 AB12 AB11 AD12 AD11 AB9 AC9 AD9 AD10 T3 U3 T5 U5	Output	SerDes	**Transmit Differential Output:** Carries the 1.25 GHz data to the optics module.
RX_P_0, RX_N_0 RX_P_1, RX_N_1 RX_P_2, RX_N_2 RX_P_3, RX_N_3 RX_P_4, RX_N_4 RX_P_5, RX_N_5 RX_P_6, RX_N_6 RX_P_7, RX_N_7 RX_P_8, RX_N_8 RX_P_9, RX_N_9	T22 U22 T20 U20 U24 T24 W24 V24 AB13 AB14 AD13 AD14 AB16 AC16 AD16 AD15 V5 V4 Y6 Y5	Input	SerDes	**Receive Differential Input:** Carries the 1.25 GHz data from the optics module. Internally terminated differentially with 100 Ω.

Table 5. CPU Interface Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
UPX_ADD10 UPX_ADD9 UPX_ADD8 UPX_ADD7 UPX_ADD6 UPX_ADD5 UPX_ADD4 UPX_ADD3 UPX_ADD2 UPX_ADD1 UPX_ADD0	C2 F1 F5 C3 G1 E2 E3 H1 F3 G4 J1	Input	2.5 V CMOS	**Address bus:** 11-bit address bus
UPX_CS_L	F20	Input	2.5 V CMOS	**Chip Select Signal:** Active Low chip select
UPX_DATA31 UPX_DATA30 UPX_DATA29 UPX_DATA28 UPX_DATA27 UPX_DATA26 UPX_DATA25 UPX_DATA24 UPX_DATA23 UPX_DATA22 UPX_DATA21 UPX_DATA20 UPX_DATA19 UPX_DATA18 UPX_DATA17 UPX_DATA16 UPX_DATA15 UPX_DATA14 UPX_DATA13 UPX_DATA12 UPX_DATA11 UPX_DATA10 UPX_DATA9 UPX_DATA8 UPX_DATA7 UPX_DATA6 UPX_DATA5 UPX_DATA4 UPX_DATA3 UPX_DATA2 UPX_DATA1 UPX_DATA0	C23 B22 A21 B18 A17 C17 A16 G14 E15 B16 G13 A15 A12 F14 C14 D14 D7 F11 E10 G12 A11 E12 A9 A10 A8 C13 E11 C12 A7 B9 A4 B3	Input/ Output	2.5 V CMOS	**Bi-directional data bus:** 32-bit bi-directional data bus
1. This I/O meets the 2.5 V CMOS specification only during boundary scan mode.				

Table 5. CPU Interface Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
UPX_WR_L	A18	Input	2.5 V CMOS	**Write Strobe:** Active Low Write strobe
UPX_RD_L	H14	Input	2.5 V CMOS	**Read Strobe:** Active Low Read strobe
UPX_RDY_L	C22	Open Drain Output*	2.5 V CMOS[1]	**Cycle complete indicator:** Indicates that Read or Write is complete. **NOTE:** An external pull-up resistor is required for proper operation. **NOTE:** *Dual-mode I/O. Normal operation: Open drain output Boundary Scan Mode: Standard CMOS output
1. This I/O meets the 2.5 V CMOS specification only during boundary scan mode.				

Table 6. Pause Control Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
TXPAUSEFR	J7	Input	2.5 V CMOS	**Pause Strobe:** Indicates when a Pause frame is to be sent
TXPAUSEADD3 TXPAUSEADD2 TXPAUSEADD1 TXPAUSEADD0	K1 J2 G2 G3	Input	2.5 V CMOS	**Pause Address Bus:** Selects the port for the Pause frames

Table 7. Optical Module Interface Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
TX_FAULT_0 TX_FAULT_1 TX_FAULT_2 TX_FAULT_3 TX_FAULT_4 TX_FAULT_5 TX_FAULT_6 TX_FAULT_7 TX_FAULT_8 TX_FAULT_9	M24 V23 Y17 R15 W14 W11 W9 AC5 P8 L2	Input	2.5 V CMOS	**Transmitter Fault:** Input used to determine when there is a optical module transmitter fault.
RX_LOS_0 RX_LOS_1 RX_LOS_2 RX_LOS_3 RX_LOS_4 RX_LOS_5 RX_LOS_6 RX_LOS_7 RX_LOS_8 RX_LOS_9	L22 V17 AD18 R12 AB15 V12 Y9 AC3 T2 P2	Input	2.5 V CMOS	**Receiver Loss of Signal:** Input used to determine when the optical module receiver loses synchronization.
MOD_DEF_0 MOD_DEF_1 MOD_DEF_2 MOD_DEF_3 MOD_DEF_4 MOD_DEF_5 MOD_DEF_6 MOD_DEF_7 MOD_DEF_8 MOD_DEF_9	N24 Y21 AA16 M20 AC14 U11 T4 AB2 R7 L1	Input	2.5 V CMOS	**Module Definition:** Input used to determine when a optical module module is present.
TX_DISABLE_0 TX_DISABLE_1 TX_DISABLE_2 TX_DISABLE_3 TX_DISABLE_4 TX_DISABLE_5 TX_DISABLE_6 TX_DISABLE_7 TX_DISABLE_8 TX_DISABLE_9	K22 M22 AC22 U18 U14 AA18 U9 AA9 V7 L4	Open Drain Output*	2.5 V CMOS[1]	**Transmitter Disable:** Output used to disable a optical module transmitter. External pull-up resistor usually resident in a optical module is required for proper operation. **NOTE:** *Dual-mode I/O. Normal operation: Open drain output Boundary Scan Mode: Standard CMOS output
TX_FAULT_INT	B11	Open Drain Output*	2.5 V CMOS[1]	**Transmitter Fault interrupt:** Open drain output interrupt to signal a TX_FAULT condition. **NOTE:** *Dual-mode I/O. Normal operation: Open drain output Boundary Scan Mode: Standard CMOS output

1. This I/O meets the 2.5 V CMOS specification only during boundary scan mode.

Table 7. Optical Module Interface Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
RX_LOS_INT	B14	Open Drain Output*	2.5 V CMOS[1]	**Receiver Loss of Signal Interrupt:** Open drain output interrupt to signal an RX_LOS condition. **NOTE:** *Dual-mode I/O. Normal operation: Open drain output Boundary Scan Mode: Standard CMOS output
MOD_DEF_INT	G15	Open Drain Output*	2.5 V CMOS[1]	**Module Definition Interrupt:** Open drain output interrupt to signal a MOD_DEF condition. **NOTE:** *Dual-mode I/O. Normal operation: Open drain output Boundary Scan Mode: Standard CMOS output
I^2C_CLK	L19	Output	2.5 V CMOS	**I^2C Reference Clock:** Clock used for I^2C bus interface.
I^2C_DATA_0 I^2C_DATA_1 I^2C_DATA_2 I^2C_DATA_3 I^2C_DATA_4 I^2C_DATA_5 I^2C_DATA_6 I^2C_DATA_7 I^2C_DATA_8 I^2C_DATA_9	G22 G23 J24 F22 E23 H24 G20 E22 G24 F24	Input/ Output*	2.5 V CMOS[1]	**I^2C Data Bus:** Data I/O for the I^2C bus interface. **NOTE:** *Dual-mode I/O. Normal operation: Input/ output Boundary Scan Mode: Standard CMOS output

1. This I/O meets the 2.5 V CMOS specification only during boundary scan mode.

Table 8. LED Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
LED_CLK	A19	Output	2.5 V CMOS	**LED Clock:** Clock output for the LED block.
LED_DATA	A20	Output	2.5 V CMOS	**LED Data:** Data output for the LED block.
LED_LATCH	K18	Output	2.5 V CMOS	**LED Latch:** Latch enable for the LED block.

Table 9. JTAG Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
TCK	AA24	Input	2.5 V CMOS	**JTAG Test Clock:** Reference clock for JTAG.
TMS	T16	Input	2.5 V CMOS	**JTAG Test Mode Select:** Selects test mode for JTAG.
TDI	AC18	Input	2.5 V CMOS	**JTAG Test Data Input:** Test data sampled with respect to the rising edge of TCK.
TRST_L	N18	Input	2.5 V CMOS	**JTAG Test Reset:** Reset input for JTAG test.
TDO	Y24	Output	2.5 V CMOS	**JTAG Test Data Output:** Test data driven with respect to the falling edge of TCK.

Table 10. System Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
CLK125	AA5	Input	2.5 V CMOS	**125 MHz Reference Clock:** Input clock to PLL.
CLK50	C21	Input	2.5 V CMOS	**SPI4-2 Reference Clock:** Input clock to SPI4-2 RX PLL. Input range is 40 MHz to 50 MHz. This clock multiplied by eight must equal the required RX SPI4-2 data clock frequency.
SYS_RES_L	Y4	Input	2.5 V CMOS	**System Reset:** System hard reset (active Low).

Table 11. Power Supply Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
AVDD1P8_1	D1 E24	–	–	**1.8 V Analog Power Supply:** 1.8 V supply for analog circuits.
AVDD1P8_2	P7 P18 V6 V11 V14 V18	–	–	**1.8 V Analog Power Supply:** 1.8 V supply for analog circuits.
AVDD2P5_1	Y1	–	–	**2.5 V Analog Power Supply:** 2.5 V supply for analog circuits.
AVDD2P5_2	N3 N22 P3 P22 V10 V15	–	–	**2.5 V Analog Power Supply:** 2.5 V supply for analog circuits.

Table 11. Power Supply Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
VDD	D6 D10 D11 D15 D19 D20 E21 F4 F21 H10 H15 J4 J11 J14 K3 K4 K5 K8 K17 K21 L9 L11 L14 L16 P9 P11 P14 P16 R4 R8 R17 R21 T11 T14 U10 U15 W4 W21 AA6 AA10 AA15 AA19 AB4	–	–	**1.8 V Digital Power Supply:** 1.8 V core supply.
VDD2	B4 B8 B12 B13 B17 B21 D2 D23 F8 F12 F13 F17 H2 H6 H19 H23 J12 J13 M2 M6 M9 M12 M13 M16 M19 M23 N2 N6 N9 N12 N13 N16 N19 N23 T12 T13 U2 U6 U19 U23 W8 W12 W13 W17 AA2 AA23 AC4 AC8 AC12 AC13 AC17 AC21	–	–	**2.5 V Digital Power Supply:** 2.5 V I/O supply.
GND	B6 B10 B15 B19 C4 D4 D5 D8 D12, D13 D17 D21 D22 D24 E1 F2 F6 F10 F15 F19 F23 G10 H4 H8 H12 H13 H17 H21 J10 J15 J21 J23 K2 K6 K9 K11 K14 K16 K19 K20 K23 K24 L3 L6 L10 L12 L13 L15 L24 M3 M4 M8 M11 M14 M17 M18 M21 N4 N8 N11 N14 N17 N21 P1 P10 P12 P13 P15 P21 P23 P24 R1 R2 R3 R6 R9 R10 R11 R14 R16 R19 R23 R24 T7 T8 T9 T10 T15 T17 T18 T19 T21 T23 U4 U7 U8 U12, U13 U16 U17 U21 V2 V3 V13 V16 W2 W3 W5 W6 W7 W10 W15 W19 W20 W23 Y2 Y3 Y8 Y12 Y13 Y15 Y16 Y18 AA1 AA3 AA4 AA7 AA8 AA12 AA13 AA14 AA17 AA21 AB6 AB7 AB10 AB17 AB21 AB23 AC6 AC7 AC10 AC11 AC15 AC19 AC20 AD21	–	–	**Ground:** Ground return for all signals.

Table 12. Unused Balls/Reserved

Signal Name	Ball Designator	Type	Standard	Signal Description
NC	A5 A6 C10 C15 G7 G8 H22 J22 K7 L21 L23 M1 M7 N1 N5 N7 N20 P4 P5 P6 P17 P19 P20 R5 R13 R18 R20 R22 T1 T6 U1 V1 V8 V9 V19 W1 W16 W18 Y7 Y10 Y11 Y14 AA11 AA20 AA22 AB3 AB5 AB8 AB18 AB19 AB20 AB22 AD4 AD5 AD6 AD7 AD8 AD17 AD19 AD20	–	–	No connection.
No Ball	A2 A3 A22 A23 A24 B1 B2 B23 B24 C1 C24 AB1 AB24 AC1 AC2 AC23 AC24 AD1 AD2 AD3 AD22 AD23 AD24	–	–	Balls removed from substrate.
No Pad	A1	–	–	Pad removed from substrate. Use this ball location as a key for device placement onto the PCB.

5.0 Functional Descriptions

5.1 Media Access Controller

5.1.1 General Description

The Intel® IXF1110 main functional block consists of a 1000 Mbps Ethernet Media Access Controller (MAC), supporting the following features:

- 1000 Mbps full-duplex operation
- Independent enable/disable of any port
- Detection of length erroror overly large packets
- RMON statistics and error counters
- Cyclic Redundancy Check (CRC) calculation and error detection
- Programmable options:
  - Filter packets with errors
  - Filter, broadcast, multicast, and unicast address packets
  - Automatically pad transmitted packets less than the minimum frame size
- Compliance with IEEE 802.3x Standard for Flow Control (symmetric pause capability)

The MAC is fully integrated, designed for use with Ethernet 802.3 Frame types, and is compliant with all of the required IEEE 802.3 MAC requirements.

The MAC adds preamble and Start-of-Frame Delimiter (SFD) to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped or sent to the SPI4-2 interface.

5.1.2 MAC Functions

Section 5.1.2.1, “Padding of Undersized Frames on Transmit” on page 43 through Section 5.1.2.3, “Filtering of Receive Packets” on page 44 cover the MAC functions.

5.1.2.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI4-2 interface and automatically padded up to 64 bytes by the MAC. This feature is enabled by setting bit 7 of the “Diverse Config ($ Port_Index + 0x18)” on page 137.

Note: If frames under 64 bytes are sent to the MAC, the padding feature must be enabled for proper operation. A 9-byte packet is the minimum size packet that can be padded up to 64 bytes. Packets under 9 bytes are not padded and are automatically dropped.

5.1.2.2 Automatic CRC Generation

The Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any incoming frame from the SPI4-2 interface. This feature is enabled by setting bit 6 of the "Diverse Config ($ Port_Index + 0x18)" on page 137

Note: When padding of undersized frames on transmit is enabled, the automatic CRC generation must be enabled for proper operation of the IXF1110.

5.1.2.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets via an interaction with the Receive FIFO control.

Note: Jumbo frames (1519 - 9600 bytes) matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, are not dropped. Instead, jumbo frames that are expected to be dropped by the RX FIFO, based on the filter settings in Table 74, "RX Packet Filter Control ($ Port_Index + 0x19)" on page 138, are sent across the SPI4-2 interface as an EOP abort frame. Jumbo frames matching the filter conditions are not counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in the Table 74, "RX Packet Filter Control ($ Port_Index + 0x19)" on page 138 are actually dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.

5.1.2.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Unicast Destination Address that does not match the Station Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all unicast frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

Note: The VLAN filter overrides the unicast filter. Thus, a VLAN frame cannot be filtered based on the unicast address.

5.1.2.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Multicast Destination Address which does not match the Port Multicast Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable register = 1. Otherwise, all multicast frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

5.1.2.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the "RX Packet Filter Control ($ Port_Index + 0x19)" = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all broadcast frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

5.1.2.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the "RX Packet Filter Control ($ Port_Index + 0x19)" = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all VLAN frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

5.1.2.3.5 Filter PAUSE Packets

This feature is enabled when bit 4 of the "RX Packet Filter Control ($ Port_Index + 0x19)" = 0. PAUSE frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the "RX FIFO Errored Frame Drop Enable ($ 0x59F)" = 1. Otherwise, all PAUSE frames are sent to the SPI4-2 interface.

Table 13. Pause Packets Drop Enable Behavior

Pause Frame Pass	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and sent to the switch or Network Processor, regardless of the Frame Drop En setting.
0	1	PAUSE Packets are marked as bad, are dropped in the RX FIFO, and never appear at the SPI4-2 interface.

5.1.2.3.6 Filter CRC Errored Packets

This feature is enabled when bit 5 of the "RX Packet Filter Control ($ Port_Index + 0x19)" = 0. Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI4-2 interface and may be dropped by the switch or system controller (see Table 14, "CRC Errored Packets Drop Enable Behavior" on page 46).

Note: When the CRC Error Pass Filter bit = 0 ("RX Packet Filter Control ($ Port_Index + 0x19)"), it takes precedence over the other filter bits. Any packet (Pause, Unicast, Multicast or Broadcast packet) with a CRC error will be marked as a bad frame when the CRC Error Pass Filter bit = 0.

Table 14. CRC Errored Packets Drop Enable Behavior

CRC Errored PASS	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and are sent to the switch or Network Processor regardless of the Frame Drop En setting.
0	1	CRC errored packets are marked as bad, dropped in the RX FIFO, and never appear at the SPI4-2 interface.

5.1.3 Flow Control

Flow Control is an IEEE 802.3x-defined mechanism for one network node to request that its link partner take a temporary “Pause” in packet transmission. This allows the requesting network node to prevent FIFO overruns and dropped packets, by managing incoming traffic to fit its available memory. The temporary pause allows the device to process packets already received or in transit, thus freeing up the FIFO space allocated to those packets.

The IXF1110 implements the IEEE 802.3x standard RX FIFO threshold-based Flow Control. When appropriately programmed, the MAC can both generate and respond to IEEE standard pause frames. The IXF1110 also supports externally triggered flow control through the Transmit Pause Control interface.

5.1.3.1 802.3x Flow Control (Full-Duplex Operation)

The IEEE 802.3x standard identifies four options related to system flow control:

- No Pause
- Symmetric Pause (both directions)
- Asymmetric Pause (Receive direction only)
- Asymmetric Pause (Transmit direction only)

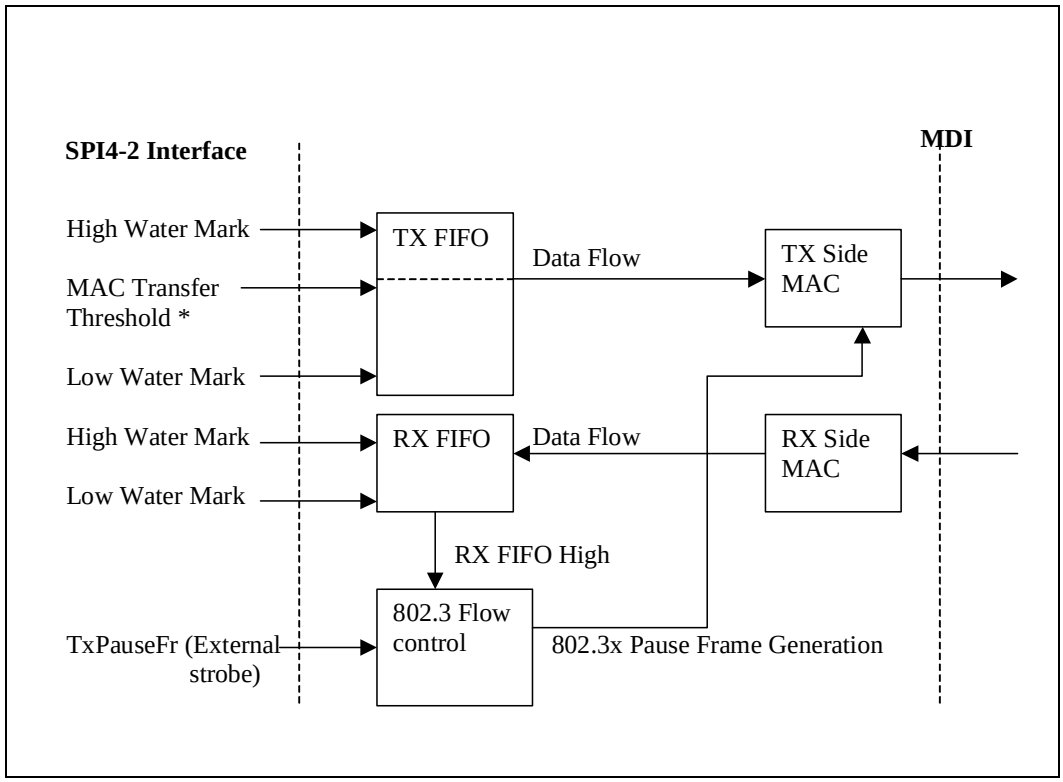
The IXF1110 supports all four options on a per-port basis. Bits 1:0 of the “FC Enable ($ Port_Index + 0x12)” on page 135 provide programmable control for enabling or disabling flow control in each direction independently.

The IEEE 802.3x flow control mechanism is accomplished within the MAC sublayer, and is based on RX FIFO thresholds called watermarks. The RX FIFO level rises and falls as packets are received and processed. When the RX FIFO reaches a watermark (either exceeding a High or dropping below a Low after exceeding a High), the IXF1110 control sublayer signals an internal state machine to transmit a PAUSE frame. The FIFOs automatically generate PAUSE frames (also called control frames) to initiate the following:

- Halt the link partner when the High watermark is reached.
- Restart the link partner when the data stored in the FIFO falls below the Low watermark.

Figure 5 illustrates the IEEE 802.3 FIFO flow control functions.

Figure 5. Packet Buffering FIFO



5.1.3.1.1 Pause Frame Format

PAUSE frames are MAC control frames that are padded to the minimum size (64 bytes). Figure 6 and Figure 7 illustrate the frame format and contents.

Figure 6. Ethernet Frame Format

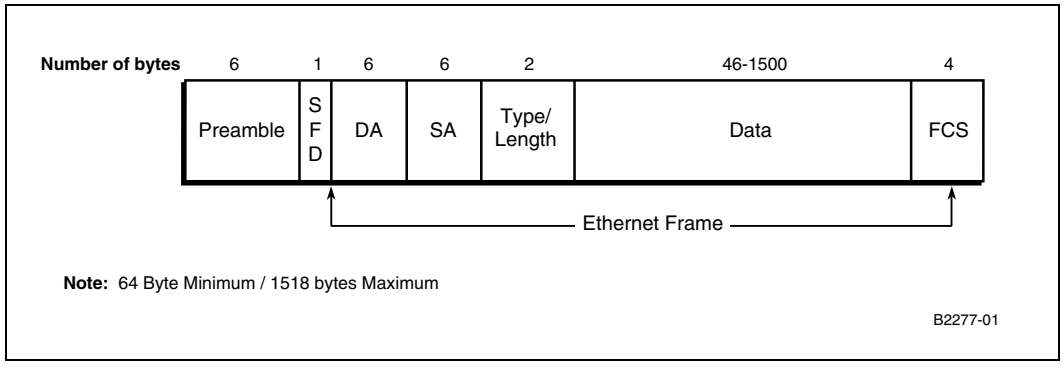
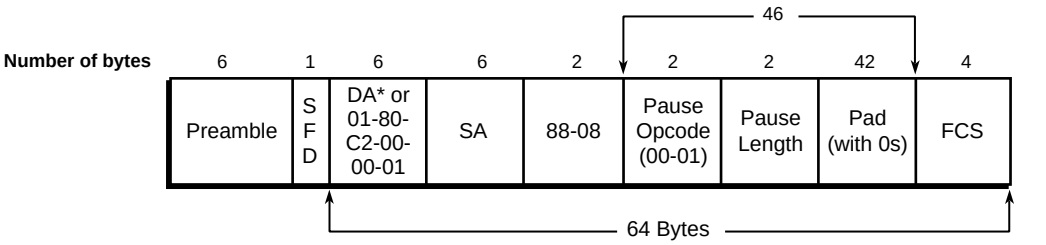


Figure 7. PAUSE Frame Format



Note: In the Intel® IXF1110 architecture, the TX block of the MAC sets this as the pause multicast address. The RX interface of the MAC will process this as the pause multicast or the MAC address.

B3426-01

An IEEE 802.3 MAC PAUSE frame is identified by detecting all of the following:

- OpCode of 00-01
- Length/Type field of 88-08
- DA matching the unique multicast address (01-80-C2-00-00-01)

XOFF. A PAUSE frame informs the link partner to halt transmission for a specified length of time. The PauseLength octets specify the duration of the no-transmit period. If this time is greater than zero, the link partner must stop sending any further packets until this time has elapsed. This is referred to as XOFF.

XON. The MAC continues to transmit PAUSE frames with the specified Pause Length as long as the FIFO level exceeds the threshold. If the FIFO level falls below the threshold before the Pause Length time expires, the MAC sends another PAUSE frame with the Pause Length time specified as zero. This is referred to as XON and informs the link partner to resume normal transmission of packets.

5.1.3.1.2 Pause Settings

The MAC must send PAUSE frames repeatedly to maintain the link partner in a Pause state. The following two inter-related variables control this process:

- Pause Length is the amount of time, measured in multiples of 512 bit times, that the MAC requests the link partner to halt transmission for.
- Pause Threshold is the amount of time, measured in multiples of 512 bit times, prior to the expiration of the Pause Length that the MAC transmits another Pause frame to maintain the link partner in the pause state.

The transmitted Pause Length in the IXF1110 is set by the “FC TX Timer Value ($ Port_Index + 0x07)".

The IXF1110 PAUSE frame transmission interval is set by the “Pause Threshold ($ Port_Index + 0x0E)” on page 134.

5.1.3.1.3 Response to Received PAUSE Command Frames

When Flow Control is enabled in the receive direction (bit 0 in the "FC Enable ($ Port_Index + 0x12)" on page 135), the IXF1110 responds to PAUSE Command frames received from the link partner as follows:

1. The IXF1110 checks the entire frame to verify that it is a valid PAUSE control frame addressed to the Multicast Address 01-80-C2-00-00-01 (as specified in IEEE 802.3, Annex 31B) or has a Destinations Address matching the address programmed in the "Station Address Low ($ Port_Index + 0x00)" through "Station Address High ($ Port_Index + 0x01)".
2. If the PAUSE frame is valid, the transmit side of the IXF1110 pauses for the required number of PAUSE Quanta, as specified in IEEE 802.3, Clause 31.
3. PAUSE does not begin until completion of the frame currently being transmitted.

The IXF1110 response to valid received PAUSE frames is independent of the PAUSE frame filter settings. Refer to Section 5.1.2.3.5, "Filter PAUSE Packets" on page 45 for additional details.

5.1.3.1.4 Transmit Pause Control Interface

The Transmit Pause Control interface allows an external device to trigger the generation of pause frames. The Transmit Pause Control interface is completely asynchronous. It consists of four address signals (TXPAUSEADD[3:0]) and a strobe signal (TXPAUSEFR). The required address for this interface operation is placed on the TXPAUSEADD[3:0] signals and the TXPAUSEFR is pulsed High and returned Low. Refer to Figure 8, "Transmit Pause Control Interface" on page 50 and Table 41, "Transmit Pause Control Interface Parameters" on page 112. Table 15 shows the valid decodes for the TXPAUSEADD[3:0] signals. Figure 8 illustrates the transmit pause control interface.

Note: Flow control must be enabled in the "FC Enable ($ Port_Index + 0x12)" for Transmit Pause Control interface operation.

Note: There are two additional decodes provided that allow the user to generate either an XOFF frame or XON frame from all ports simultaneously.

The default pause quanta for each port is held by the "FC TX Timer Value ($ Port_Index + 0x07)"). The default value of this register is 0x05E after reset is applied.

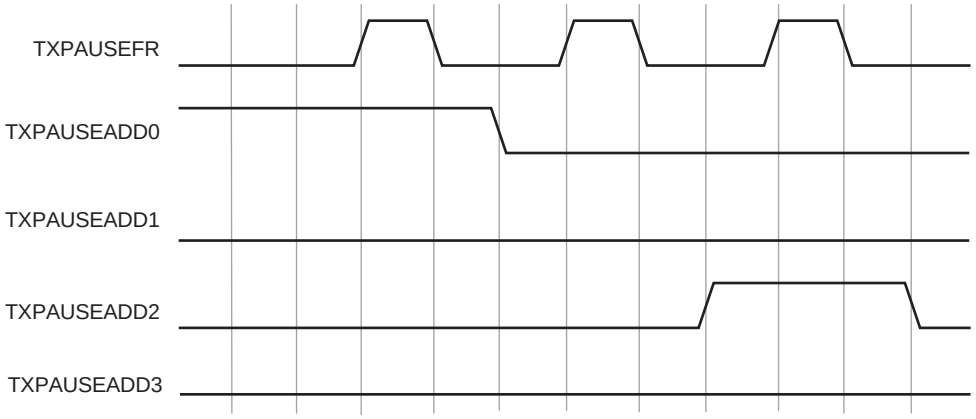
Table 15. Valid Decodes for TXPAUSEADD[3:0]

TXPAUSEADD[3:0]	TX Pause Control Interface Operation
0x0	Transmits a PAUSE frame on every port with a pause_time = ZERO (XON) (Cancels all previous pause commands).
0x1	Transmits a PAUSE frame on port 0 with pause_time equal to the value programmed in the port 0 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x2	Transmits a PAUSE frame on port 1 with pause_time equal to the value programmed in the port 1 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x3	Transmits a PAUSE frame on port 2 with pause_time equal to the value programmed in the port 2 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x4	Transmits a PAUSE frame on port 3 with pause_time equal to the value programmed in the port 3 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x5	Transmits a PAUSE frame on port 4 with pause_time equal to the value programmed in the port 4 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).

Table 15. Valid Decodes for TXPAUSEADD[3:0]

TXPAUSEADD[3:0]	TX Pause Control Interface Operation
0x6	Transmits a PAUSE frame on port 5 with pause_time equal to the value programmed in the port 5 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x7	Transmits a PAUSE frame on port 6 with pause_time equal to the value programmed in the port 6 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x8	Transmits a PAUSE frame on port 7 with pause_time equal to the value programmed in the port 7 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0x9	Transmits a PAUSE frame on port 8 with pause_time equal to the value programmed in the port 8 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0xA	Transmits a PAUSE frame on port 9 with pause_time equal to the value programmed in the port 9 "FC TX Timer Value ($ Port_Index + 0x07)" (XOFF).
0xB - 0XE	Reserved
0xF	Transmits a PAUSE frame on every port with pause_time equal to the value programmed in the "FC TX Timer Value ($ Port_Index + 0x07)" for each port (XOFF).

Figure 8. Transmit Pause Control Interface



This example shows the following conditions:

Strobe 1:
- Port 0: Transmit Pause Packet (XOFF)

Strobe 2:
- All Ports: Transmit Pause Packet with pause_time = 0 (XON)

Strobe 3:
- Port 3: Transmit Pause Packet (XOFF)

B3366-01

5.1.4 Fiber Operation

The data path in the MAC is an internal 10-bit interface, as described in the IEEE 802.3z Standard. It is connected directly to an internal SerDes block for Serialization/Deserialization and transmission/reception on the fiber medium to/from the link partner.

Note: The MAC contains all the PCS (8B/10B encoding and 10B/8B decoding) required to encode and decode the data. The MAC also supports auto-negotiation per the IEEE 802.3z Standard via access to the "TX Config Word ($ Port_Index + 0x17)" on page 136, "RX Config Word ($ Port_Index + 0x16)" on page 135, and Diverse Config Registers (see "Diverse Config ($ Port_Index + 0x18)" on page 137.

By default, IXF1110 auto-negotiation is disabled by Register bit 5 (AN_enable) of the "Diverse Config ($ Port_Index + 0x18)". When auto-negotiation is disabled, the IXF1110 can operate in forced mode, which is 1000 Mbps full duplex only. This is equivalent to entering the state AN_DISABLE_LINK_OK as described in Figure 37-6 of IEEE 802.3. The IXF1110 can pass packets when auto-negotiation is disabled only when the internal Synchronization State Machine indicates that the sync_status is OK as described in Figure 36-9 of IEEE 802.3.

Note: Packet IPG must contain a minimum of three consecutive /I1/ or /I2/ ordered sets per IEEE 802.3 for correct operation.

Note: The IXF1110 treats the K28.1 code word as an unknown control word; therefore, it should not be used.

5.1.5 Auto-Negotiation

Auto-negotiation is carried out by an internal state machine within the MAC in the IXF1110. The IXF1110 is fully IEEE 802.3z standard compliant.

The following three registers are involved in this auto-negotiation process: RX Config Word TX Config Word, and Diverse Config:

- The "RX Config Word ($ Port_Index + 0x16)" performs the operation of auto-negotiation base page ability.
- The "TX Config Word ($ Port_Index + 0x17)" performs the operation of auto-negotiation advertisement.
- The "Diverse Config ($ Port_Index + 0x18)" enables auto-negotiation.

The "TX Config Word ($ Port_Index + 0x17)" must be written to program the modes advertised. The "Diverse Config ($ Port_Index + 0x18)" bit 5 (AN_enable) must be written to enable auto-negotiation. The "RX Config Word ($ Port_Index + 0x16)" bit 21 (AN_complete) must be polled to determine when auto-negotiation is complete. The following MAC registers must be programmed to match the results upon completion:

- Link LED: Table 80, "Link LED Enable ($ 0x502)" on page 149
- Flow Control: If the link partner does not support flow control, the "FC Enable ($ Port_Index + 0x12)" on page 135 must be updated to reflect this change.

Note: In auto-negotiation mode, the TX SPI4-2 status bus (TSTAT[1:0]) is held in the SATISFIED state until auto-negotiation completes and a valid link is established. This prevents the TX FIFO from being filled prior to transmission of packets.

5.1.5.1 Determining If Link Is Established in Auto-Negotiation Mode

A valid link is established when the (AN_complete) bit is set and the RX_Sync bit reports synchronization has occurred. Both register bits are located in the "RX Config Word ($ Port_Index + 0x16)".

If the link goes down after auto-negotiation is completed, RX_Sync indicates that a loss of synchronization occurred. The IXF1110 restarts auto-negotiation and attempts to re-establish a link. Once a link has been re-established, the AN_complete bit is set and the RX_sync bit shows that synchronization has occurred.

To manually restart auto-negotiation, bit 5 of the "Diverse Config ($ Port_Index + 0x18)" (AN_enable) must be de-asserted, then re-asserted.

5.1.6 Forced Mode Operation

The fiber operation of the MAC can be forced to operated at 1000 Mbps, full duplex without completion of the auto negotiation function. In this mode, the receive path of the MAC must achieve synchronization with the link partner. Once this has been achieved, the transmit path of the MAC will be enabled to allow data transmission, which is known as "forced mode" operation. Forced mode is limited to operation with a link partner that operates with a full-duplex link at a speed of 1000 Mbps.

Forced mode is enabled by Register bit 5 (AN_enable) in the "Diverse Config ($ Port_Index + 0x18)". By default, the IXF1110 is set to forced mode operation.

Note: In forced mode, the TX SPI4-2 status bus (TSTAT[1:0]) is held in the SATISFIED state until sync_status is OK. This prevents the TX FIFO from being filled prior to transmission of packets.

5.1.6.1 Determining If Link Is Established in Forced Mode

When the IXF1110 is in forced mode operation, the "RX Config Word ($ Port_Index + 0x16)" bit 20 RX Sync indicates when synchronization has occurred and valid link is established.

Note: The Rx Sync bit indicates a loss of synchronization when the link is down.

5.1.7 Jumbo Packet Support

The IXF1110 supports the concept of jumbo frames. The jumbo frame length is dependent on the application, and the IXF1110 design has been optimized for 9.6 KB jumbo frame length. Lengths larger than this can be programmed, but will limit system performance.

The value programmed into the Max Frame Size Register (Addr: Port_Index + 0x0F) determines the maximum length frame size the MAC can receive or transmit without activating any error counters, and without truncation.

The Max Frame Size Register (Addr: Port_Index + 0x0F) bits 13:0 set the frame length. The default value programmed into this register is 0x05EE (1518). The value is internally adjusted by +4 if the frame has a VLAN tag. The overall programmable maximum is 0x3FFF or 16383 bytes. The register should be programmed to 0x2667 for the 9.6 KB length jumbo frame for which the IXF1110 is optimized.

The RMON counters are also affected for jumbo frame support as follows:

RX Statistics:

- RXOctetsTotalOK (Addr: Port_Index + 0x20)
- RXPkts1519toMaxOctets (Addr: Port_Index + 0x2B)

- RXFCSErrors (Addr: Port_Index + 0x2C)
- RXDataError (Addr: Port_Index + 0x02E)
- RXAlignErrors (Addr: Port_Index + 0x2F)
- RXLongErrors (Addr: Port_Index + 0x30)
- RXJabberErrors (Addr: Port_Index + 0x31)
- RXVeryLongErrors (Addr: Port_Index + 0x34)

TX Statistics:

- TXOctetsTotalOK (Addr: Port_Index + 0x40)
- TxPkts1519toMaxOctets (Addr: Port_Index + 0x4B)
- TxExcessiveLengthDrop (Addr: Port_Index + 0x53)
- TXCRCError (Addr: Port_Index + 0x56)

The IXF1110 checks the CRC for all legal length jumbo frames (frames between 1519 and the Max Frame Size). On transmission, the MAC can be programmed to append the CRC to the frame or check the CRC and increment the appropriate counter. On reception, the MAC transmits these frames across the SPI4-2 interface (jumbo frames with a bad CRC cannot be dropped and are sent across the SPI4-2 interface). If the receive frame has a bad CRC, the appropriate counter is incremented and the EOP Abort code is set in the SPI4-2 control word.

Jumbo frames also impact flow control. The maximum frame size needs to be taken into account when determining the FIFO watermarks. The current transmission must be completed before a Pause frame can be transmitted (needed when the receiver FIFO high watermark has been exceeded). If the current transmission is a jumbo frame, the delay may be significant and increase data loss due to insufficient available FIFO space.

5.1.8 RMON Statistics Support

5.1.8.1 RMON Statistics

The IXF1110 supplies RMON statistics via the CPU interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the IXF1110 memory map. Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1110.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Intel switch and router products. This implementation allows the IXF1110 to provide all of the RMON Statistics group as defined by RFC2819.

The IXF1110 supports the RMON RFC2819 Group 1 statistics counters. Table 16 notes the differences and additional statistics registers supported by the IXF1110 that are outside the scope of the RMON RFC2819 document.

Table 16. RMON Additional Statistics Registers (Sheet 1 of 2)

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1110 Equivalent Statistics	Type	Definition of RMON Versus IXF1110 Documentation
etherStatsIndex	Integer32	N/A	N/A	N/A
etherStatsDataSource	Object Identifier	N/A	N/A	N/A
etherStatsDropEvents	Counter32	RX/TX FIFO Number of Frames Removed	Counter32	See Table note 1.
etherStatsOctets	Counter32	RXOctetsTotalOK RXOctetsBad TXOctetsTotalOK TXOctetsBad	Counter32	**Note:** The IXF1110 has two counters for RX and TX that use different naming conventions for total Octets and Octets bad. These counters need to be combined to meet the RMON spec.
etherStatsPkts	Counter32	RX/TXUCPkts RX/TXBCPkts RX/TXMCPkts	Counter32	**Note:** The IXF1110 has three counters for etherStatsPkts that need to be combined to give the total packets as defined by the RMON spec.
etherStatsBroadcastPkts	Counter32	RX/TXBCPkts	Counter32	OK
etherStatsMulticastPkts	Counter32	RX/TXMCPkts	Counter32	See table note 2.
etherStatsCRCAlignErrors	Counter32	RXAlignErrors RXFCSErrors TXCRCError	Counter32	**Note:** The IXF1110 has two counters for alignment and CRC errors for the RX side only. The IXF1110 has CRCError for the TX side.
etherStatsOversizePkts	Counter32	RXLongErrors TXExcessiveLengthDrop	Counter32	OK
etherStatsJabbers	Counter32	RXJabberErrors	Counter32	OK

1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1110 supports this and will increment when either an RX or TX FIFO has over flowed. If any IXF1110 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.
2. The IXF1110 has an extra counter RX/TXUCPkts that can be used.
3. The IXF1110 has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.

Table 16. RMON Additional Statistics Registers (Sheet 2 of 2)

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1110 Equivalent Statistics	Type	Definition of RMON Versus IXF1110 Documentation
etherStatsCollisions	Counter32	TXSingleCollisions TXMultipleCollisions TXLateCollisions TXTotalCollisions	Counter32	OK **Note:** Registers exist on the TX side but should not increment since the IXF1110 only supports full-duplex.
etherStatsPkts64Octets	Counter32	RX/TXPkts64Octets	Counter32	OK
etherStatsPkts65to127Octets	Counter32	RX/TXPkts65to127Octets	Counter32	OK
etherStatsPkts128to255Octets	Counter32	RX/TXPkts128to255Octets	Counter32	OK
etherStatsPkts256to511Octets	Counter32	RX/TXPkts256to511Octets	Counter32	OK
etherStatsPkts512to1023Octets	Counter32	RX/TXPkts512to1023Octets	Counter32	OK
etherStatsPkts1024to1518Octets	Counter32	RX/TXPkts1024to1518Octets	Counter32	See table note 3.
etherStatsOwner	Owner String	N/A	N/A	N/A
etherStatsStatus	Entry Status	N/A	N/A	N/A

1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1110 supports this and will increment when either an RX or TX FIFO has over flowed. If any IXF1110 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.
2. The IXF1110 has an extra counter RX/TXUCPkts that can be used.
3. The IXF1110 has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.

5.1.8.2 Conventions

The following conventions are used throughout the RMON MIB and its companion documents.

- **Good Packets**: Error-free packets that have a valid frame length. For example, on Ethernet, good packets are error-free packets that are between 64 octets long and 1518 octets long. They follow the form defined in IEEE 802.3, Section 3.2.
- **Bad Packets**: Packets that have proper framing and are therefore recognized as packets, but contain errors within the packet or have an invalid length. For example, on Ethernet, bad packets have a valid preamble and SFD, but have a bad CRC, or are either shorter than 64 octets or longer than 1518 octets.

5.1.8.3 Additional Statistics

The following additional IXF1110 registers support features not documented in RMON:

- MAC (flow) control frames
- VLAN tagged frames

- Sequence errors
- Symbol errors
- CRC errors

These additional counters allow for additional differentiation over and above standard RMON probes.

Note: A packet transfer with an invalid 10-bit symbol will not always update the statistics registers correctly.

- **Behavior:** The IXF1110 8B10B decoder substitutes a valid code word octet in its place. The packet transfer is aborted and marked as bad. The new internal length of the packet is equal to the byte position where the invalid symbol was. No packet fragments are seen at the next packet transfer.
- **Issue:** If the invalid 10-bit code is inserted in a byte position of 64 or greater, expected RX statistics are reported. However, if the invalid code is inserted in a byte position of less than 64, expected RX statistics are not stored.

5.2 System Packet Interface Level 4 Phase 2

The System Packet Interface Level 4 Phase 2 (SPI4-2) provides a high-speed connection to a network processor or an ASIC. The interface implemented on the IXF1110 operates at data rates up to 12.8 Gbps and supports up to ten 1 Gbps MAC ports. The data path is 16 lanes wide in each direction, with each lane operating from 640 Mbps up to 800 Mbps. Port addressing, start/end packet control, and error control codes are all transferred “in-band” on the data bus. In-band addressing supports up to 10 ports. Separate transmit and receive FIFO status lines are used for flow control. By keeping the FIFO status information out-of-band, the transmit and receive interfaces may be de-coupled to operate independently. Figure 9 and Table 17 provide an overview of the IXF1110 SPI4-2 interface.

Figure 9. SPI4-2 Interfacing with the Network Processor or Forwarding Engine

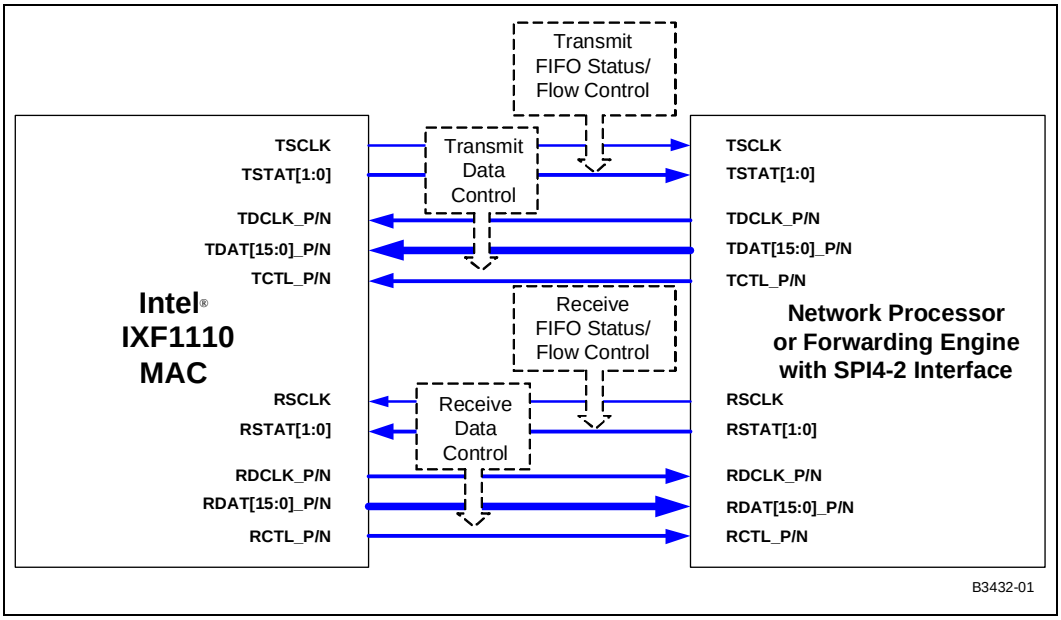


Table 17. SPI4-2 Interface Signal Summary (Sheet 1 of 2)

Signal Name	Signal Description
Transmit	
TDAT[15:0]_P/N	**Transmit Data Bus:** Differential LVDS lines used to carry payload data and in-band control words. Internally terminated differentially with 100 Ω.
TDCLK_P/N	**Transmit Data Clock:** Differential LVDS clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω. **NOTE:** If TDCLK is applied to the IXF1110 after the device has come out of reset, the system designer must ensure the TDCLK is stable when applied. Failure to due so can result in the IXF1110 training on a non-stable clock, causing DIP4 errors and data corruption.
TCTL_P/N	**Transmit Control:** Differential LVDS lines used to indicate when a control word is being transmitted. A High level indicates a control word present on TDAT[15:0]. Internally terminated differentially with 100 Ω.

Table 17. SPI4-2 Interface Signal Summary (Sheet 2 of 2)

Signal Name	Signal Description
TSCLK	**Transmit Status Clock:** LVTTL clock associated with TSTAT [1:0]. Frequency is equal to one-quarter TDCLK.
TSTAT1, TSTAT0	**Transmit FIFO Status:** LVTTL lines used to carry round-robin FIFO status information, along with associated error detection and framing.
Receive	
RDAT[15:0]_P/N	**Receive Data:** Carries payload data and in-band control from the IXF1110 link-layer device. Internally terminated differentially with 100 Ω
RDCLK_P/N	**Receive Data Clock:** Differential LVDS clock associated with RDAT[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω
RCTL_P/N	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low. Internally terminated differentially with 100 Ω
RSCLK	**Receive Status Clock:** LVTTL clock associated with RSTAT[1:0].
RSTAT1, RSTAT0	**Receive FIFO Status:** LVTTL lines used to carry round-robin FIFO status information, along with associated error detection and framing.

5.2.1 Data Path

Transfer of complete packets or shorter bursts is controlled by the programmed MaxBurst1 or MaxBurst2 in conjunction with the FIFO status bus. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted between burst transfers only. Once a transfer begins, data words are sent uninterrupted until an end-of-packet, or until a multiple of 16 bytes is reached as programmed in MaxBurst1 and MaxBurst2. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and/or training patterns.

Note: The system designer should be aware that the MAC Transfer Threshold Register must be set to a value which exceeds the MaxBurst1 setting of the network processor or ASIC. Otherwise, a TX FIFO under-run may result.

The minimum and maximum supported packet lengths are determined by the application. Because the IXF1110 is targeted at the Ethernet environment, the minimum frame size is 64 bytes and the maximum frame size is 1522 bytes for VLAN packets (1518 bytes for non-VLAN packets). For larger frames, adjust the value of the “Max Frame Size ($ Port_Index + 0x0F)” on page 134. For ease of implementation, successive start-of-packets must occur not less than eight cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

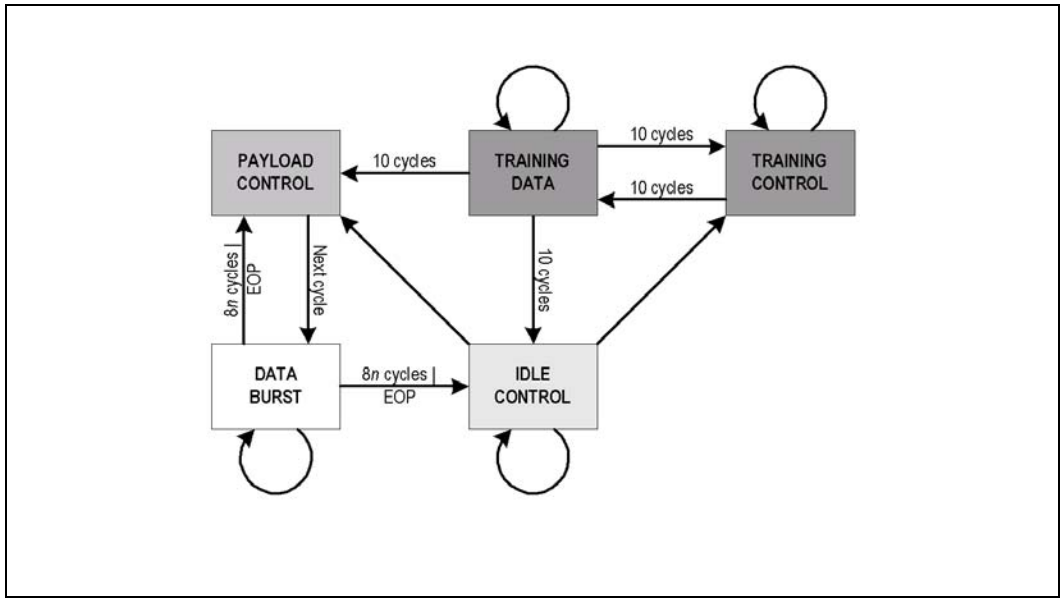
Note: Data packets with frame lengths less than 64 bytes should not be transferred to the IXF1110 unless packet padding is enabled. If this rule is disregarded, unwanted fragments may be generated on the network at the SerDes interface.

Figure 10 on page 59 shows cycle-by-cycle behavior of the data path for valid state transitions. The states correspond to the type of words transferred on the data path. Transitions from the “Data Burst” state (to “Payload Control” or “Idle Control”) are possible only on the integer multiples of

eight cycles (corresponding to multiples of 16-byte segmentations) or upon end-of-packet. A data burst must immediately follow a payload control word on the next cycle. Arcs not annotated correspond to single cycles.

In the IXF1110, the RX FIFO Status channel operates in a “pessimistic mode.” It is termed as pessimistic because it has the longest latency and largest impact on usable bandwidth. However, as a DIP-2 check error is a rare event, there will be no ‘real world’ effect on bandwidth utilization and no possibility of data loss. For example, if there is a DIP-2 check error found, all previously granted credits are cancelled and the internal status for each port is set to SATISFIED. Any current data burst in transmission is completed. No new credits are granted until a complete FIFO status cycle has been received and validated by a correct DIP-2 check. This is the only method of operation that can eliminate the possibility of an overrun in the link partner device.

Figure 10. Data Path State



5.2.1.1 Control Words

A common control word format is used in both the transmit and receive interfaces. Table 18 describes the fields in the control word. When inserted in the data path, the control word is aligned such that its MSB is sent on the MSB of the transmit or receive data lines. A payload control word that separates two adjacent burst transfers contains status information pertaining to the previous transfer and the following transfer. Table 19 provides a list of control-word definitions.

Table 18. Control Word Format

Bit Position	Label	Description
15	Type	**Control Word Type.** Set to either of the following values: 0 = Idle or training control word 1 = Payload control word (payload transfer will immediately follow the control word)
14:13	EOPS	**End-of-Packet (EOP) Status.** Set to the following values according to the status of the immediately preceding payload transfer: 00 = Not an EOP. 01 = EOP Abort (application-specific error condition 10 = EOP Normal termination, 2 bytes valid 11 = EOP Normal termination, 1 byte valid EOPS is valid in the first control word following a burst transfer. It is ignored and set to “00” otherwise.
12	SOP	**Start-of-Packet.** Set to 1 if the payload transfer immediately following the control word corresponds to the start of a packet. Set to 0 otherwise. Set to 0 in all idle and training control words
11:4	ADR	**Port Address.** 8-bit port address of the payload data transfer immediately following the control word. None of the addresses are reserved (all are available for payload transfer). Set to all zeroes in all idle control words Set to all ones in all training control words
3:0	DIP-4	**4-bit Diagonal Interleaved Parity.** 4-bit odd parity computed over the current control word and the immediately preceding data words (if any) following the last control word

Table 19. Control Word Definitions (Sheet 1 of 2)

	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
0	0000	Idle	Continued	Idle, not EOP, training control word
1	0001	Reserved	Reserved	Reserved
2	0010	Idle	EOP w/abort	Idle, Abort last packet
3	0011	Reserved	Reserved	Reserved
4	0100	Idle	EOP w/ 2 bytes	Idle, EOP with 2 bytes valid
5	0101	Reserved	Reserved	Reserved
6	0110	Idle	EOP w/ 1 byte	Idle, EOP with 1byte valid
7	0111	Reserved	Reserved	Reserved
8	1000	Valid	None	Valid, no SOP, no EOP
9	1001	Valid/SOP	None	Valid, SOP, no EOP
A	1010	Valid	EOP w/abort	Valid, no SOP, abort
B	1011	Valid/SOP	EOP w/abort	Valid, SOP, abort
C	1100	Valid	EOP w/ 2 bytes	Valid, no SOP, EOP with 2 bytes valid

Table 19. Control Word Definitions (Sheet 2 of 2)

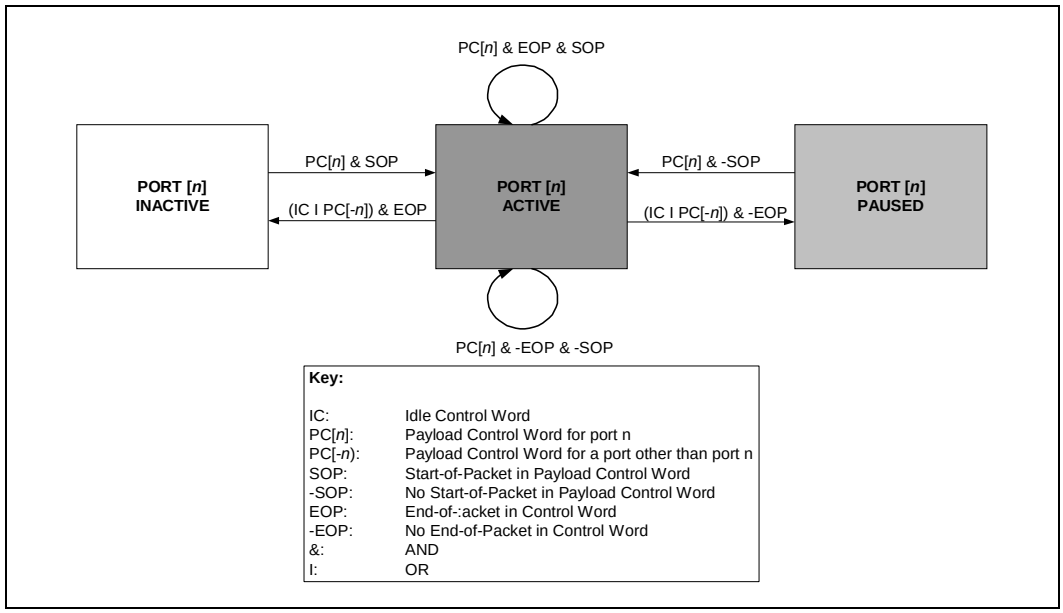
	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
D	1101	Valid	EOP w/ 2 bytes	Valid, SOP, EOP with 2 bytes valid
E	1110	Valid	EOP w/ 1 byte	Valid, no SOP, EOP with 1byte valid
F	1111	Valid	EOP w/ 1 byte	Valid, SOP, EOP with 1byte valid

The SPI4-2 specification details all available Payload Control Words and should be used to reference the specific meaning of each. The IXF1110 supports all required functions per this specification. However, there are various specifics in the way certain Control Words affect the balance of the IXF1110 operation, such as how the device deals with EOP Aborts.

The SPI4-2 specification allows the EOP Abort Payload Control word, which signals that the data associated with a particular frame is errored and should be dropped, or errored and dropped by the far-end link partner. In the IXF1110, all TX SPI4-2 transfers that end with an EOP Abort code have the TX SerDes CRC corrupted. This is true regardless of the MAC configuration.

Figure 11 shows per-port state transitions at control-word boundaries. At any given time, a port may be active (sending data), paused (not sending data but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

Figure 11. Per-Port State Diagram with Transitions at Control Words



5.2.1.2 EOP Abort

EOP Aborts is an End-of-Packet (EOP) termination that is sent out of the IXF1110 SPI4-2 to tell the upstream SPI4-2 device that a packet is bad. EOP Abort packets are sent by the IXF1110 under the following conditions:

- Standard size (64-1518 byte) packets that are filtered ("RX Packet Filter Control ($ Port_Index + 0x19)") but not dropped due to the setting in the "RX FIFO Errored Frame Drop Enable ($ 0x59F)" (see Section 5.1.2.3, "Filtering of Receive Packets" on page 44).
- Standard size (64-1518 byte) packets that are greater in size than the setting in the "Max Frame Size ($ Port_Index + 0x0F)" and are not dropped due to the setting in the "RX FIFO Errored Frame Drop Enable ($ 0x59F)".
- Jumbo frames that meet the filter conditions set in the "RX Packet Filter Control ($ Port_Index + 0x19)" on page 138 or are above the "Max Frame Size ($ Port_Index + 0x0F)" on page 134.
- RX FIFO overflows.
- Packets received with /V/ error codes on the SerDes interface that are not dropped due to settings in the "RX FIFO Errored Frame Drop Enable ($ 0x59F)" on page 159.
- Runt Packets (under 64 bytes) received that are not dropped due to the setting in the "RX FIFO Errored Frame Drop Enable ($ 0x59F)" on page 159.

Note: EOP Abort packets sent out on the RX SPI4-2 may have the packet size modified. When an EOP abort packet is received on the TX SPI4-2, the IXF1110 sends the packet out to the SerDes interface with an invalid CRC and is recorded in the TX statistics as a CRC error.

5.2.1.3 DIP4

Figure 12 shows the range over which the Diagonal Interleaved Parity (DIP-4) parity bits are computed. A functional description of calculating the DIP-4 code is given as follows. Assume that the stream of 16-bit data words are arranged as shown in Figure 13 (MSB at the left most column, time moving downward). (The first word received is at the top of the figure; the last word is at the bottom of the figure.) The parity bits are generated by summing diagonally (in the control word, the space occupied by the DIP-4 code (bits a, b, c, d) is set to all 1s during encoding). The first 16-bit result is split into two bytes, which are added to each other modulo-2 to produce an 8-bit result. The 8-bit result is then divided into two 4-bit nibbles, which are added to each other modulo-2 to produce the final DIP-4 code. The procedure described applies to either parity generation on the Rx path or to check parity on the Tx path.

Figure 12. DIP-4 Calculation Boundaries

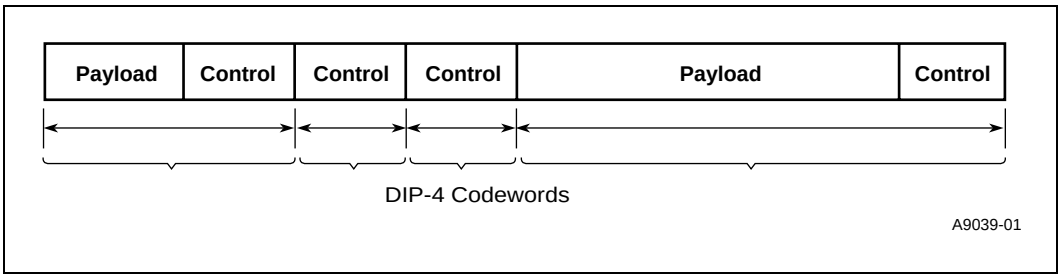
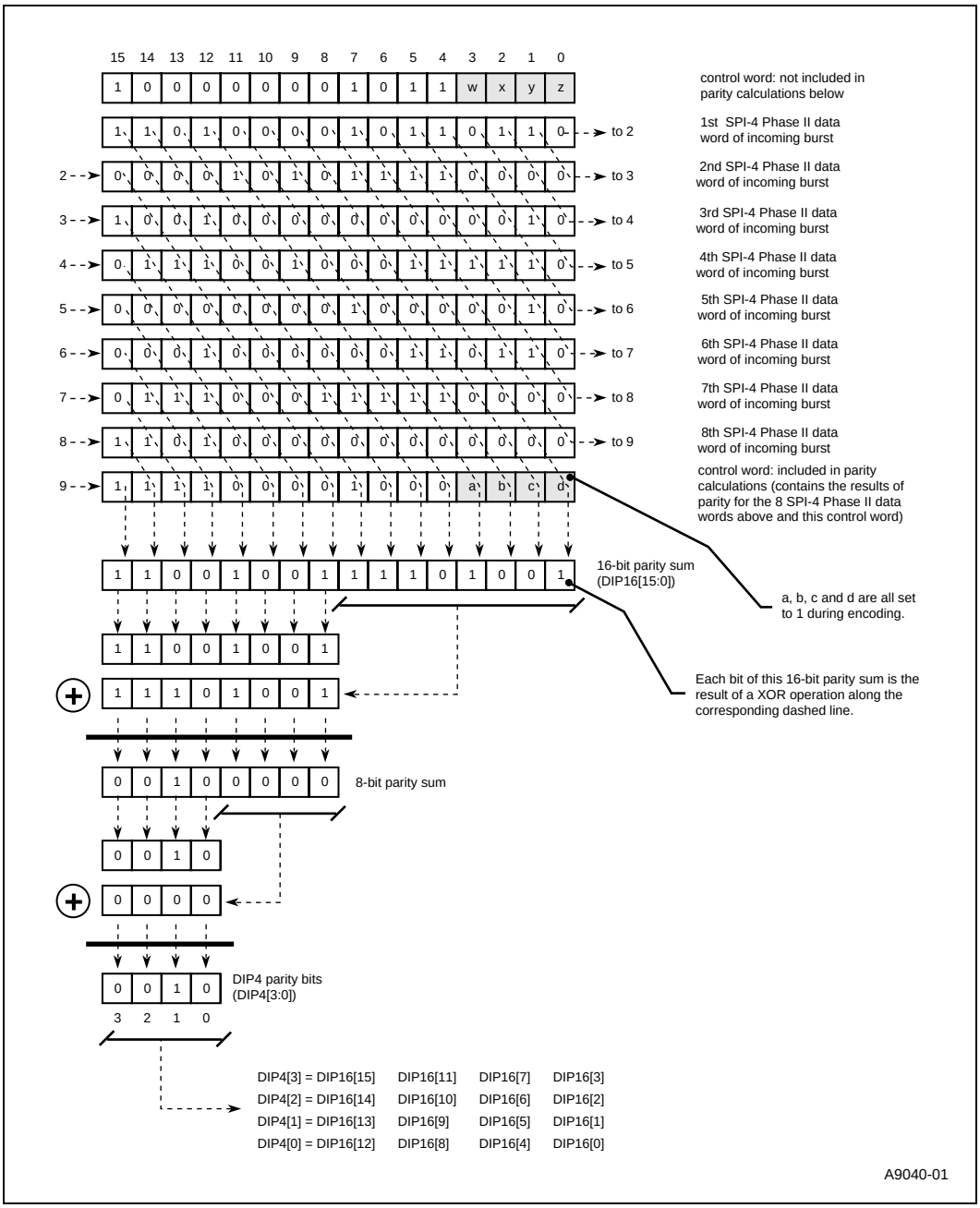


Figure 13. DIP-4 Calculation Algorithm



5.2.2 Start-Up Parameters

5.2.2.1 CALENDAR_LEN

CALENDAR_LEN specifies the length of each calendar sequence. As the IXF1110 is a 10-port device, CALENDAR_LEN is fixed at 10 for both TX and RX data paths.

5.2.2.2 CALENDAR_M

CALENDAR_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence.

In the IXF1110, the TX path CALENDAR_M is fixed at 1; thus, the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence.

In the IXF1110, the RX path CALENDAR_M is also fixed at 1. Thus, the status for port 0-9 must only be sent once between framing and DIP2.

Therefore, the value of both Tx and RX CALENDAR_M parameters is always fixed a 1.

5.2.2.3 DIP2_Thr

DIP2_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and therefore terminate sending training sequences. In Table 103, “SPI4-2 RX Calendar ($ 0x702)” on page 173, bits 19 to 16 specify this parameter. The default value for DIP2_Thr is 1.

5.2.2.4 Loss_Of_Sync

Loss_of_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and therefore restart training sequences. Table 103, “SPI4-2 RX Calendar ($ 0x702)” on page 173, bits 11 to 8 specify this parameter. The default value for Loss_Of_Sync is three.

5.2.2.5 DATA_MAX_T

DATA_MAX_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. In Table 102, “SPI4-2 RX Training ($ 0x701)” on page 172, bits 15 to 0 specify this parameter. The default value for DATA_MAX_T is 0x0000, which disables periodic training sequence transmission.

5.2.2.6 REP_T

REP_T is an RX SPI4-2 parameter specifying the number of repetitions of the training sequence to be scheduled every DATA_MAX_T interval. In Table 102, “SPI4-2 RX Training ($ 0x701)” on page 172, bits 23 to 16 specify this parameter. The default value for REP_T is 0x00.

5.2.2.7 DIP4_UnLock

DIP4_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected in order to declare loss of synchronization and drive TSTAT[1:0] bus with framing. In Table 104, “SPI4-2 TX Synchronization ($ 0x703)” on page 174, bits 15 to 8 specify this parameter. The default value for DIP4_UnLock is 0x4.

5.2.2.8 DIP4_Lock

DIP4_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected in order to declare synchronization achieved and enable the calendar sequence. In

Table 104, “SPI4-2 TX Synchronization ($ 0x703)” on page 174, bits 7 to 0 specify this parameter. The default value for DIP4_Lock is 0x20.

5.2.2.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “starving”. Bits 24 to 16 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes [see Table 101, “SPI4-2 RX Burst Size ($ 0x700)” on page 172].

5.2.2.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “hungry”. Bits 8 to 0 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst2 of 32 bytes (see Table 101, “SPI4-2 RX Burst Size ($ 0x700)” on page 172).

5.2.3 Dynamic Phase Alignment Training Sequence (Data Path De-skew)

5.2.3.1 Training at Start-up

The SPI4-2 Specification states that on power-up or after a reset, the training sequence (as defined in the SPI4-2 Specification) is sent indefinitely by the source side until it receives valid FIFO status on the FIFO bus. The specification also states that it is possible for the bus de-skew to be completed after one training sequence takes place. It is unlikely that the bus can be de-skewed in a single training sequence because of the presence of both random and deterministic jitter. The only way to account for the random element is to determine an average over repeated training sequences. Since the required number of repeats is dependent on several characteristics of the system in which the IXF1110 is being used, power on training (or training following loss of synchronization) will continue until synchronization is achieved and the calendar is provisioned. The length of power on training will not be a fixed number of repeats.

The number of training sequence repeats could be fairly large (16, 32, or 64). If this is necessary every time training is required, a significant use of interface bandwidth is needed just to train and de-skew the data path. This is only done at power-up or reset for an optimal starting point interface. After this, periodic training provides a better adjustment and a substantially lower bandwidth overhead.

5.2.3.2 Periodic Training

A scheduled training sequence is sent at least once every pre-configured bounded interval (DATA_MAX_T) on both the transmit and receive paths. These training sequences are used by the receiving end of each interface for de-skewing bit arrival times on the data and control lines. The sequence allows the receiving end to correct for relative skew difference of up to +/- 1 bit time. The training sequence consists of one (1) idle control word followed by one or more repetitions of a 20-word training pattern consisting of 10 (repeated) training-control words followed by 10 (repeated) training-data words.

The initial idle control word removes dependencies of the DIP-4 in the training control words from preceding data words. Assuming a maximum of +/- bit time alignment jitter on each line, and a maximum of +/- bit time relative skew between lines, there are at least eight bit times when a receiver can detect a training control word prior to de-skew. The training data word is chosen to be orthogonal to the training control word. In the absence of bit errors in the training pattern, a receiver should be able successfully to de-skew the data and control lines with one training pattern. The sending side of the data path on both the transmit and receive interfaces must schedule the training sequence at least once every DATA_MAX_T cycles.

Note: DATA_MAX_T may be set to zero, disabling periodic training on the interface (refer to Table 102, "SPI4-2 RX Training ($ 0x701)" on page 172). This is done when a system shows very little drift during normal operation, and no fine-grain correction on an on-going basis is needed. This allows the maximum possible bandwidth for data transfer. The transmit and receive interface training sequences are scheduled independently.

5.2.3.3 Training in a Practical Implementation

The OIF Standard states that it should be possible to train and de-skew the data input in a single training cycle. However, from the research carried out and the variances in jitter and skew due to board layout and clock tolerance issues, some sort of averaging over several repeated training patterns is required to reliably determine the optimal point at which to capture the incoming data. This is true for both static alignment and dynamic phase alignment. Therefore, several training patterns are required for an average. The more training patterns, the more accurate the average.

The de-skew circuit in the IXF1110 uses dynamic phase alignment with a typical averaging requirement of 32 training patterns required to deliver a reliable result. During power-on training, an unlimited number of training cycles is sent by the data sourcing device. (The standard states that training must be sourced until a calendar has been provisioned.) In the IXF1110, the de-skew circuit waits until completion of its programmed average over the training patterns, ensuring that the required number of good DIP-4s is seen. Only then is a calendar provisioned.

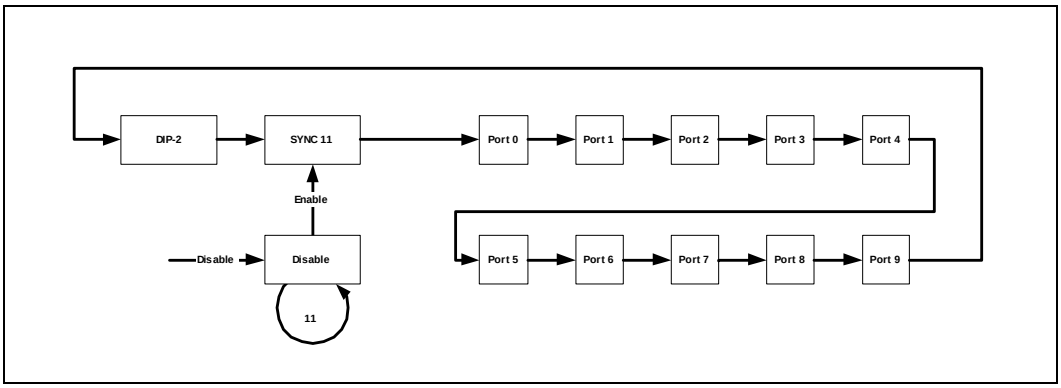
During periodic training, it is important to ensure that the training result is no less accurate than that already used for the initial decision during power-on training. Thus, a similar number of training cycles must be averaged over (32). This could make the overhead associated with periodic training large if it is required to be carried out too often. We therefore recommend that periodic training be scheduled infrequently (DATA_MAX_T = a large number) and that the number of repetitions of training be = 32(α).

5.2.4 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the IXF1110 to the upper layer processor device, and over the RSTAT link from the upper layer processor to the IXF1110. The status channels operate independently.

Figure 14 shows the operation of the FIFO status channel. The sending side of the FIFO status channel is initially in the DISABLE state and sends the "1 1" pattern repeatedly. When FIFO status transmission is enabled, there is a transition to the SYNC state and the "1 1" framing pattern is sent. FIFO status words are then sent according to the calendar sequence, repeating the sequence CALENDAR_M times, followed by the DIP-2 code.

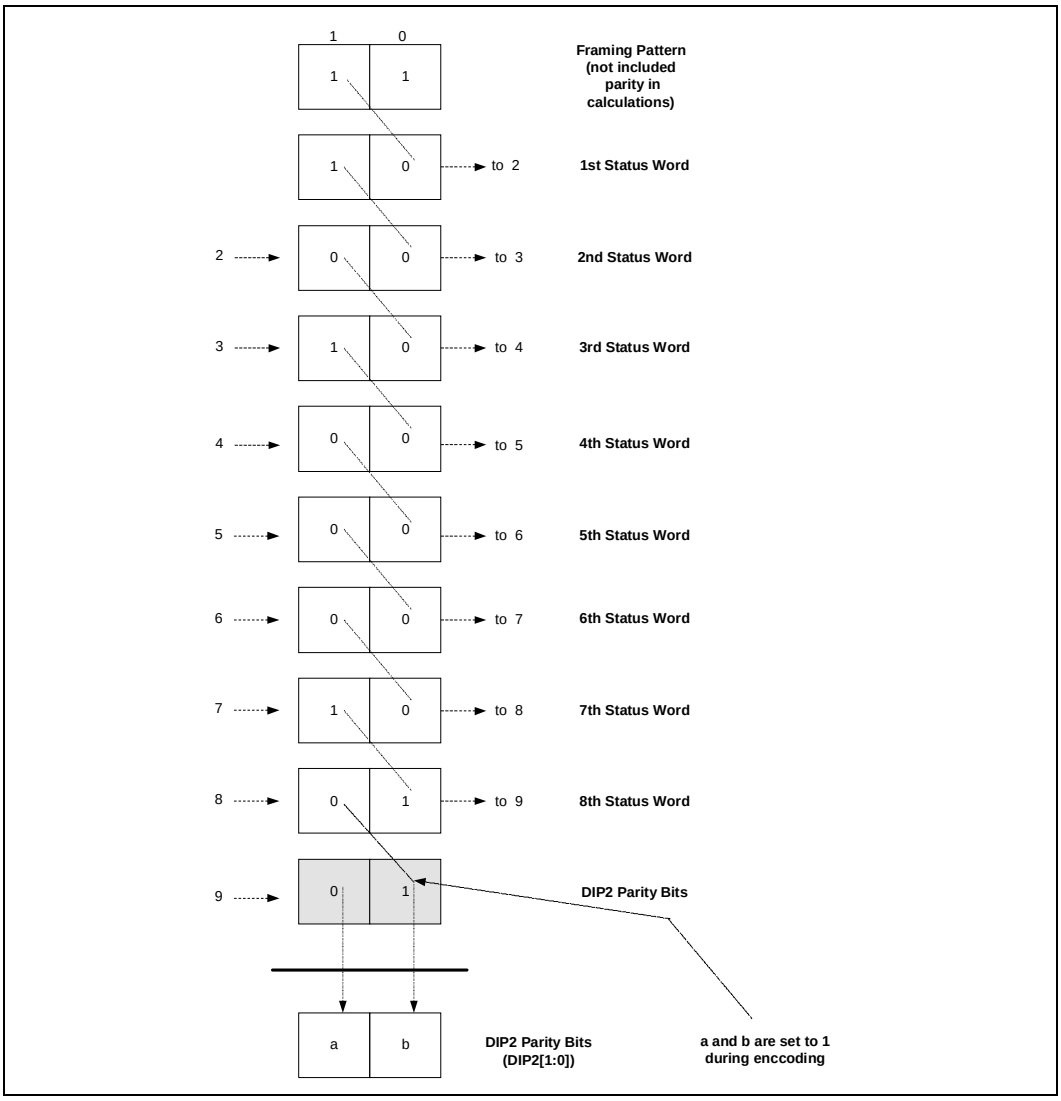
Figure 14. FIFO Status State Diagram



The FIFO status of each port is encoded in a 2-bit data structure, which is defined in Table 20, "FIFO Status Format" on page 69. The most significant bit of each port status is sent over TSTAT[1]/RSTAT[1] and the least significant bit is sent over TSTAT[0]/RSTAT[0]. The "1 1" pattern is reserved for In-band framing, which must be sent once prior to the start of the FIFO status sequence.

Immediately before the "1 1" framing pattern, a DIP-2 odd parity checksum is sent at the end of each complete sequence. The DIP-2 code is computed diagonally over TSTAT[1]/RSTAT[1] and TSTAT[0]/RSTAT[0] for all preceding FIFO status indications sent after the last "1 1" framing pattern, as shown in Figure 15, "Example of DIP-2 Encoding" on page 68. The first word is at the top of the figure and the last word is at the bottom. The parity bits are computed by summing diagonally. Bits a and b in line 9 correspond to the space occupied by the DIP-2 parity bits and are set to 1 during encoding. The "1 1" framing pattern is not included in the parity calculation. The procedure described applies to either parity generation on the egress path or to check parity on the ingress path.

Figure 15. Example of DIP-2 Encoding



When the parity bits mimic the “1 1” pattern, the receiving end still frames successfully by syncing onto the last cycle in a repeated “1 1” pattern, and by making use of the configured sequence length when searching for the framing pattern.

To permit more efficient FIFO utilization, the MaxBurst1 and MaxBurst2 credits are granted and consumed in increments of 16-byte blocks. For any given port, these credits correspond to the most recently received FIFO status. They are not cumulative and supersede previously granted credits for the given port. A burst transfer shorter than 16 bytes (for example, an end-of-packet fragment) consumes an entire 16-byte credit.

A continuous stream of repeated “1 1” framing patterns indicates a disabled status link. For example, it may be sent to indicate that the data path de-skew is not yet completed or confirmed. When a repeated “1 1” pattern is detected, all outstanding credits are cancelled and set to zero.

Table 20. FIFO Status Format

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED: Indicates that the corresponding port's FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY: When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks, or the remainder of what was previously granted (whatever is greater), may be sent to the corresponding port until the next status update.
0	0	STARVING: Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update

The indicated FIFO status is based on the latest available information. A STARVING indication provides additional feedback information, so that transfers are scheduled accordingly. Applications that do not distinguish between HUNGRY and STARVING may only examine the most significant FIFO status bit.

Note: If a port is disabled on the IXF1110, FIFO status for the port is set to SATISFIED to avoid the possibility of any data being sent to it by the controlling device. This applies to the IXF1110 transmit path.

Upon reset, the FIFOs in the data path receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, and before active traffic is generated, the data transmitter sends continuous training patterns. Transmission of the training patterns continues until valid information is received on the FIFO Status channel. The receiver ignores all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisional number of consecutive correct DIP-4 code words is seen. Loss of synchronization may be reported after a provisional number of consecutive DIP-4 code words is detected. [For details, see Table 104, “SPI4-2 TX Synchronization ($ 0x703)” on page 174.]

The DIP-4 thresholds are programmable. However, there is a potential issue with the possibility of a given link showing DIP-4 errors that may never lose synchronization and re-train to fix the issue. This would mean an on-going and potentially significant loss of data on the link affecting all ports transferring data at that time.

This issue may be seen in the following two instances:

- During training (most likely periodic training)
- During data transfers where each of the data transfers (MaxBurst1 or MaxBurst2) are separated by more than one idle control word

The mechanism for both issues is the same because data will not change during a repeated period of the same control word being transmitted on the link. If there have been some consecutive DIP-4 errors, they will be incremented towards the Loss-of-Sync threshold. This is most likely to occur from a path requiring de-skew. If either a stream of idles or training control words follow the burst and the DIP-4 associated with each of the words is checked, only the first one and the last one will be seen as invalid. Any other control words in the middle will be seen as having a valid DIP-4 and will reset the Loss-of-Sync threshold counter back to zero.

In order to avoid this, the IXF1110 has altered the way in which the check is done for idle control words and training control words. We now only validate the first occurrence of the DIP-4 in both training control words and idle control words for correctness. We do still check each of the words but only use the first occurrence to clear the DIP-4 error counter. Any DIP-4 error in any of these words is still counted towards the Loss-of-Sync threshold counter. It is now impossible to mask the DIP-4 error on our interface.

5.2.5 DC Parameters

For DC parameters on the SPI4-2 interface, please refer to Table 36, “2.5 V LVTTL and CMOS I/O Electrical Characteristics” on page 107 and Table 37, “LVDS I/O Electrical Characteristics” on page 107.

5.3 SerDes Interface

5.3.1 Introduction

The IXF1110 has ten integrated Serializer/Deserializer (SerDes) devices that allow direct connection to optical modules. Each SerDes interface is fully compliant with the relevant IEEE 802.3 Specifications, including auto-negotiation (see “Fiber Operation” on page 50. Each port is also compliant with and supports the requirements of the Small Form Factor Pluggable (SFP) Multi-Source Agreement (MSA), see “Optical Module Interface” on page 72.

The following sections describe the operations supported by each SerDes interface, the configurable options, and register bits that control these options. (A full list of the register addresses and full bit definitions are found in the Register Map (Table 58, “SerDes Block Register Map” on page 130).

5.3.2 Features

The SerDes cores are designed to operate in point-to-point data transmission applications. While the core can be used across various media types, such as PCB or backplanes, it is configured specifically for use in 1000BASE-X Ethernet fiber applications in the IXF1110. The following features are supported.

- 10-bit data path, which connects to the output/input of the 8B/10B encoder/decoder PCS that resides in the MAC controller
- Data frequency of 1.25 GHz
- Low power: <200 mW per SerDes port
- Asynchronous clock data recovery

5.3.3 Functional Description

The SerDes transmit interface sends serialized data at 1.25 GHz. The interface is differential with two pins for transmit operation. The transmit interface is designed to operate in a 100 Ω differential environment and all the terminations are included on the device. The outputs are high speed SerDes and AC coupling is recommended for this interface to ensure that the correct input bias current is supplied at the receiver.

The SerDes receive interface receives serialized data at 1.25 GHz. The interface is differential with two pins for the receive operation. The equalizer receives a differential signal that is equalized for the assumed media channel. The SerDes transmit and receive interfaces are designed to operate within a 100 Ω differential environment and all terminations are included on the device.

5.3.3.1 Transmitter Operational Overview

The transmit section of the IXF1110 has to serialize the Ten Bit Interface (TBI) data from the IXF1110 MAC section and outputs this data at 1.25 GHz differential signal levels. The 1.25 GHz differential SerDes signals are compliant with the Small Form Factor Pluggable (SFP) Multi-Source Agreement (MSA).

The transmitter section takes the contents of the data register within the MAC and synchronously transfers the data out, ten bits at a time – Least Significant Bit (LSB) first, followed by the next Most Significant Bit (MSB). When these ten bits have been serialized and transmitted, the next word of 10-bit data from the MAC is ready to be serialized for transmission.

The data is transmitted by the high-speed current mode differential SerDes output stage using an internal 1.25 GHz clock generated from the 125 MHz clock input.

5.3.3.2 Transmitter Programmable Driver-Power Levels

The IXF1110 SerDes core has programmable transmitter power levels to enhance usability in any given application.The SerDes Registers are programmable to allow adjustment of the transmit core driver output power. When driving a 100 Ω differential terminated network, these output power settings effectively establish the differential voltage swings at the driver output.

The (Register) allows the selection of 4 discrete power settings. The selected power setting of these inputs is applied to each of the transmit cores drivers on a per-port basis. Table 17, “SPI4-2 Interface Signal Summary” lists the Normalized power setting of the transmit drivers as a function of the Driver Power Control inputs. The normalized current setting is 10 mA which corresponds to the normalized power setting of 1.0. This is the default setting of the IXF1110 SerDes interface. Other values listed in the Normalized Driver Power Setting column are multiples of 10 mA. For example, with inputs at 1110, the driver power is .5 x 10 mA = 5 mA.

Table 21. SerDes Driver TX Power Levels

DRVPWRx[3]	DRVPWRx[2]	DRVPWRx[1]	DRVPWRx[0]	Normalized Driver Power Setting	Driver Power
0	0	1	1	1.33	13.3 mA
1	0	1	1	2.0	20 mA
1	1	0	1	1.0	10 mA
1	1	1	0	0.5	5 mA
NOTE: All other values are reserved.					

5.3.3.3 Receiver Operational Overview

The receiver structure performs Clock and Data Recovery (CDR) on the incoming serial data stream. The quality of this operation is a dominant factor for the Bit Error Rate (BER) system performance. Feed forward and feedback controls are combined in one receiver architecture for enhanced performance. The data is over-sampled and a digital circuit detects the edge position in the data stream. A signal is not generated if an edge is not found. A feedback loop takes care of low-frequency jitter phenomenon of unlimited amplitude, while a feed forward section suppresses high-frequency jitter having limited amplitude. The static edge position is held at a constant position in the over-sampled by a constant adjustment of the sampling phases with the early and late signals.

5.3.3.4 Selective Power-Down

The IXF1110 offers the ability to selectively power-down any of the SerDes TX or RX ports that are not being used. This is done via "SerDes TX and RX Power-Down Ports 0-9 ($ 0x787)" on page 175.

5.3.4 Timing and Electrical Characteristics

For timing and electrical characteristics for the IXF1110, see Figure 39, "SerDes Timing" on page 118, "Transmitter Characteristics" on page 118 and "Receiver Characteristics" on page 119.

5.4 Optical Module Interface

5.4.1 Introduction

This section describes the connection of the IXF1110 ports to an optical module, and the connections supported for correct operation are detailed. The registers used to write control and read status information are documented in Section 8.5.9, "Optical Module Interface Block Register Overview" on page 176).

The optical module interface allows the IXF1110 a seamless connection to the Small Form Factor Optical Modules (SFP) that form the system's physical media connection, eliminating the need for any FPGAs or CPUs to process data. All required information of the optical modules is available to the system CPU through the IXF1110 CPU interface, leading to a more integrated, reliable, and cost-effective system.

5.4.2 IXF1110 Supported Optical Module Interface Signals.

For optical module interface operation, three supported signal subgroups are required, allowing a more explicit definition of each function and implementation. The three subgroups are as follows:

- High-Speed Serial Interface
- Low-Speed Status Signaling Interface
- I^2C Module Configuration Interface

Table 22 provides descriptions for IXF1110-to-SFP optical module connection pins.

Table 22. IXF1110-to-SFP Connections

IXF1110 Pin Names	SFP Module Pin Name	Description	Notes
TX_9:0_P	TD+	Transmit Data, Differential SerDes	Output from the IXF1110
TX_9:0_N	TD-		
RX_9:0_P	RD+	Receive Data, Differential SerDes	Input to the IXF1110
RX_9:0_N	RD-		
I^2C_CLK	MOD-DEF1	I^2C_CLK Output from IXF1110 (SCL)	Output from the IXF1110
I^2C_DATA_9:0	MOD-DEF2	I^2C_DATA I/O (SDA)	Input/Output
MOD_DEF_9:0	MOD-DEF0	MOD_DEF(0) should be TTL Low level during normal operation.	Input to the IXF1110
TX_DISABLE_9:0	TX DISABLE	Transmitter Disable, Logic High, Open collector compatible	Output from the IXF1110
TX_FAULT_9:0	TX FAULT	Transmitter Fault, Logic High, Open collector compatible	Input to the IXF1110
RX_LOS_9:0	LOS	Receiver Loss of Signal, Logic High, Open collector compatible	Input to the IXF1110

5.4.3 Functional Descriptions

5.4.3.1 High-Speed Serial Interface

These signals are responsible for transfer of the actual data at 1.25 Gbps. The data is 8B/10B encoded and transmitted differentially at SerDes levels per the required specifications.

The signals required to implement the high-speed serial interface are:

- TX_9:0_P
- TX_9:0_N
- RX_9:0_P
- RX_9:0_N

5.4.3.2 Low-Speed Status Signaling Interface

The following low-speed signals indicate the state of the line via the optical module:

- MOD_DEF_9:0
- TX_FAULT_9:0
- RX_LOS_9:0
- TX_DISABLE_9:0
- MOD_DEF_Int
- TX_FAULT_Int
- RX_LOS_Int

5.4.3.2.1 MOD_DEF_9:0

These signals are direct inputs to the IXF1110 and are pulled to a logic Low level during normal operation, indicating that a module is present for each port, respectively. If a module is not present, a logic High is received, which is achieved by an external pull-up resistor at the IXF1110 pad.

The status of each bit (one for each port) is found in bits 9:0 of the Optical Module Status Register (refer to Table 108, "Optical Module Status Ports 0-9 ($ 0x799)" on page 176). Any change in the state of these bits causes a logic Low level on the MOD_DEF_Int output if this operation is enabled.

5.4.3.2.2 TX_FAULT_9:0

These 10 pins are inputs to the IXF1110. These signals are pulled to a logic Low level by the optical module during normal operation, which indicates no fault condition exists. If a fault is present, a logic High is received via the use of an external pull-up resistor at the IXF1110 pad.

The status of each bit (one for each port) can be found in bits 19:10 of the Optical Module Status Register (see Table 108, "Optical Module Status Ports 0-9 ($ 0x799)" on page 176). Any change in the state of these bits causes a logic Low level on the TX_FAULT_Int output if this operation is enabled.

5.4.3.2.3 RX_LOS_9:0

These 10 pins are inputs to the IXF1110. During normal operation, these signals are pulled to a logic Low level by the optical module, which indicates that no Loss-of-Signal exists. If a Loss-of-Signal occurs, a logic High is received on these inputs via the use of an external pull-up resistor at the IXF1110 pad.

The status of each bit (one for each port) is found in "Optical Module Status Ports 0-9 ($ 0x799)" bits 29:20. Any change in the state of these bits causes a logic Low level on the RX_LOS_Int output if this operation is enabled.

5.4.3.2.4 TX_DISABLE_0:9

These 10 pins are outputs from the IXF1110. During normal operation, these signals are pulled to a logic Low level by the IXF1110, indicating that the optical module transmitter is enabled. If the optical module transmitter is disabled, these signals are switched to a logic High level. On the IXF1110, these outputs are open-drain types and pulled up by the 4.7k to 10k pull-up resistor at the optical module. Each of these signals is controlled via "Optical Module Control Ports 0-9 ($ 0x79A)" bits 9:0, respectively.

5.4.3.2.5 MOD_DEF_INT

MOD_DEF_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the MOD_DEF_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the "Optical Module Status Ports 0-9 ($ 0x799)" takes place. The signal then returns to an inactive state.

Note: The MOD_DEF_9:0 inputs shown in Table 108, "Optical Module Status Ports 0-9 ($ 0x799)" on page 176 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

5.4.3.2.6 Tx_FAULT_INT

TX_FAULT_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the TX_FAULT_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the "Optical Module Status Ports 0-9 ($ 0x799)" takes place. The signal then returns to an inactive state.

Note: The TX_FAULT_9:0 inputs shown in Table 108, "Optical Module Status Ports 0-9 ($ 0x799)" on page 176 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

5.4.3.2.7 RX_LOS_INT

RX_LOS_INT is a single output, open-drain type signal, and is active Low. A change in state of any of the RX_LOS_0:9 inputs causes this signal to switch Low and remain in this state until a Read of the Optical Module Status register has taken place. The signal then returns to an inactive state.

Note: The RX_LOS_0:9 inputs shown in Table 108, "Optical Module Status Ports 0-9 ($ 0x799)" on page 176 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

Note: MOD_DEF_INT, TX_FAULT_INT, and RX_LOS_INT are open-drain type outputs. With the three signals on the device, the system can decide which Optical module Status Register bits to look at to identify the interrupt condition source port. However, this is achieved at the expense of two device pins.

In systems that cannot support multiple interrupt signals (applications that do not have extra hardware pins), these three outputs can be connected to a single pull-up resistor and used as a single interrupt pin.

5.4.4 I^2C Module Configuration Interface

The I^2C interface is supported on SFP optical modules. Details of the operation are found in the SFP multi-source agreement (MSA). This document details the contents of the registers and addresses accessible on a given optical module supporting this interface.

The SFP MSA identifies up to 512 8-bit registers that are accessible in each optical module. The I^2C interface is Read/Write capable and supports either sequential or random access to the 8-bit parameters. The maximum clock rate of the interface is 100 kHz. All address select pins on the internal E^2PROM are tied Low to give a device address equal to zero (00h).

The specific interface in the IXF1110 supports only a subset of the full I^2C interface, and only the features required to support the optical modules are implemented, leading to the following support features:

- Single I^2C_CLK pin connected to all modules, and implemented to save unnecessary pin use.
- Ten per-port I^2C_DATA pins optical ($I^2C_DATA_9:0$) are required due to the optical module requirement that all modules must be addressed as 00h.

Document Number: 250210
Revision Number: 008
Revision Date: August 10, 2004

- Due to the single internal controller, only one optical module may be accessed at any one time. Optical module accesses contains a single register Read. Since these register accesses will most likely be done during power-up or discovery of a new module, these restrictions should not affect normal operation.
- The I^2C interface also supports byte write accesses to the full address range.

5.4.4.1 General Description

In the IXF1110, the entire I^2C interface is controlled through separate I^2C Control and Data Registers (see "I2C Control Ports 0-9 ($ 0x79B)" on page 176 and "I2C Data Ports 0-9 ($ 0x79C)" on page 177. The general operation is described below.

The I^2C Control Register is divided into the following sections:

- Port Address Error
- Write Protect Error bit
- No Acknowledge Error bit
- I^2C Enable bit
- I^2C Start Access bit
- Write Access Complete bit
- Read DataValid bit
- 4-bit Port Address Select
- Read/Write access select
- 4-bit Device ID
- 11-bit Register Address

The I^2C Data Register is divided into the following sections:

- 8-bit Write Data
- 8-bit Read Data

The 4-bit Device ID field defaults to Ah, this value is compatible with standard fiber module based on the Atmel Serial E^2Prom family. I^2C accesses to non-Atmel compatible devices will require to update this field with the appropriate value.

The 11-bit Register Address is split into two sub-fields:

- Bits [10:8] must be set to 0h to be compatible with standard fiber optical module. Alternatively these bits can be set to 1h - 7h to permit access to seven other I^2C component on the same bus.
- Bits [7:0] specify the particular location to be accessed within the device specified by the Device ID field and Register Address[10:8].

Initiating an access where the 4-bit Port Address field to a value > 9h will not generate an I^2C access. Instead the Port Address Error will be set.

Initiating a write access where the Device ID field = Ah and the Register Address[10:8] = 0h will generate an I^2C access. In addition the Write Protect Error bit will be set to indicate a write has been initiated to the write protected optical module.

5.4.4.1.1 Read Access Operation Example

The following sequence provides an example of reading the data stored in the Optical Module Register 0x000 for Port 5:

1. Program the "I2C Control Ports 0-9 ($ 0x79B)" on page 176 with the following information:
   a. Enable I^2C Block by setting bit 25 to '1'.
   b. Set the port to be accessed by setting bits [19:16] to 0x5.
   c. Select a READ access by setting bit 15 to '1'.
   d. Set the Device ID, bits [14:11] to be 0xA (Atmel compatible).
   e. Set the 11-bit Register Address, bits [10:0] to 0x000.
   f. Initiate the I^2C transfer by setting bit 24 to '1'.

   All other bits in this register should be written with the value '0'.

   This data is written into the I^2C Control Register in a single cycle via the CPU interface.
2. When this register is written and the I^2C Start bit is at a Logic 1, the I^2C access state machine examines the Port Address Select and enables the I^2C_DATA_0:9 output for the selected port.
3. The state machine uses the data in the Device ID and Register Address fields to build the data frame to be sent to the optical module.
4. The I^2C DATA_READ_FSM internal state machine takes over the task of transferring the actual data between the IXF1110 and the selected optical module (refer to the details in Section 5.4.4.2, "I2C Protocol Specifics" on page 78).
5. The I^2C DATA_READ_FSM internal state machine places the received data into the Read_Data field, bits [7:0] of the I^2C Data Register, and sets the Read Data Valid bit, bit 20 of the I^2C Control Register to '1' to signify that the Read data is valid.
6. The data is read through the CPU interface. The CPU must poll the Read Data Valid bit until it is set to '1. Only once this bit is set, it is safe to read the data in the I^2C Data Register.

5.4.4.1.2 Write Access Operation Example

The following sequence provides an example of writing data to the Optical Module Register 0xFF for Port 9:

1. Program the "I2C Control Ports 0-9 ($ 0x79B)" with the following information:
   a. Enable I^2C Block by setting bit 25 to '1'.
   b. Set the port to be accessed by setting bits [19:16] to 0x9.
   c. Select a WRITE access by setting bit 15 to '0'.
   d. Set the Device ID, bits [14:11] to be 0xA (Atmel compatible).
   e. Set the 11-bit Register Address, bits [10:0] to 0xFF.
   f. Initiate the I^2C transfer by setting bit 24 to '1'.

   All other bits in this register should be written with the value '0'.

   This data is written into the I^2C Control Register in a single cycle via the CPU interface.

2. When this register is written and the I2C Start bit is at a Logic 1, the I2C access state machine examines the Port Address Select and enables the I2C_DATA_0:9 output for the selected port.
3. The state machine uses the data in the Device ID and Register Address fields to build the data frame to be sent to the optical module.
4. The I2C DATA_WRITE_FSM internal state machine takes over the task of transferring the actual data between the IXF1110 and the selected optical module (refer to the details in Section 5.4.4.2, “I2C Protocol Specifics” on page 78).
5. The I2C DATA_WRITE_FSM internal state machine uses the data from the Write_Data field, bits [23:16] of the I2C Data Register, and sets the Write_Complete bit, bit 22 of the I2C Control Register to ‘1’ to signify that the Write Access is complete.
6. The data is written through the CPU interface. The CPU must poll the Write_Complete bit until it is set to ‘1. Only once this bit is set, it is safe to request a new access.

Note: Only one optical module I2C access sequence can be run at any given time. If a second Write is carried out to the I2C Control Register before a result is returned for the previous Write, the data for the first Write is lost. To ensure no data is lost, make sure Write complete = 1 before starting the next Write sequence.

5.4.4.2 I2C Protocol Specifics

This section describes the I2C protocol behavior supported by the IXF1110, which is controlled by an internal state machine. Specific protocol states are defined below, with an additional description of the hardware pins used on the interface.

The Serial Clock Line (I2C_CLK) is an IXF1110 output. The serial data is synchronous with this clock and is driven off the rising edge by the IXF1110 and off the falling edge by the optical module. The IXF1110 has only one I2C_CLK line that drives all of the optical modules. The I2C_CLK runs continuously when enabled (I2C Enable = 01h0).

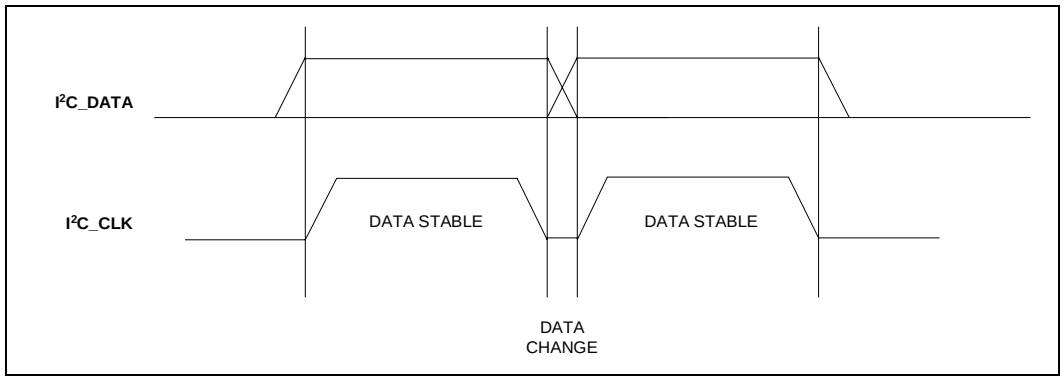
The Serial Data (I2C_DATA_0:9) pins (one per port) are bi-directional for serial data transfer, and are open drain.

5.4.4.3 Port Protocol Operation

5.4.4.4 Clock and Data Transitions

The I2C_DATA is normally pulled High with an extra device. Data on the I2C_DATA pin changes only during the I2C_CLK Low time periods (see Figure 16). Data changes during I2C_CLK High periods indicate a start or stop condition.

Figure 16. Data Validity Timing



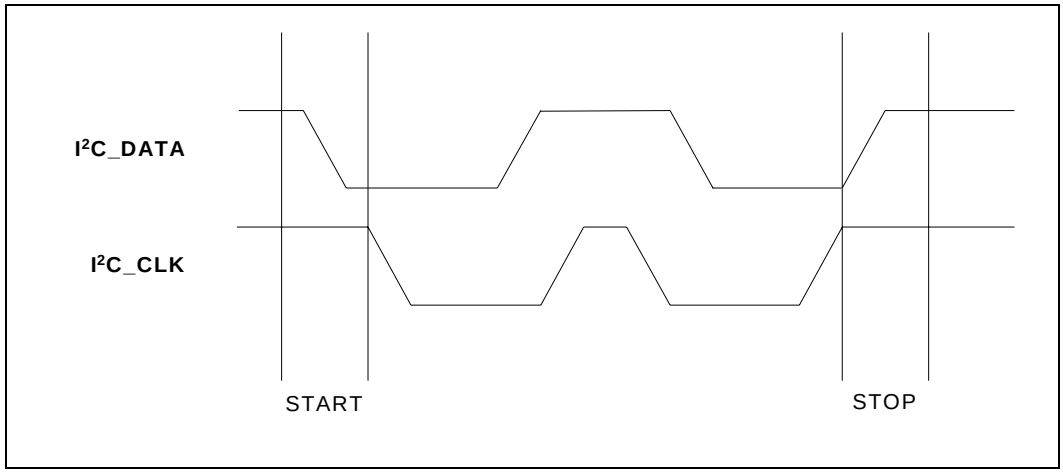
5.4.4.4.1 Start Condition

A High-to-Low transition of I^2C_DATA, with I^2C_CLK High, is a start condition that must precede any other command (see Figure 17).

5.4.4.4.2 Stop Condition

A Low-to-High transition of the I^2C_DATA with I^2C_CLK High is a stop condition. After a Read sequence, the stop command places the E^2PROM in the optical in a standby power mode (see Figure 17).

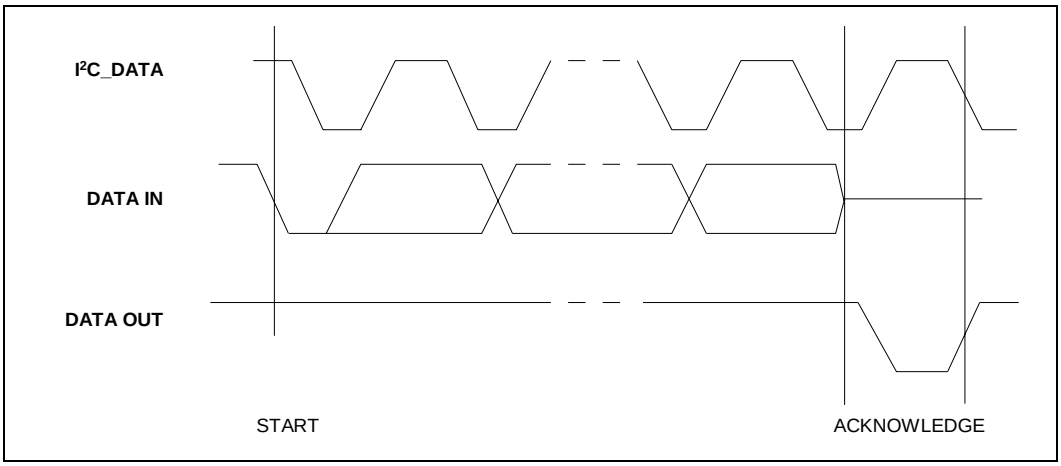
Figure 17. Start and Stop Definition Timing



5.4.4.4.3 Acknowledge

All addresses and data words are serially transmitted to and from the optical module in 8-bit words. The optical module E^2PROM sends a zero to acknowledge that it has received each word, which happens during the ninth clock cycle (see Figure 18).

Figure 18. Acknowledge Timing



5.4.4.4.4 Memory Reset

After an interruption in protocol, power loss, or system reset, any two-wire Optical Module can be reset by following three steps:

1. Clock up to nine cycles
2. Wait for I^2C_DATA High in each cycle while I^2C_CLK is High
3. Initiate a start condition

The following defines device memory reset:

- Always add a stop condition following the start as there is no clean finish to end the reset of the memory with a start condition after completing steps one through three. This ensures a clean protocol termination if there is no more data to transfer at the end of the reset cycle.

5.4.4.4.5 Device Addressing

All E^2PROMs in Optical Module devices require an 8-bit device address word following a start condition to enable the chip to read or write. The device address word consists of a mandatory one, zero sequence for the four most significant bits. This is common to all devices. The next 3 bits are the A2, A1 and A0 device address bits that are tied to zero in a optical module. The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is High and a Write operation is initiated if this bit is Low.

Upon comparison of the device address, the optical module outputs a zero. If a comparison is not made, the optical module E^2PROM returns to a standby state.

When not accessing the optical module E^2PROM, the device address or device ID is completely programmable for maximum flexibility.

5.4.4.4.6 Random Read Operation

A random Read requires a “dummy” Byte/Write sequence to load the data word address. The following describes how to achieve the “dummy” Write:

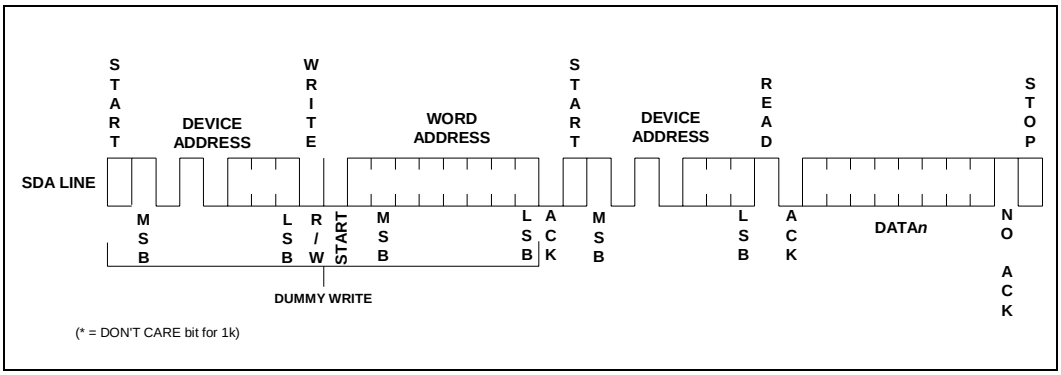
- The IXF1110 generates a start condition.
- The IXF1110 sends a device address word with the Read/Write bit cleared to Low, signaling a Write operation.
- The optical module acknowledges receipt of the device address word.
- The IXF1110 sends the data word address, which is again acknowledged by the optical module.
- The IXF1110 generates another start condition.

This completes the “dummy” Write and sets the optical module E^2PROM pointers to the desired location.

The following describes how the IXF1110 initiates a current address Read:

- The IXF1110 sends a device address with the Read/Write bit set High
- The optical module acknowledges the device address and serially clocks out the data word.
- The IXF1110 does not respond with a zero but generates a stop condition (see Figure 19).

Figure 19. Random Read



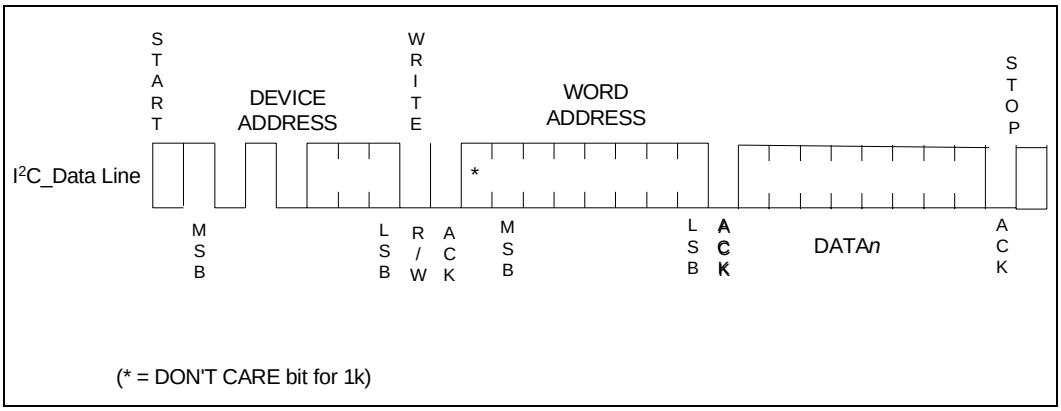
Timing diagrams and tables can be found in Section 7.0, “Electrical Specifications” on page 105.

5.4.4.4.7 Byte Write Operation

The following describes how to achieve the byte write operation:

- The IXF1110 generates a start condition.
- The IXF1110 sends a device address word with the Read/Write bit cleared to Low, signaling a Write operation.
- The optical module acknowledges receipt of the device address word.
- The IXF1110 sends the data word address.
- The optical module acknowledges receipt of the data word address.
- The IXF1110 sends the data byte to be written.
- The optical module acknowledges the data word.
- The IXF1110 generates a stop condition (see Figure 20).

Figure 20. Byte Write



5.4.4.5 AC Timing Characteristics

Table 43, "I2C AC Timing Characteristics" on page 114, Figure 35, "I2C Bus Timing" on page 114, and Figure 36, "I2C Write Cycle" on page 114 provide the AC timing characteristics of the optical module interface.

5.5 LED Interface

5.5.1 Introduction

The IXF1110 uses a serial interface consisting of three signals to provide LED data to a serial-to-parallel logic external driver. The three signals are as follows:

- LED CLK: This clock is provided by the IXF1110 to clock the external parallel-to-serial shift registers.
- LED DATA: This serial data is provided by the IXF1110 to the external parallel-to-serial shift registers.
- LED LATCH: This latch is provided by the IXF1110 to latch the data on the parallel-to-serial shift registers.

The LED_DATA stream provides data for 30 separate direct drive LEDs and allows three LEDs per MAC port. The three LED pins outlined above are detailed in Table 23, "LED Signal Descriptions".

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in Section 5.5.2, "Modes of Operation".

5.5.2 Modes of Operation

Mode selection is accomplished by using bit 0 of the "LED Control ($ 0x509)" on page 151. This bit is globally selected and controls the mode of operation of all ports Section 5.5.2.1 and Section 5.5.2.2 provide the two modes of operation.

5.5.2.1 Mode 0

This mode selects operations compatible with the SGS Thompson M5450 Led Display Driver Device. This device converts the serial data stream, output by IXF1110, into 30 direct-drive LED outputs. In this mode, the latch signal is not required. This mode is selected by setting bit 0 of the "LED Control ($ 0x509)" to 0 (default).

5.5.2.2 Mode 1

This mode selects operations compatible with TTL (74LS595) or HCMOS (74HC595) octal shift registers. This device converts the serial data stream, output by IXF1110, into 30 direct-drive LED outputs. In this mode the LED DATA, LED CLK and LED LATCH signals are used. This mode is selected by setting bit 0 of the "LED Control ($ 0x509)" to 1.

5.5.3 LED Interface Signal Description

The IXF1110 LED interface consists of three output signal pins that are 2.5 V CMOS level pads. Table 23, "LED Signal Descriptions" provides LED signal names, pin numbers, and descriptions.

Table 23. LED Signal Descriptions

Signal Name	Ball Designator	Signal Description
LED_CLK	A20	**LED_CLK:** This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 720 hz. The behavior of this signal remains constant in all modes of operation.
LED_DATA	A19	**LED_DATA:** This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	K18	**LED_LATCH:** This is an output pin and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

5.5.4 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 21 on page 84 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 21 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device.The actual data shown in Figure 21 consists of a chain of 36 bits only, 30 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 21. Mode 0 Timing

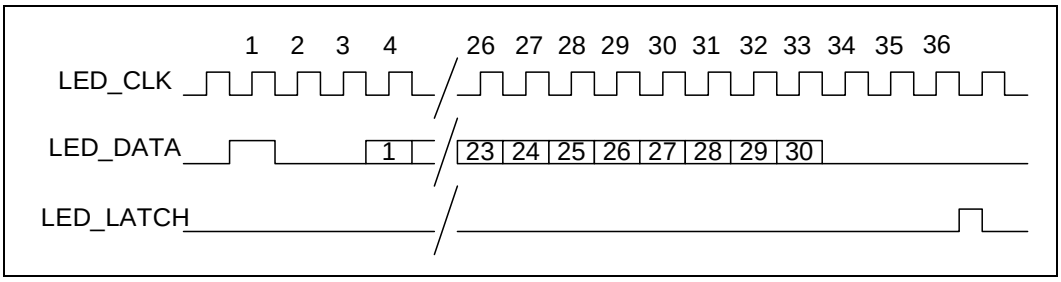


Table 24. Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 30 bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.
4:33	LED DATA 1-30	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in Table 23, “LED Signal Descriptions” on page 83. The data is TRUE. Logic 1(LED ON) = High
34:36	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.

When implemented on a board with the M5450 device, the LED DATA bit 1 appears on output bit 3 of the M5450 and the LED DATA bit 2 appears on output bit 4, etc. This means that output bits 1, 2, 3, 34, and 35 will never have valid data and should not be used.

5.5.5 Mode 1: Detailed Operation

Note: Please refer to manufacturers’ 74LS/HC595 datasheet for information on device operation.

The operation of the LED Interface in Mode 1 is again based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK.

Figure 22 on page 85 shows the basic timing relationship and relative positioning in the data stream of each bit. Figure 22 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift Register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC595 device. As seen in Figure 22, the LED_LATCH signal is active High during the Low period on the 36th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC595 devices, the LED DATA bit 1 is output on Shift Register bit 1, and so on up the chain. Only Shift Register bits 31 and 32 do not contain valid data. The actual data shown in Figure 22 consists of a 36-bit chain, of which 30 bits are valid LED DATA. The 36-bit data chain is built up as follows:

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 22. Mode 1 Timing

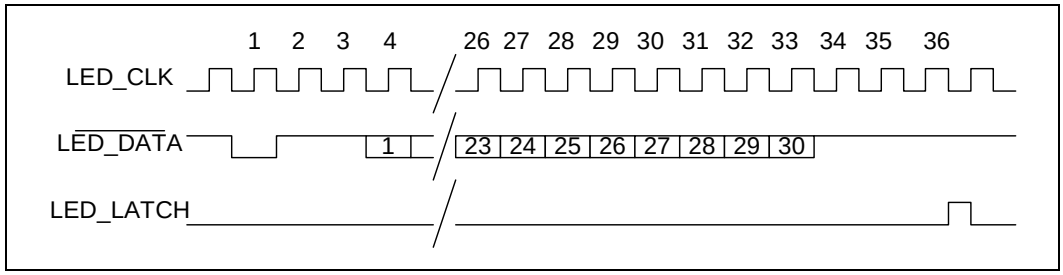


Table 25. Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
4:33	LED DATA 1-30	These bits are the actual data to be transmitted to the 32-stage shift register chain. The decode for each bit in each mode is defined in Table 25 on page 85. The data is INVERTED. Logic 1 (LED ON) = Low.
34:36	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

5.5.6 Power-On, Reset, and Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1110 device configuration is completed.

5.5.6.1 Enabling the LED Interface

"LED Control ($ 0x509)": This register must be set to globally enable LED interface. This is done by setting the LED_ENABLE bit to a logic 1. The power-on default for this bit is Logic 0.

"Port Enable ($ 0x500)": This register enables and disables ports on a per port basis. A port must be enabled for the LEDs to operate for that port. If the port is not enabled, the LEDs will be off for that port. The power-on default for this register is 0x3FF, which means all ports are enabled.

"Link LED Enable ($ 0x502)": This register must be set on a per port basis when link is detected by the system software. This enables the per-port link LEDs for the IXF1110. Link LEDs do not automatically update. For more details on which LEDs are affected by this register, refer to section Section 5.5.7.1, "LED Signaling Behavior" on page 86.

5.5.7 LED Data Decodes

Table 26 shows the data decode of the data for the IXF1110.

5.5.7.1 LED Signaling Behavior

Table 26. LED Data Decodes

LED_DATA#	MACPORT #	IXF1110 Designation
1	0	Rx LED - Amber
2		Rx LED - Green
3		Tx LED - Green
4	1	Rx LED - Amber
5		Rx LED - Green
6		Tx LED - Green
7	2	Rx LED - Amber
8		Rx LED - Green
9		Tx LED - Green
10	3	Rx LED - Amber
11		Rx LED - Green
12		Tx LED - Green
13	4	Rx LED - Amber
14		Rx LED - Green
15		Tx LED - Green
16	5	Rx LED - Amber
17		Rx LED - Green
18		Tx LED - Green
19	6	Rx LED - Amber
20		Rx LED - Green
21		Tx LED - Green
22	7	Rx LED - Amber
23		Rx LED - Green
24		Tx LED - Green
25	8	Rx LED - Amber
26		Rx LED - Green
27		Tx LED - Green
28	9	Rx LED - Amber
29		Rx LED - Green
30		Tx LED - Green

The operation in each mode for the decoded LED data in Table 26 is detailed in Table 27.

Table 27. LED Behavior

Type	Status	Description
RXLED	Off	Synchronization has occurred but no packets are being received and "Link LED Enable ($ 0x502)" has not been set.
	Amber On	RX Synchronization has not occurred or no optical signal exists.
	Amber Blinking	Port has remote fault and "LED Fault Disable ($ 0x50B)" is not set. Based on remote fault bit setting received in RX_Config word.
	Green On	RX Synchronization has occurred and the "Link LED Enable ($ 0x502)" bit is set.
	Green Blinking	RX Synchronization has occurred and port is receiving data.
TXLED	Off	Port is not transmitting data or "Link LED Enable ($ 0x502)" is not set.
	Green Blinking	Port is transmitting data and "Link LED Enable ($ 0x502)" bit is set
NOTE: The LED behavior table assumes the port is enabled in the "Port Enable ($ 0x500)" and the LEDs are enabled in the "LED Control ($ 0x509)". If a port is not enabled, all the LEDs for that port will be off. If the LEDs are not enabled, all of the LEDs will be off.		

5.6 CPU Interface

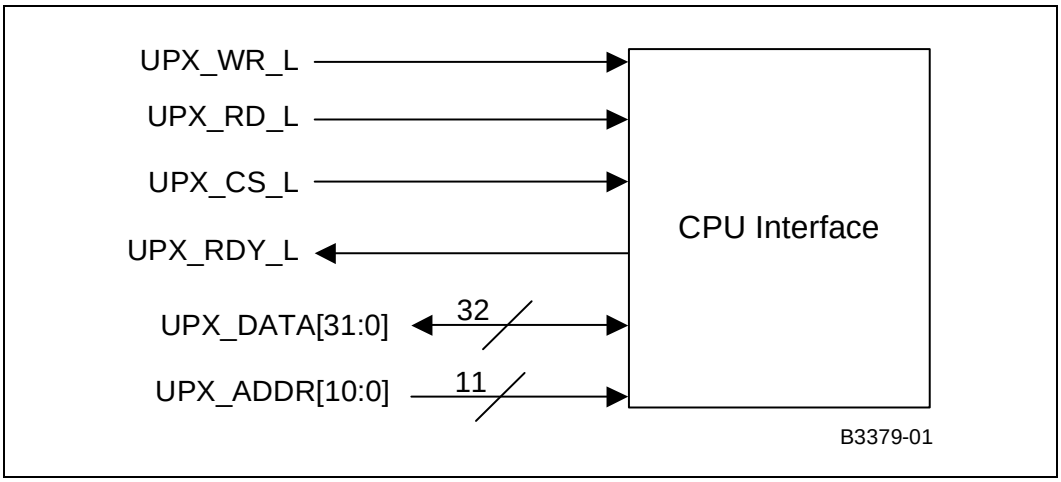
5.6.1 General Description

The CPU Interface block provides access to registers and statistics in the IXF1110. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to the following registers:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- Global Status and Configuration
- RX Block
- TX Block
- SPI4-2 Block
- SerDes Block
- Optical Module Block

Figure 23 illustrates the I/O for the CPU interface on the IXF1110.

Figure 23. CPU Interface Inputs/Outputs



5.6.2 Functional Description

The CPU interface is designed for a generic 32-bit asynchronous CPU bus. The bus is a 32-bit data bus only and has an 11-bit address bus.

The IXF1110 external CPU interface is asynchronous and has no clock. This allows flexibility for CPU selection.The interface to all IXF1110 registers is synchronous to 125 MHz internally.

In some applications, synchronous-to-asynchronous glue logic is required between the IXF1110 and the system CPU. This glue logic must be designed so that the IXF1110 Read and Write access times are not violated. It may be possible to interface without glue logic if the CPU can meet the timing seen in Figure 24, “Read Timing – Asynchronous Interface” on page 90, Figure 25, “Write Timing – Asynchronous Interface” on page 90, and Table 39, “CPU Timing Parameters” on page 109

Table 28. CPU Interface Signals

Name	Direction	Standard	Description
UPX_ADD[10:0]	Input	CMOS 2.5 V	Address bus
UPX_CS_L	Input	CMOS 2.5 V	Chip Select Signal
UPX_DATA[31:0]	Bi_Dir	CMOS 2.5 V	Bi-directional data bus
UPX_WR_L	Input	CMOS 2.5 V	Write Strobe
UPX_RD_L	Input	CMOS 2.5 V	Read Strobe
UPX_RDY_L	Output	CMOS 2.5 V	Cycle complete indicator

UPX_ADD[10:0]

Internal IXF1110 registers and counters are selected using the 11-bit address bus input provided at the CPU interface. This address must be stable for the entire cycle.

UPX_CS_L

The chip select input when active Low selects IXF1110 for the current cycle. No CPU cycle is recognized without this signal being active. At the end of the cycle, the chip select can be driven High to deselect the device or it can be left active if the next access is to the same device (as long as both Read and Write control signals are inactive between cycles).

The CPU usually supports multiple chip selects, and glue logic is required to drive separate chip selects if more than one IXF1110 is being controlled by one CPU.

UPX_DATA[31:0]

These pins comprise the 32-bit data bus pins containing data to and from the CPU interface. This data is asynchronous on the IXF1110. The Write data provided by the CPU must be stable during the entire CPU cycle to prevent erroneous Write operations to a register.

UPX_WR_L

This pin indicates there is data on the CPU data bus to be written to the IXF1110. A Low-to-High transition latches the data and a High-to-Low transition latches the address. This Write operation is active Low.

UPX_RD_L

This pin indicates there is data on the CPU data bus to be read from the IXF1110. A High-to-Low transition latches the address. This Read operation is active Low.

UPX_RDY_L

This pin indicates the Read or Write cycle is complete for the IXF1110. This operation is active Low.

Note: External pull-up resistor required for proper operation.

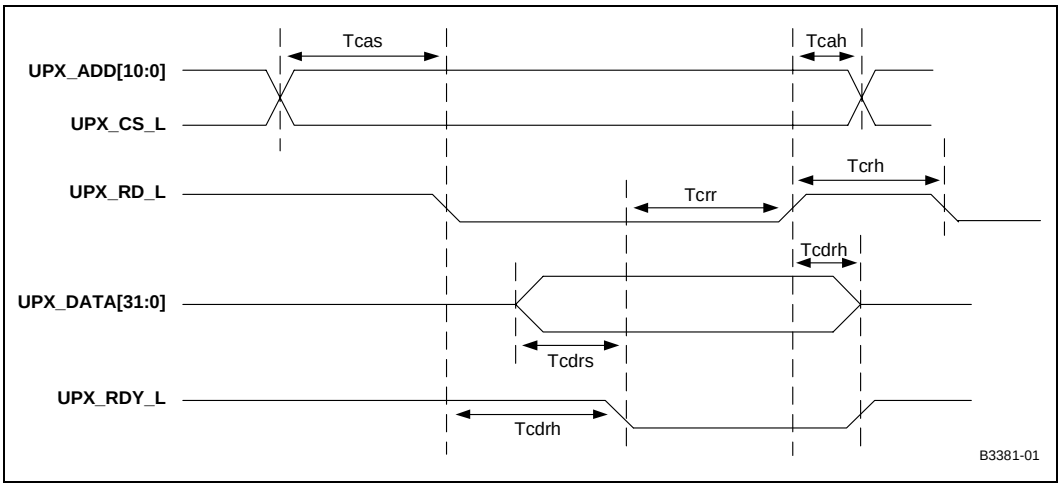
5.6.2.1 Read Access

The IXF1110 read access cycle operation is done in the following order:

1. Chip Select (UPX_CS_L) is asserted at all times for the duration of the operation. The address to be read should be on the IXF1110 address bus (UPX_ADD[10:0]).
2. UPX_RD_L should be asserted by the CPU. The IXF1110 latches the address.
3. IXF1110 drives valid data onto the processor bus (UPX_DATA[31:0]).
4. IXF1110 asserts asynchronous-ready (UPX_RDY_L). This indicates to the CPU that the Read cycle is complete.

Figure 24 provides the timing of the asynchronous interface for Read access.

Figure 24. Read Timing – Asynchronous Interface



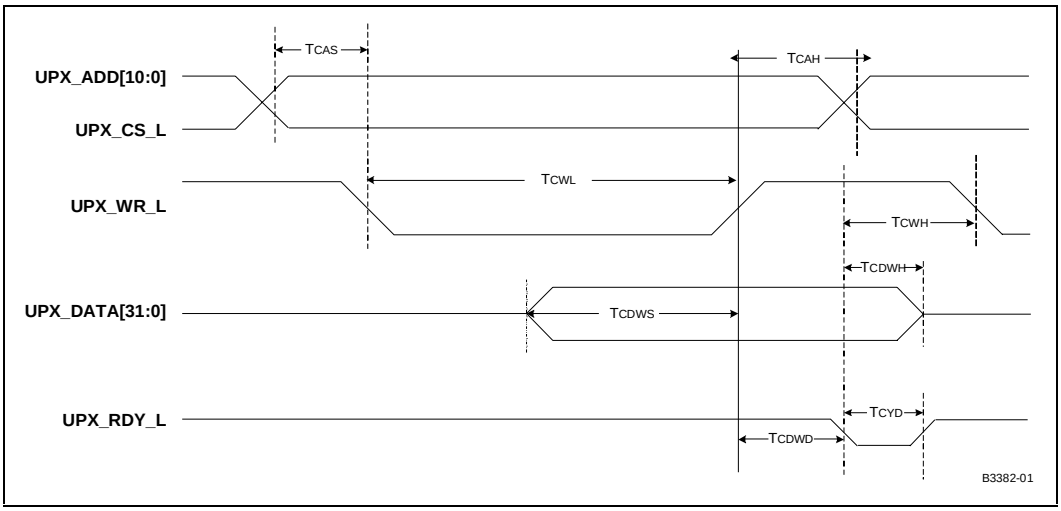
5.6.2.2 Write Access

The IXF1110 Write access cycle operation is done in the following order:

1. Chip Select (UPX_CS_L) is asserted at all times for the duration of the operation. The address to be read should be on the IXF1110 address bus (UPX_ADD[10:0]).
2. UPX_WR_L should be asserted by the CPU. The IXF1110 latches the address.
3. The CPU drives valid data onto the processor bus (UPX_DATA[31:0]).
4. The CPU de-asserts the asynchronous Write signal (UPX_WR_L) of the IXF1110. The IXF1110 latches the data.
5. The IXF1110 asserts asynchronous-ready (UPX_RDY_L). The glue logic indicates to the CPU that the Write cycle is complete.

Figure 25 provides the timing of the asynchronous interface for Write access.

Figure 25. Write Timing – Asynchronous Interface



5.6.2.3 Timing parameters

Timing parameters for the CPU interface are seen in Table 39, “CPU Timing Parameters” on page 109.

5.6.3 Endian

The Endian of the CPU interface may be changed to allow connection of various CPUs to the IXF1110. The Endian selection is determined by setting the Endian bit in the “CPU Interface ($ 0x508)” on page 150).

5.7 JTAG (Boundary Scan)

The IXF1110 includes an IEEE 1149.1 boundary scan test port for board level testing. All inputs are accessible. The BSDL file for this device is available by accessing the intel website developer.intel.com.

5.7.1 TAP Interface (JTAG)

The IXF1110 includes an IEEE 1149.1 compliant Test Access Port (TAP) interface used during boundary scan testing. The interface consists of the following five pins:

- TDI – Serial data input
- TMS – Test mode select
- TCLK – TAP clock
- TRST_L – Active low asynchronous reset for the TAP
- TDO – Serial data output

TDI and TMS require external pull-up resistors to float the pins High per the IEEE 1149.1 specification. Pull-ups are recommended on TCK and TDO. For normal operation, TRST_L can be pulled Low, permanently disabling the JTAG interface. If the JTAG interface is used, the TAP controller must be reset as described in Section 5.7.2, “TAP State Machine” on page 92 and returned to a logic High.

Note: The JTAG pins must be terminated correctly for proper device operation.

Table 29. Recommended JTAG Termination

Signal	Description
TRST_L[1]	Pull-down through 10 K Ω resistor
TDO	Pull-up through 10 K Ω resistor

1. TRST_L must be pulled Low to ensure proper IXF1110 operation. When TRST_L is Low, the JTAG interface is disabled. If the boundary scan logic is used, TRST_L must be pulsed Low after power-up to ensure reset of the TAP controller. For more information, refer to Section 5.7.2, “TAP State Machine” on page 92 or the IEEE 1149.1 Boundary Scan Specification.

Table 29. Recommended JTAG Termination

Signal	Description
TDI	Pull-up through 10 K Ω resistor
TMS	Pull-up through 10 K Ω resistor
TCK	Pull-up through 10 K Ω resistor

1. TRST_L must be pulled Low to ensure proper IXF1110 operation. When TRST_L is Low, the JTAG interface is disabled. If the boundary scan logic is used, TRST_L must be pulsed Low after power-up to ensure reset of the TAP controller. For more information, refer to Section 5.7.2, "TAP State Machine" on page 92 or the IEEE 1149.1 Boundary Scan Specification.

5.7.2 TAP State Machine

The TAP pins drive a TAP controller, which implements the 16-state machine specified by the IEEE 1149.1 specification. Following power up, the TAP controller must be reset by one of following two mechanisms:

- Asynchronous reset – achieved by pulsing or holding TRST_L low
- Synchronous reset – achieved by clocking TCK with five clock pulses while TMS is held or floats High.

This ensures that the boundary scan cells do not block the pin to core connections in theIXF1110.

5.7.3 Instruction Register and Supported Instructions

The instruction register is a 4-bit register that enacts the boundary scan instructions. After the state machine resets, the default instruction is IDCODE. The decode logic in the TAP controller selects the appropriate data register and configures the boundary scan cells for the current instruction. The table below shows the supported boundary scan instructions.

Table 30. Supported Boundary Scan Instructions

Instruction	Code	Description	Data Register
EXTEST	0000	External Test	Boundary Scan
SAMPLE	0001	Sample Boundary	Boundary Scan
HIGHZ	0101	Float Boundary	Bypass
IDCODE	0110	ID Code Inspection	ID
CLAMP	0111	Clamp Boundary	Bypass
BYPASS	1111	1-bit Bypass	Bypass

5.7.4 ID Register

The ID register is a 32-bit register. The IDCODE instruction connects this register between TDI and TDO. Refer toTable 87, "JTAG ID Revision ($ 0x50C)" on page 152 for register bit descriptions.

Note: The four bit version field is stepping dependent. The seven bit Manufacturers ID is the Intel® JEDEC ID less the parity bit per the IEEE 1149.1 specification.

5.7.5 Boundary Scan Register

The boundary scan register is a shift register made up of all the boundary scan cells associated with the device pins. The number, type, and order of the boundary scan cells are specified in the IXF1110 BSDL file. The EXTEST and SAMPLE instructions connect this register between TDI and TDO.

5.7.6 Bypass Register

The bypass register is a one bit register that is used so the IXF110 can be bypassed to reduce the length of the JTAG chain when trying to access other devices on the chain besides the IXF1110. The BYPASS, HIGHZ, and CLAMP instructions connect this register between TDI and TDO.

5.8 Clocks

The IXF1110 has system interface reference clocks, SPI4-2 data path input and output clocks, a JTAG input clock, a I^2C output clock, and an LED output clock. Section 5.8 details the unique clock source requirements.

5.8.1 System Interface Reference Clocks

There are two system interface clocks required by the IXF1110:

5.8.1.1 CLK125

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- +/- 50 ppm
- Maximum duty cycle distortion 40/60

5.8.1.2 CLK50

The other system interface clock supplies the clock source to the SPI4-2 receive circuitry. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- 1/8 frequency of the SPI4-2 data path clock (RDCLK_P/N)
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Range = 40 Mhz to 50 MHz

5.8.2 SPI4-2 Receive and Transmit Data Path Clocks

The SPI4-2 data path clocks are compliant with the OIF 2000.88.4 Specification.

The IXF1110 has the following requirements on the transmit data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable (frequency and level) when reset is removed or when sourced, whichever happens last
- TSCLK frequency is one-quarter TDCLK frequency

The IXF1110 meets the following specifications on the receive data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable when sourced

5.8.3 JTAG Clock

The IXF1110 supports JTAG. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- Maximum clock frequency 11 MHz
- Maximum duty cycle distortion 40/60

5.8.4 I^2C Clock

The IXF1110 device supports a single output I^2C clock to support all 10 optical module interfaces. The IXF1110 meets the following specifications for this clock:

- 2.5 V CMOS drive
- Maximum clock frequency of 100 kHz

5.8.5 LED Clock

The IXF1110 supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 720 Hz.

The IXF1110 supports a serial LED data stream. The IXF1110 meets the following specifications for this clock:

- 2.5 V CMOS drive
- Maximum frequency of 720 Hz
- Maximum duty cycle distortion: 50/50

6.0 Applications

6.1 Power Supply Sequencing

Follow the power-up and power-down sequence described in this section to ensure correct IXF1110 operation. The sequence covers all IXF1110 digital and analog supplies.

Caution: Failure to follow the power-up and power-down sequences will damage the IXF1110.

6.1.1 Power-Up Sequence

Ensure that the 1.8 V supplies (VDD/AVDD1P8_1/AVDD1P8_2) are applied and stable prior to the application of the 2.5 V supplies (VDD2/AVDD2P5_1/AVDD2P5_2).

Caution: If the 2.5 V supplies (VDD2/AVDD2P5_1/AVDD2P5_2) exceed the 1.8 V (VDD/AVDD1P8_1/AVDD1P8_2) supplies by more than 2.0 V during power-up, the ESD structures within the analog I/Os can be damaged.

6.1.2 Power-Down Sequence

The power-down sequence is the reverse of the power-up sequence. Remove the 2.5 V supplies prior to removing the 1.8 V supplies.

Figure 26 and Table 31 provide information on power sequencing.

Note: If the 2.5 V supplies (VDD2/AVDD2P5_1/AVDD2P5_2) exceed the 1.8 V (VDD/AVDD1P8_1/AVDD1P8_2) supplies by more than 2.0 V during power-down, damage can occur to the ESD structures within the analog I/Os.

Figure 26. Power Sequencing

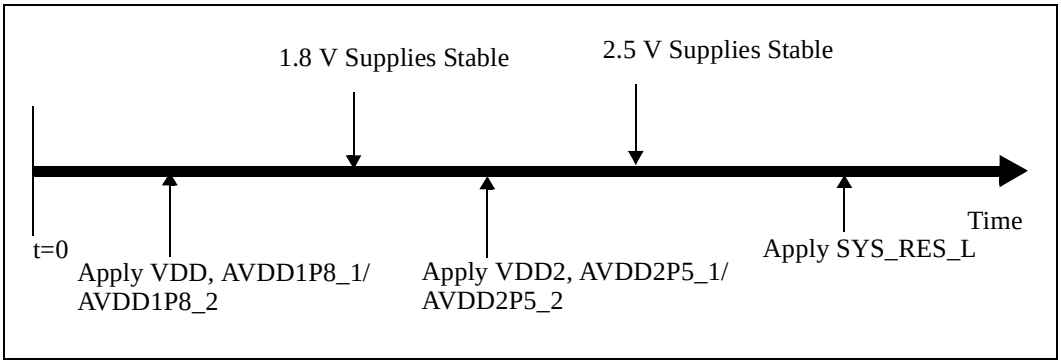


Table 31. Power Sequencing

Power Supply	Power-Up Order	Time Delta to Next Supply[1]	Description
VDD, AVDD1P8_1/ AVDD1P8_2	First	0	1.8 V supplies
VDD2, AVDD2P5_1/ AVDD2P5_2	Second	10 µs	2.5 V supplies

1. The value of 10 µs given is a nominal value only. The exact time difference between the application of the 2.5 V analog supply will be determined by a number of factors dependent on the power management method used.

6.2 Analog Power Filtering

Figure 32 illustrates an analog power supply filter network and Table 32 lists the analog power balls.

Figure 27. Analog Power Supply Filter Network

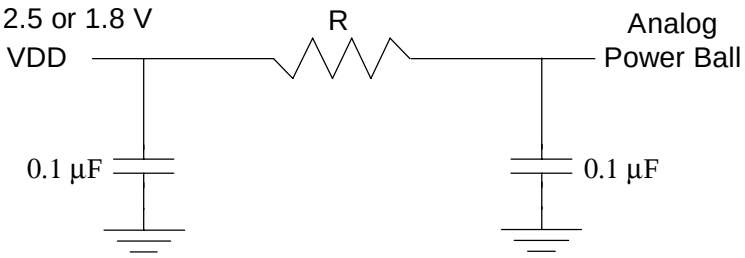


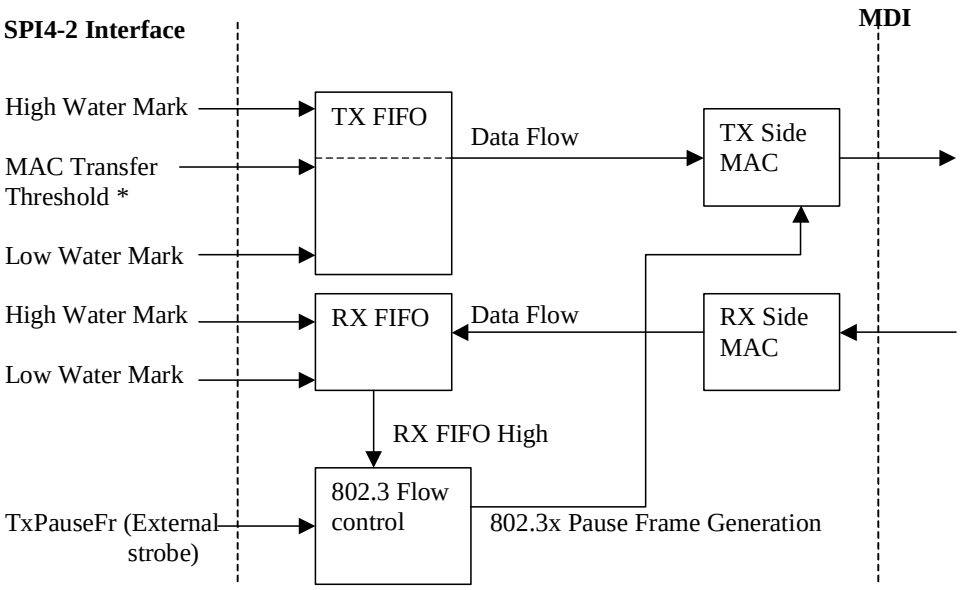
Table 32. Analog Power Balls

Signal Name	Ball Designator	Comments
AVDD1P8_1	D1 E24	Need to provide a filter (see Figure 27). **R:** AVDD1P8_1 and AVDD2P5_1 = 5.6 Ω resistor.
AVDD2P5_1	Y1	
AVDD1P8_2	P7 P18 V6 V11 V14 V18	Need to provide a filter (see Figure 27). **R:** AVDD1P8_2 and AVDD2P5_2 = 1.0 Ω resistor.
AVDD2P5_2	N3 N22 P3 P22 V10 V15	

6.3 TX FIFO and RX FIFO Operation

The Intel® IXF1110 packet buffering is comprised of individual port FIFOs and system-interface FIFOs. Figure 28 illustrates the interaction of these FIFOs.

Figure 28. Packet Buffering FIFO



NOTE: The MAC Transfer Threshold determines when the transmit data is transferred from the TX FIFO to the TX side of the MAC. Once the data has been sent from the TX FIFO to the MAC, it will be transmitted to the PHY and cannot be flow controlled from the link partner.

6.3.1 TX FIFO

The IXF1110 TX FIFOs are implemented with 4.5 KB for each port. This provides enough space for at least one maximum size packet per-port storage and ensures that no under-run conditions occur, assuming that the sending device can supply data at the required data rate.

Note: The TX FIFO High and Low Watermark must be programmed correctly to ensure that the TX FIFO does not overflow.

6.3.1.1 MAC Transfer Threshold

The "TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D)" parameter, which is user programmable, determines when data is transmitted out of the TX FIFO to the MAC. This parameter is configurable for specific block sizes and the user must ensure that an under-run does not occur. The threshold must be set to a value that exceeds the programmed MaxBurst1 parameter from the Network Processor (NPU) or SPI4-2 ASIC. This method of operation eliminates the possibility of under-run, except when the controlling NPU device fails.

The MAC transfer threshold operates on a per packet basis. Once the number of bytes of a packet received in the TX FIFO exceeds the MAC transfer threshold, it will start to be transmitted to the MAC. If the MAC transfer is greater than the packet size, the packet is sent to the MAC once an EOP is received.

The MAC transfer threshold should be set below the Table 94, “TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609)” on page 162. If the MAC transfer threshold is set above the TX FIFO high watermark, the TX FIFO high watermark will act as the MAC transfer threshold. Data is transmitted out of the TX FIFO to the MAC when the TX FIFO high watermark is reached.

6.3.1.2 TX FIFO Relation to the SPI4-2 Transmit FIFO Status (TSTAT)

The amount of data in the TX FIFO dictates the FIFO status sent to the NPU on the TSTAT bus. The following lists how the FIFO status is determined from the TX FIFO High and Low Watermarks.

SATISFIED: The status given for a port when the amount of data in the per port TX FIFO is greater than the programmed “TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609)”.

HUNGRY: The status given for a port when the amount of data in the per port TX FIFO is between the programmed “TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609)” and the “TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613)”.

STARVING: The status given for a port when the amount of data in the per port TX FIFO is below the programmed value in “TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613)”.

Note: The user must ensure the TX FIFO High and Low Watermarks are programmed correctly to ensure no underrrun or overflow occur. Failure to do this may result in packet loss.

6.3.1.3 TX FIFO Drain (IXF1110 Version)

The IXF1110 can allow the SPI4-2 NPU or ASIC to dump data to the IXF1110 while the link is down. This allows the NPU or ASIC to empty its FIFOs, if necessary.

The IXF1110 operates in the following manner under normal operating conditions:

> If the IXF1110 detects that the link is down for a given port, the SPI4-2 interface FIFO status bus indicates SATISFIED. This tells the NPU or ASIC that no data can be passed across the SPI4-2.

The IXF1110 operates in the following the manner when the TX FIFO drain is enabled:

> The SPI4-2 FIFO status bus indicates STARVING for the given port. This tells the NPU or ASIC that it can pass data to the IXF1110 for that port, regardless of the link status, and all data sent to that port will be discarded.

Note: The TX FIFO drain is enabled using the Section 98, “TX FIFO Drain ($0x620)”.

6.3.1.3.1 Enabling the TX FIFO Drain

The TX FIFO drain is enabled using the “TX FIFO Drain ($0x620)”. The following occurs when the TX FIFO drain is enabled for a given port:

- The TX FIFO is held in reset
- The FIFO status for that port indicates SATISFIED
- All data sent to that port is discarded

6.3.1.3.2 Putting the TX FIFO in Drain Mode

Use the TX FIFO drain when the link is down. The following is a step-by-step sequence to put a port(s) into the TX FIFO drain mode:

1. The system detects that link is down for a given port using bits 21:20 of the RX Config Word Register ($Port_Index + 0x16). The SPI4-2 TX FIFO port status is SATISFIED when the link is down.
2. Set the appropriate bit to 1 for the given port in the TX FIFO Drain Register ($0x620) once link is down. This incurs the following:
   a. Enables the drain mode
   b. Causes the TX FIFO for the selected port to enter a reset state
   c. Causes the TX FIFO SPI4-2 FIFO status for that port to change to STARVING.
3. Set the MAC Soft Reset Register bit to 1 for the port(s) that has entered the TX FIFO drain mode.
4. De-assert the MAC Soft Reset Register. Redo the MAC configurations. If applicable, re-enable auto-negotiation for the selected port(s) by setting bit 5 of the Diverse Config Register back to 1.
5. The connected SPI4-2 NPU or ASIC can now dump data to the port(s) that has entered the drain mode. All data sent to the port(s) selected is discarded and not recorded in any register in the IXF1110.
6. Monitor the RX Config Word Register to reestablish link with the link partner. Exit the TX FIFO drain mode when the system software detects link establishment.

6.3.1.3.3 Exiting the TX FIFO Drain Mode

To exit the TX FIFO drain mode.

1. Set the TX FIFO Drain Register bits back to 0. This exits the TX FIFO drain mode and the TX FIFO status bus now indicates the actual TX FIFO status.
2. The IXF1110 is ready to resume normal data transmission.

6.3.2 RX FIFO

The IXF1110 RX FIFOs are provisioned so that each port has its own 17.0 KB memory space. This is enough memory to ensure against an over-run on any port while transferring normal Ethernet frame-size data.

The RX FIFOs are configured by default to automatically generate Pause control frames to initiate the following:

- Halt the link partner when the RX FIFO High Watermark is reached
- Restart the link partner when the data stored in the RXFIFO falls below the Low Watermark.

Pause control frame generation is enabled by default in the "FC Enable ($ Port_Index + 0x12)". Section 8.5.5, "Global RX Block Register Overview" on page 153 documents the registers needed to set the RX FIFO watermarks.

Note: Users should ensure that flow control is enabled to prevent RX FIFO overflows. If an RX FIFO overflow occurs, data is sent out on the SPI4-2 interface regardless of the "RX FIFO Errored Frame Drop Enable ($ 0x59F)" settings. The data is marked with an EOP abort code to inform the upstream device that this data is corrupted.

6.4 Reset and Initialization

When powering up the IXF1110, the hardware reset signal (SYS_RES_L) should be held active Low for a minimum of 100 ns after all of the power rails have fully stabilized to their nominal values and the input clocks have reached their nominal frequency (TDCLK = 400 MHz, CLK125 = 125 MHz, and CLK50 = 50 MHz).

Note: In systems where the SYS_RES_L pin is driven from a single board-wide reset signal, the switch or network processor only comes out of reset at the same time as the IXF1110, or possibly later. This means the TDCLK may not be applied to theIXF1110 when the SYS_RES_L pin is released. However, the system designer must ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency. Failure to apply a stable TDCLK to the IXF1110 can result in the IXF1110 training on a non-stable clock thus causing DIP4 errors and data corruption. This will require a re-training once the TDCLK is stable.

When the TDCLK is applied after the reset pin is released, a built-in feature in the IXF1110 reactivates the internal reset once TDCLK is applied. The IXF1110 extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 4.11 ms after all clocks are stable.

The device is correctly initialized at this point and ready for use. Clocks start to appear at the relevant device ports and the SPI4-2 interface begins to source a training pattern on the receive side while waiting for a training pattern on the transmit side. The SPI4-2 interface synchronizes with the connected switch or network processor per the SPI4-2 Specification.

The CPU accesses can begin to configure the device for any existing user preferences desired.By default, all ports on the IXF1110 are enabled after power-up. The device is ready for use at this time if the default settings are to be used. Otherwise, access the required registers via the CPU interface and configure the control registers to the required settings.

6.4.1 SPI4-2 Initialization

6.4.1.1 RX SPI4-2

After reset or Power-up the RX SPI4-2 interface will start to source training patterns on the data bus to the upstream SPI4-2 device. The IXF1110 will continue to send the training patterns until a valid calendar is sent on RSTAT[1:0] from the upstream device to the IXF1110. At this point, synchronization with the upstream device is complete and the IXF1110 will start to send data once data is available and a credit has been granted from the RSTAT[1:0] bus.

When synchronization is completed, bit 13 of the "SPI4-2 RX Calendar ($ 0x702)" is "1". Before completion, bit 13 is "0", indicating the IXF1110 is sending out training patterns on the RX SPI4-2 data bus.

6.4.1.2 TX SPI4-2

After reset or power-up, the TX SPI4-2 interface outputs a constant framing pattern on TSTAT until it receives the proper SPI4-2 training pattern from the upstream SPI4-2 device. For more information on the required training pattern, see "Dynamic Phase Alignment Training Sequence (Data Path De-skew)" on page 65.

Note: If TDCLK is applied to the IXF1110 after the device has come out of reset, the system designer must ensure the TDCLK is stable when applied. Failure to due so can result in the IXF1110 training on a non-stable clock, causing DIP4 errors and data corruption.

Once the valid training pattern is received and the IXF1110 outputs a 10-port calendar on TSAT, bit 12 of the "SPI4-2 RX Calendar ($ 0x702)" on page 173 will be set. This indicates that synchronization on the TX SPI4-2 is complete.

Ports will show a SATISFIED status on the SPI4-2 TSTAT bus until a valid link is established for that port. To determine if a valid link is established, see "Fiber Operation" on page 50.

6.4.1.3 SerDes

After reset or power-up the SerDes interface will start to output idles on the TX_P/N for forced mode operation. If Auto-Negotiation mode is required bit 5 of the "Diverse Config ($ Port_Index + 0x18)" on page 137 must be set. A link is established when the RX SerDes has received the appropriate code words from the link partner. Refer to "Fiber Operation" on page 50 for more information.

6.4.1.4 CPU

The CPU interface is ready for operation after power-up or reset. Through this interface, the user can configure the device for any desired setting from the defaults. (Refer to "CPU Interface" on page 87 for more information.)

6.5 SerDes Power-Down Capabilities

The IXF1110 has the ability to power down the TX and RX SerDes individually on each port (see Section 5.3, "SerDes Interface" on page 70). Use the following sequence to correctly power up and power down the SerDes ports.

Note: These sequences must be followed to ensure a port correctly operates when brought out of a power-down mode:

6.5.1 Placing the SerDes Port in Power-Down Mode

1. Disable the port(s) by de-asserting the appropriate bit(s) in the "Port Enable ($ 0x500)"
2. Power-down "SerDes TX and RX Power-Down Ports 0-9 ($ 0x787)"
3. The SerDes port is now powered down and the TSAT Status for the port is SATISFIED

6.5.2 Bringing the SerDes Port Out of Power-Down Mode

1. Power up TX and RX SerDes
2. Enable the port(s) by de-asserting the appropriate bit(s) in the "Port Enable ($ 0x500)"
3. Enable auto-negotiation (if applicable). The device defaults to forced mode if it is not enabled.
4. Once a valid link is established, the TSTAT status bus for that port changes from SATISFED to STARVING.

6.6 IXF1110 Unused Ports

Intel recommends the following be used to disable an unused port. The SPI4-2 TSTAT status bus will always reflect status for ten ports regardless of the number of IXF1110 unused ports. Any port which is disabled will have a constant status of SATISFIED. RSTAT must also be input to reflect the status of all ten ports regardless of how many are disabled.

1. Disable ports by setting the appropriate bits in the "Port Enable ($ 0x500)".
2. Power down SerDes for the unused port by setting the appropriate bits in the "SerDes TX and RX Power-Down Ports 0-9 ($ 0x787)"
3. TX SerDes pairs can be left unconnected.
4. RX SerDes pairs should be connected to ground

6.7 Optical Module Connections to the IXF1110

6.7.1 SFP-to-IXF1110 Connection

The IXF1110 SerDes and Optical Module interfaces allow system designers to connect the IXF1110 to various optical transceivers. When using Small Form Factor Pluggable (SFP) optical transceivers to connect to the IXF1110, all SerDes and Optical Module status pins are used. Use Figure 29, "SFP-to-IXF1110 Connection" and Table 33, "SFP-to-IXF1110 Connection" to connect an SFP to the IXF1110.

Figure 29. SFP-to-IXF1110 Connection

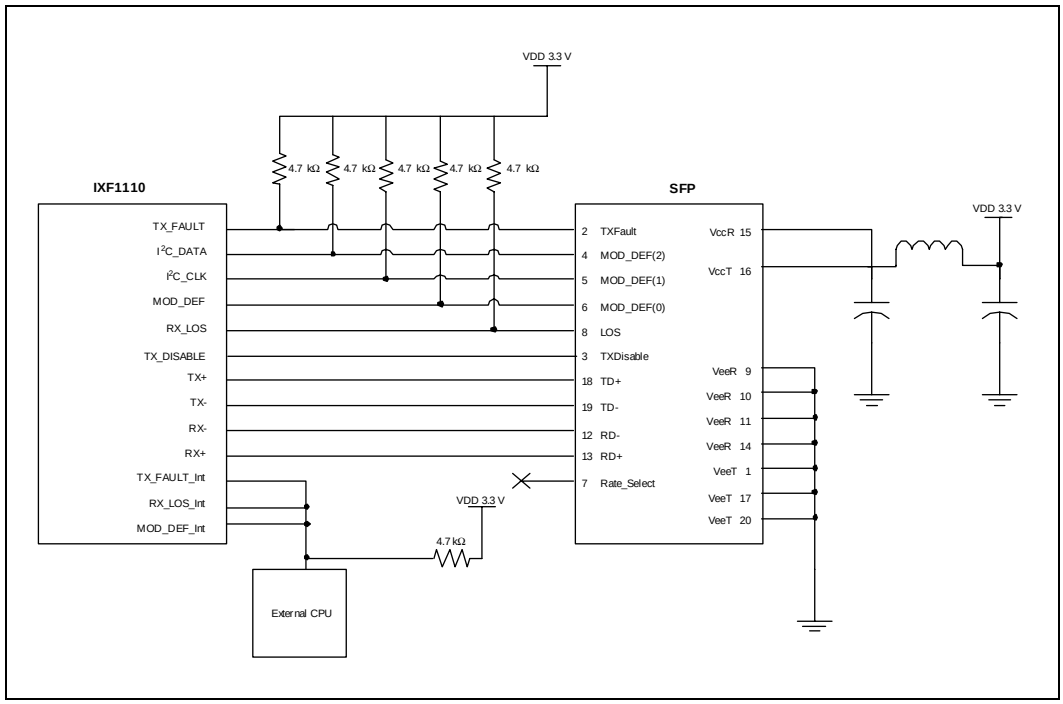


Table 33. SFP-to-IXF1110 Connection (Sheet 1 of 2)

SFP Pin #	SFP Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
1	VeeT	NA	NA	Connect to ground.
2	TxFault	M24, V23, Y17, R15, W14, W11, W9, AC5, P8, L2	TX_FAULT_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
3	TxDisable	K22, M22, AC22, U18, U14, AA18, U9, AA9, V7, L4	TX_DISABLE_[0:9]	SFP module has internal pull-up.
4	MOD_DEF (2)	G22, G23, J24, F22, E23, H24, G20, E22, G24, F24	I^2C_DATA_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
5	MOD_DEF (1)	L19	I^2C_CLK	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
6	MOD_DEF (0)	N24, Y21, AA16, M20, AC14, U11, T4, AB2, R7, L1	MOD_DEF_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
7	Rate Select	NA	NA	Leave floating.
8	LOS	L22, V17, AD18, R12, AB15, V12, Y9, AC3, T2, P2	RX_LOS_[0:9]	Use an external 4.7 kΩ pull-up resistor to 3.3 V.
9	VeeR	NA	NA	Connect to ground.
10	VeeR	NA	NA	Connect to ground.
11	VeeR	NA	NA	Connect to ground.

Table 33. SFP-to-IXF1110 Connection (Sheet 2 of 2)

SFP Pin #	SFP Pin Name	IXF1110 Pin # 0:9	IXF1110 Pin Name	Description
12	RD-	U22, U20, T24, V24, AB14, AD14, AC16, AD15, V4, Y5	RX_N_[0:9]	The IXF1110 has a 100 Ω differential termination on the chip that requires it to be AC-coupled. AC-coupling is done inside the SFP module and is not required on the host board.
13	RD+	T22, T20, U24, W24, AB13, AD13, AB16, AD16, V5, Y6	RX_P_[0:9]	
14	VeeR	NA	NA	Connect to ground.
15	VccR	NA	NA	Connect to filtered 3.3 V.
16	VccT	NA	NA	Connect to filtered 3.3 V.
17	VeeT	NA	NA	Connect to ground.
18	TD+	V20, Y19, V22, Y23, AB12, AD12, AB9, AD9, T3, T5	TX_P_[0:9]	These pins are the differential transmitter inputs. They are AC-coupled differential lines with 100 Ω differential termination inside the SFP module. The AC-coupling is done inside the SFP module and is not required on the host board.
19	TD-	V21, Y20, W22, Y22, AB11, AD11, AC9, AD10, U3, U5	TX_N_[0:9]	
20	VeeT	NA	NA	Connect to ground.
N/A	N/A	B11	TX_FAULT_Int	Connect to Interrupt Service Routine. Use an external 4.7 kΩ pull-up resistor to 3.3 V.
N/A	N/A	B14	RX_LOS_Int	Connect to Interrupt Service Routine. Use an external 4.7 kΩ pull-up resistor to 3.3 V.
N/A	N/A	G15	MOD_DEF_Int	Connect to Interrupt Service Routine. Use an external 4.7 kΩ pull-up resistor to 3.3 V.

7.0 Electrical Specifications

Table 34 through Table 49 on page 121 and Figure 30 on page 109 through Figure 41 on page 121 represent the target specifications of the following IXF1110 interfaces:

- "CPU Timing Specification"
- "JTAG Timing Specification"
- "Transmit Pause Control Timing Specifications"
- "Optical Module Interrupt and I2C Timing Specification"
- "System Timing Specifications"
- "LED Timing Specifications"
- "SerDes Timing Specification"
- "SPI4-2 Timing Specifications"

Note: These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 36 through Table 49 on page 121 apply over the recommended operating conditions specified in Table 34.

Table 34. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage		VDD	-0.3	2.4	Volts
		AVDD1P8_1/ AVDD1P8_2	-0.3	2.4	Volts
		VDD2	-0.3	3.0	Volts
		AVDD2P5_1/ AVDD2P5_2	-0.3	3.0	Volts
Operating Temperature	Ambient	TOPA	-15	+85	°C
	Case	TOPC	–	+130	°C
Storage Temperature		TST	-65	+125	°C
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.					

Table 35. Operating Conditions

Parameter		Symbol	Min	Typ[1]	Max	Units
Recommended Supply Voltage		VDD, AVDD1P8_1, AVDD1P8_2	1.71	1.80	1.89	Volts
		VDD2, AVDD2P5_1, AVDD2P5_2	2.375	2.50	2.625	Volts
Operating Current	1000BASE-SX	IDD and AIDD1P8_1, AIDD1P8_2	–	2.31	2.75	Amps
		IDD2 and AIDD2P5_1, AIDD2P5_2	–	0.310	0.42	Amps
Recommended Operating Temperature[2]	Ambient	TOPA	0	–	70	°C
	Case with Heat Sink	TOPC-HS	0	–	119	°C
	Case without Heat Sink	TOPC-NHS	0	–	118	°C
Recommended Storage Temperature		TOST	-65	–	40	°C
Power Consumption	1000BASE-SX full-duplex all ports enabled and passing data	P	–	4.9	6.3	Watts
	1000BASE-SX full-duplex six ports enabled and passing data	P	–	4.5	5.2	Watts

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Refer to the Intel® IXF1110 Thermal Design Guidelines (document number 250289).

7.1 DC Specifications

Table 36. 2.5 V LVTTL and CMOS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	–	–	0.70	V	VCC = MIN
Input High Voltage[2]	V_{IH}	1.7	–	3.6	V	VCC = MIN
Output Low Voltage	V_{OL}	–	–	0.40	V	VCC = MIN, IOL = 3.9 mA
Output High Voltage	V_{OH}	2.0	–	–	V	VCC = MIN, IOH = -2.9 mA
Output Leakage Current	I_{OZ}	–	–	10	µA	VCC = MAX

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 3.3 V CMOS tolerant.

Table 37. LVDS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Range	VI	-0.20	–	VddMax+ 0.20	V	–
Differential Input Voltage	|VID|	100	–	–	mV	@ 400 MHz
Input Common-Mode Current	ICM	–	–	–	µA	LVDS Input VOS = 1.2 V
Threshold Hysteresis	TH	25	–	–	mV	–
Differential Input Impedance	R_{IN}	85	100	115	Ω	Typical 100 Ω
Output Low Voltage	V_{OL}	0.95	–	–	V	–
Output High Voltage	V_{OH}	–	–	1.51	V	–
Differential Output Voltage	|VOD|	330	–	446	mV	–
Delta Differential Output Voltage (Complementary States)	Δ|VOD|	–	–	25	mV	–
Offset (Common-Mode) Voltage	VOS	1.12	–	1.30	V	–
Output Leakage Current	IOZ	–	–	10	µA	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.2 Undershoot/Overshoot Specifications

The overshoot figures given in this section represent the maximum voltage that can be applied without affecting the reliability of the device (see Table 38).

Caution: Exceeding these values will damage the device.

Table 38. Undershoot/Overshoot Limits

Ball Type	Undershoot	Overshoot
2.5 V CMOS	-0.60 V	3.9 V
2.5 V LVTTL	-0.60 V	3.9 V

7.3 CPU Timing Specification

Figure 30. CPU Port Read Timing

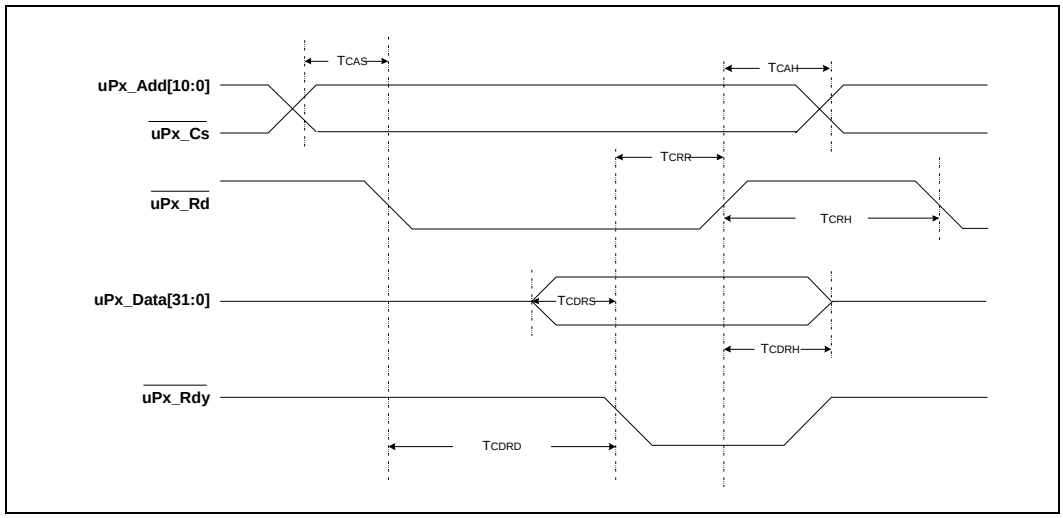


Figure 31. CPU Port Write Timing

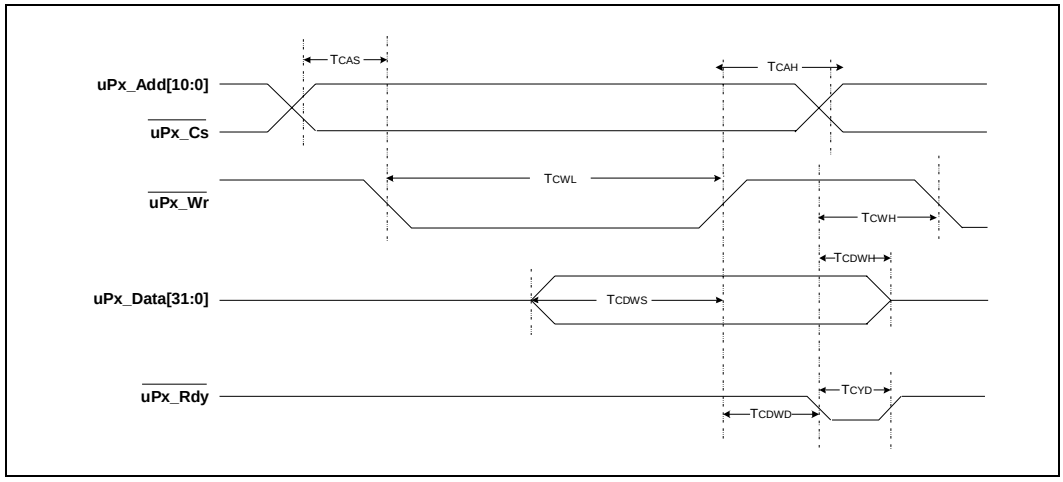


Table 39. CPU Timing Parameters (Sheet 1 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
UPX_ADD[12:0], UPX_CS_L Setup Time	TCAS	10	–	–	ns	–
UPX_ADD[12:0], UPX_CS_L Hold Time	TCAH	10	–	–	ns	–
UPX_RDY_L Assertion to UPX_RD_L De-assertion	TCRR	10	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 39. CPU Timing Parameters (Sheet 2 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
UPX_RD_L High Width	TCRH	24 (3x cycle)	–	–	ns	–
UPX_DATA[31:0] to UPX_RDY_L Setup Time	TCDRS	10	–	–	ns	–
UPX_DATA[31:0] to UPX_RD_L Hold Time	TCDRH	8	–	32	ns	–
Read UPX_DATA[31:0] Driving Delay	TCDRD	24	–	355	ns	–
UPX_WR_L Width	TCWL	40	–	–	ns	–
UPX_RDY_L to UPX_WR_L Hold Time	TCWH	16	–	–	ns	–
UPX_DATA[31:0] to UPX_WR_L Setup Time	TCDWS	10	–	–	ns	–
UPX_RDY_L to UPX_DATA[31:0] Hold Time	TCDWH	10	–	–	ns	–
UPX_DATA[31:0] Latching Delay	TCDWD	8	–	40	ns	–
UPX_RDY_L Width in Write Cycle	TCYD	24	–	40	ns	–
Read UPX_RDY_L de-assertion to UPX_WR_L Assertion	TRTW	32	–	–	ns	–
Write UPX_RDY_L de-assertion to UPX_RD_L Assertion	TWTR	32	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

7.4 JTAG Timing Specification

Figure 32. JTAG Timing

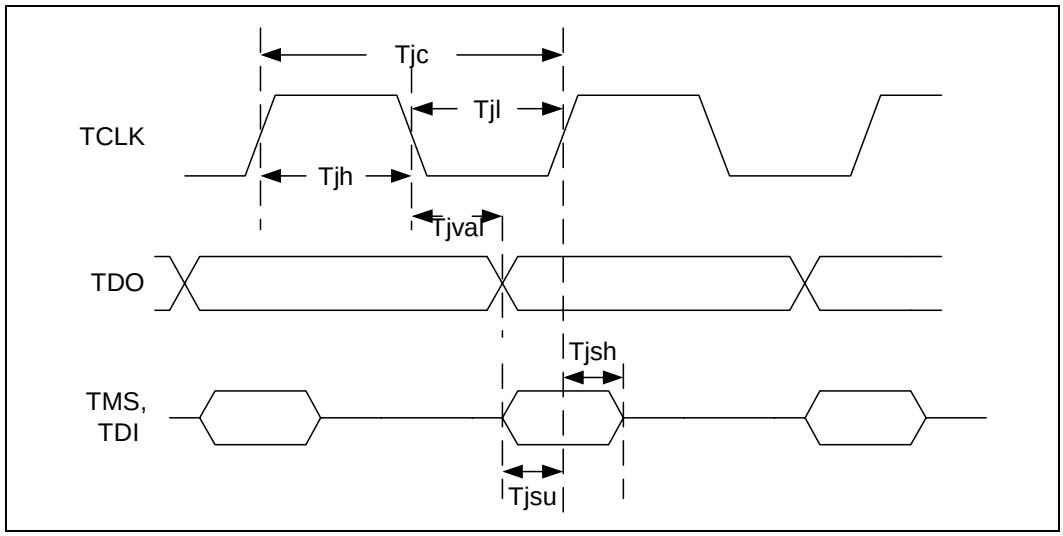


Table 40. JTAG Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TCLK Cycle Time	T_{JC}	90	–	–	ns	–
TCLK High Time	T_{JH}	0.4 x T_{JC}	–	0.6 x T_{JC}	ns	–
TCLK Low Time	T_{JL}	0.4 x T_{JC}	–	0.6 x T_{JC}	ns	–
TCLK Falling Edge to TDO Valid	T_{JVAL}	–	–	25	ns	–
TMS/TDI Setup to TCLK	T_{JSU}	20	–	–	ns	–
TMS/TDI Hold from TCLK	T_{JSH}	5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.5 Transmit Pause Control Timing Specifications

Figure 33. Transmit Pause Control Interface

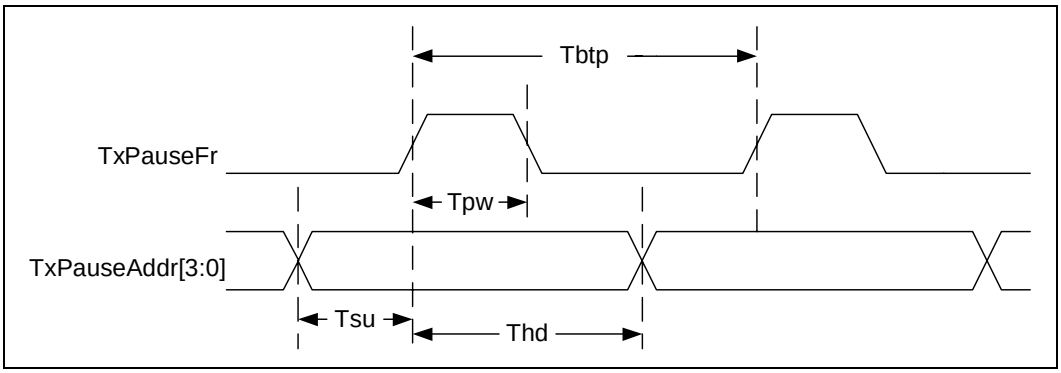


Table 41. Transmit Pause Control Interface Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TXPAUSEFR Width	TPW	16	–	–	ns	–
TXPAUSEADDR[3:0] Setup to TXPAUSEFR	TSU	16	–	–	ns	–
TXPAUSEADDR[3:0] Hold from TXPAUSEFR	THD	32	–	–	ns	–
TXPAUSEFR Pulse to Pulse	TBTP	48	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.6 Optical Module Interrupt and I²C Timing Specification

Figure 34. Optical Module Interrupt Timing

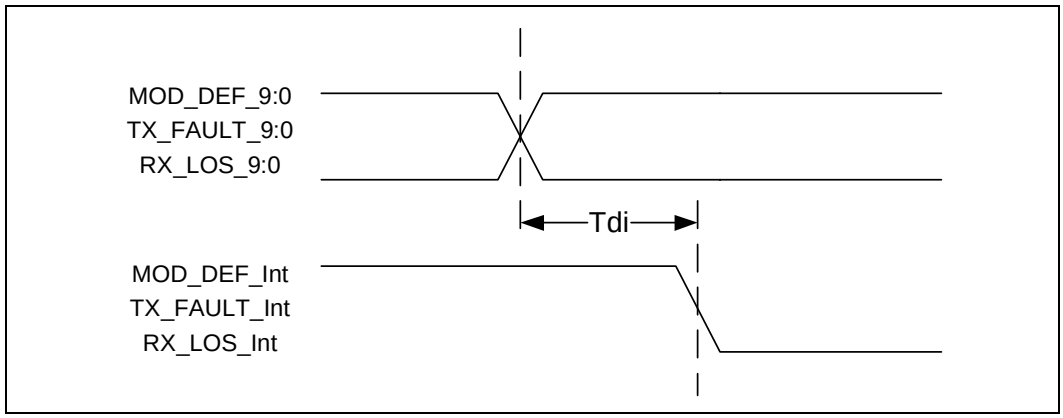


Table 42. Optical Module Interrupt Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Change of state on MOD_DEF_9:0 or TX_FAULT_9:0 or RX_LOS_9:0 to assertion (active Low) on MOD_DEF_Int or TX_FAULT_Int or RX_LOS_Int	TDI	24	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 35. I²C Bus Timing

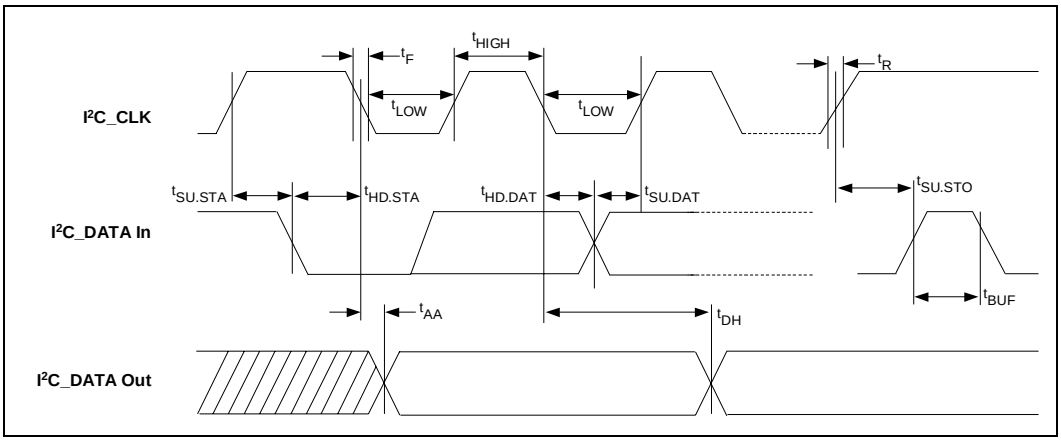


Figure 36. I²C Write Cycle

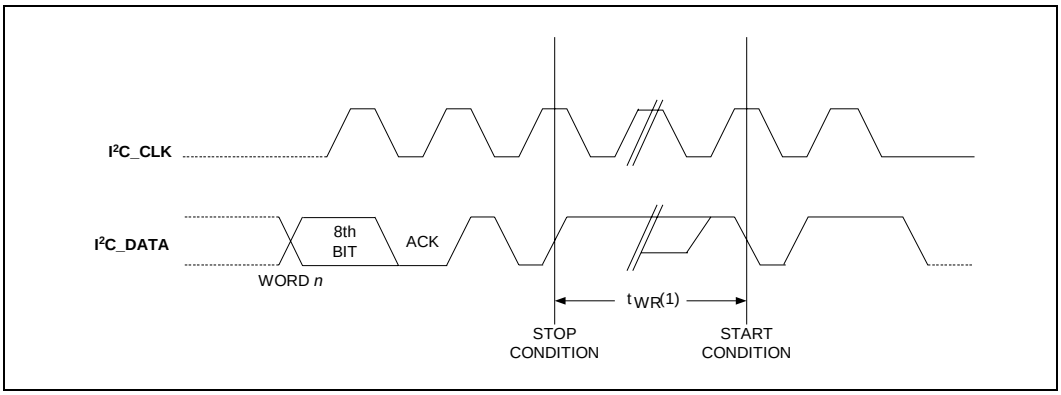


Table 43. I²C AC Timing Characteristics (Sheet 1 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Clock Frequency, SCL	f_{SCL}	–	–	100	kHz	–
Clock Pulse Width Low	t_{LOW}	4.7	–		µs	–
Clock Pulse Width High	t_{HIGH}	4.0	–		µs	–
Noise Suppression	t_I	–	–	100	ns	–
Clock Low to Data Valid Out	t_{AA}	0.1	–	4.5	µs	–
Time bus must be free before a new transmission starts	t_{BUF}	4.7	–	–	µs	–
Start Hold Time	$t_{HD.STA}$	4.0	–	–	µs	–
Start Setup Time	$t_{SU.STA}$	4.7	–	–	µs	–
Data In Hold Time	$t_{HD.DAT}$	0	–	–	µs	–
Data In Setup time	$t_{SU.DAT}$	200	–	–	ns	–
Inputs Rise Time	t_R	–	–	1.0	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 43. I²C AC Timing Characteristics (Sheet 2 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Inputs Fall Time	t_F	–	–	300	ns	–
Stop Setup Time	$t_{SU.STO}$	4.7	–	–	µs	–
Data Out Hold Time	t_{DH}	100	–	–	ns	–
Write Cycle Time	t_{WR}	–	–	10	ms	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.7 System Timing Specifications

Figure 37. Hardware Reset Timing

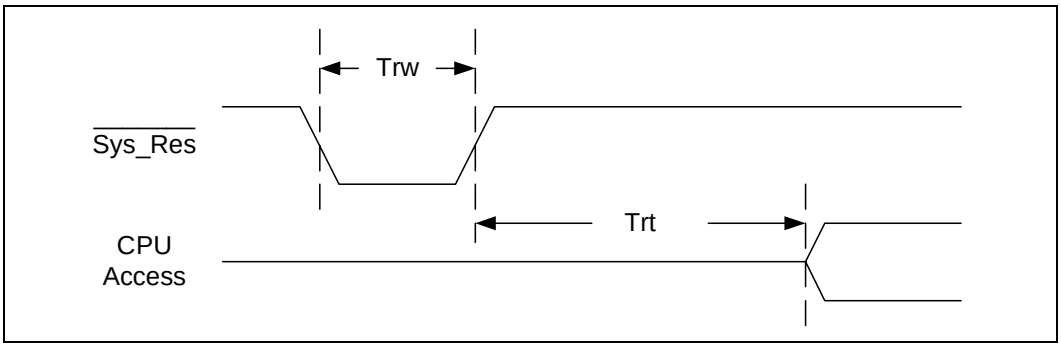


Table 44. Hardware Reset Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Reset Pulse Width	TRW	100	–	–	ns	–
Reset Recovery Time	TRT	4.11	–	–	ms	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.8 LED Timing Specifications

Figure 38. LED Timing

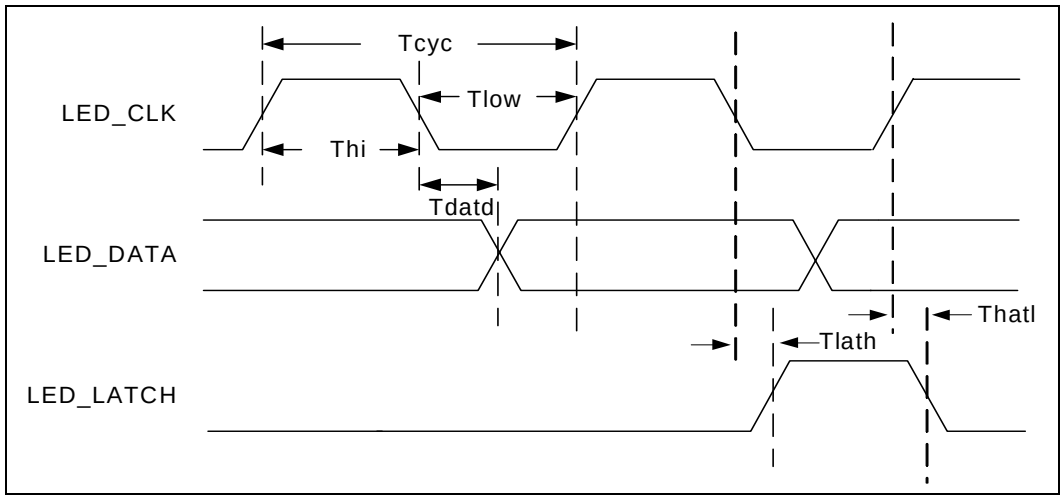


Table 45. LED Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions[2]
LED_CLK Cycle Time	TCYC	1.36	–	1.40	ms	–
LED_CLK High Time	THI	680	–	700	µs	50% duty cycle
LED_CLK Low Time	TLOW	680	–	700	µs	50% duty cycle
LED_CLK Falling Edge to LED_DATA Valid	TDATD	2	–	5	ns	–
LED_CLK Rising Edge to LED_LATCH Falling Edge	THATL	690	–	700	µs	–
LED_CLK Falling Edge to LED_LATCH Rising Edge	TLATH	690	–	700	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Flash Rate = 100 ms, LED Mode 1.

7.9 SerDes Timing Specification

Table 46 specifies the transmit electrical specifications based on a recommended 1.8 V AVDD1P8_1 and AVDD1P8_2 termination voltage and the required 50 Ω termination and Table 46 specifies the receiver electrical specifications based on a recommended 1.8 V AVDD1P8_1 and AVDD1P8_2 termination voltage. Figure 39 illustrates the timing requirements for the IXF1110 transmit and receive SerDes signals.

Note: It is essential that both positive and negative drive levels at the receiver input maintain a minimum voltage of 0.8 V relative to ground to help ensure proper circuit operation.

Figure 39. SerDes Timing

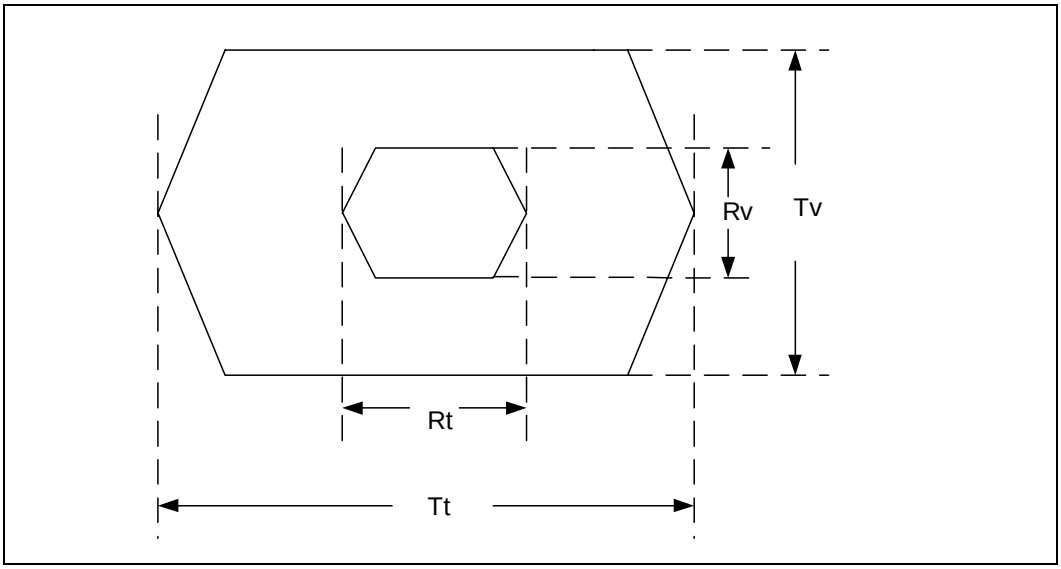


Table 46. Transmitter Characteristics (Sheet 1 of 2)

Parameter	Symbol	Normalized Power Driver Setting	Min	Typ[1]	Max	Units	Test Conditions
Transmit differential signal level	T_V	0.50	180	230	325	mVpp diff	AVDD1P8_1 and AVDD1P8_2 terminated to 1.8 V; R_{LOAD} = 50 Ω;
		1.00	350	440	700		
		1.33	425	580	900		
		2.00	600	770	1050		
Transmitter Common Mode Voltage Range	–	0.50	1300	1600	1940	mV	–
		1.00	1000	1400	1870		
		1.33	800	1300	1825		
		2.00	700	1100	1760		
Transmit Eye Width	T_T	1.00	800	–	–	pS	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

NOTE: Refer to Table 21, “SerDes Driver TX Power Levels” on page 71 for valid SerDes power levels.

Table 46. Transmitter Characteristics (Sheet 2 of 2)

Parameter	Symbol	Normalized Power Driver Setting	Min	Typ[1]	Max	Units	Test Conditions
Differential signal rise/fall time	–	1.00	60	96	132	pS	R_{LOAD} = 50 Ω; 20% to 80% max
Differential Output Impedance	–		60	100	150	Ω diff	DC
Transmitter short circuit current	–		-100	–	100	mA	–
Transmitter Frequency	–		1.249875	1.25	1.250125	GHz	Reference Oscillator 125 MHz +/- 100 ppm
Total Transmitter output jitter	–				122	pS p-p	Total Jitter at BER 1E-12

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

NOTE: Refer to Table 21, "SerDes Driver TX Power Levels" on page 71 for valid SerDes power levels.

Table 47. Receiver Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receiver differential voltage requirement at center of receive-eye	R_V	200	–	–	mVp-p diff	–
Receiver common mode voltage range		900	1275	1650	mV	–
Receive Eye Width	R_T	280	–	–	pS	–
Receiver termination impedance	–	40	–	62.5	Ω	–
Signal detect level	–	125	–	400	mVp-p diff	–
Total Receiver jitter tolerance	–	–	–	600	pS p-p	Total Jitter at BER 1E-12

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.10 SPI4-2 Timing Specifications

Figure 40. SPI4-2 Transmit FIFO Status Bus Timing

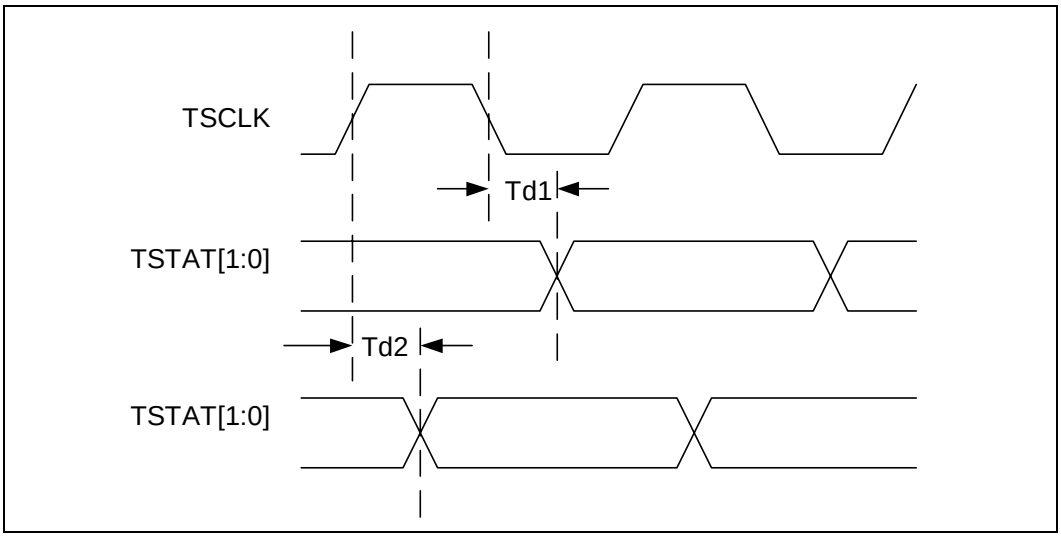


Table 48. SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TSCLK Falling Edge to TSTAT[1:0] Valid (Active edge flipped to falling)	T_{D1}	–	–	280	pS	–
TSCLK Rising Edge to TSTAT[1:0] Valid (Default operation)	T_{D2}	–	–	280	pS	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 41. SPI4-2 Receive FIFO Status Bus Timing

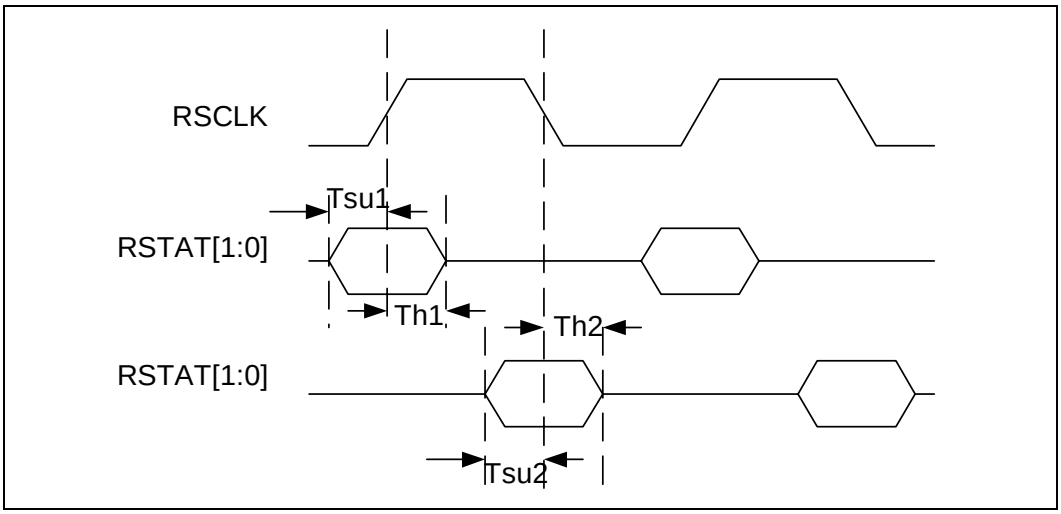


Table 49. SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RSTAT[1:0] Setup to RSCLK Rising Edge (Default operation)	TSU1	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Rising Edge (Default operation)	TH1	0.5	–	–	ns	–
RSTAT[1:0] Setup to RSCLK Falling Edge (When active edge flipped to falling)	TSU2	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Falling Edge (When active edge flipped to falling)	TH2	0.5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 50. SPI4-2 LVDS Rise/Fall Times

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Rise/Fall at source	RTsrc	–	–	0.2	ns	400 Mhz operation – measured using conditions set forth in ANSI/TIA/EIA-644-A-2001
Rise/Fall at sink	RTsnk	–	–	0.4	ns	400 Mhz operation – measured using conditions set forth in ANSI/TIA/EIA-644-A-2001

8.0 Register Definitions

8.1 Introduction

This section provides information on the location and functionality of the IXF1110 Control and Status Registers.

8.2 Document Structure

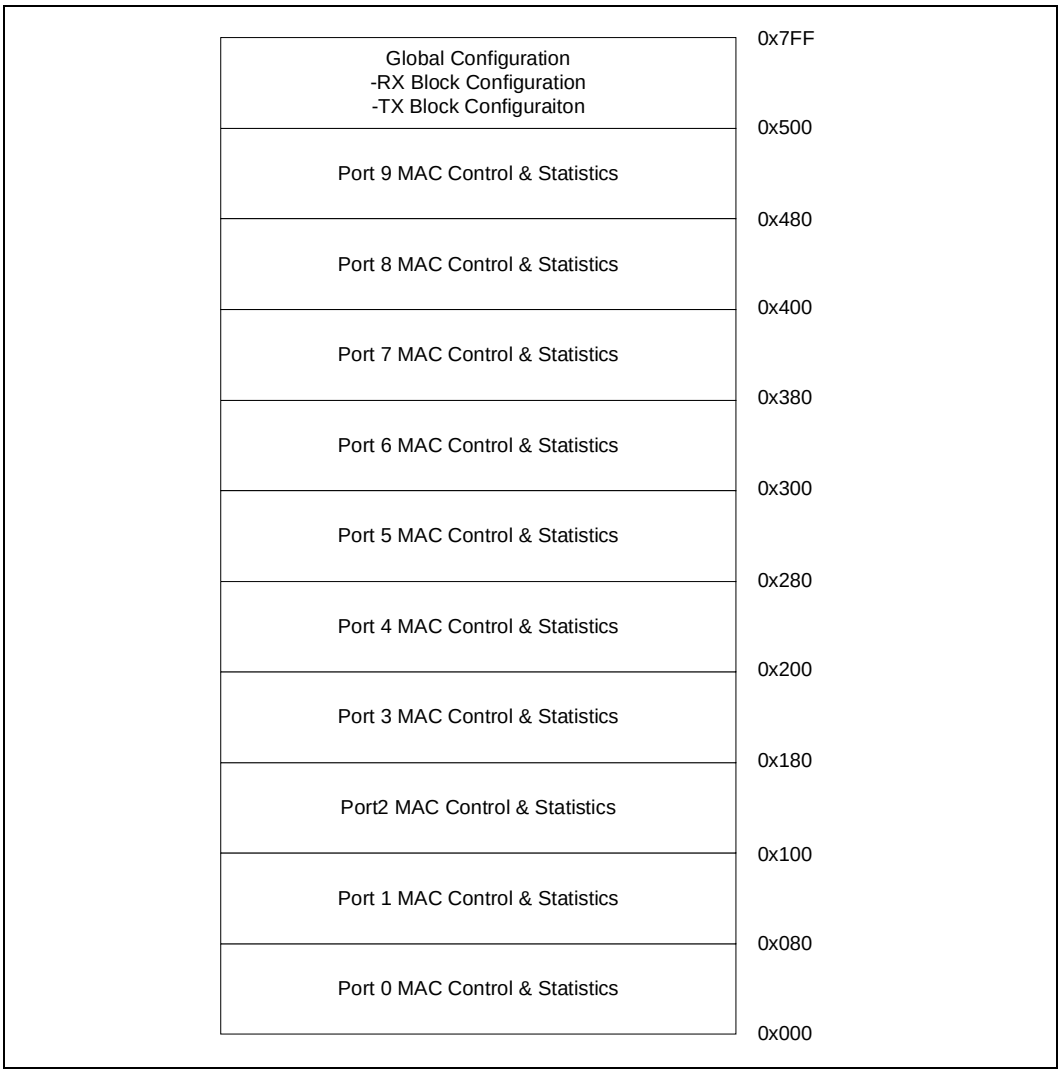
This document is structured to give a general overview of the register map and an in-depth description of each bit of a register in later sections.

8.3 Graphical Representation

Figure 42 represents an overview of the IXF1110 Global Control Status Registers that are used to configure or report on all ports.

Caution: Do not write to any reserved register unless specified. Writing to a reserved register address may cause improper device operation.

Figure 42. Memory Overview

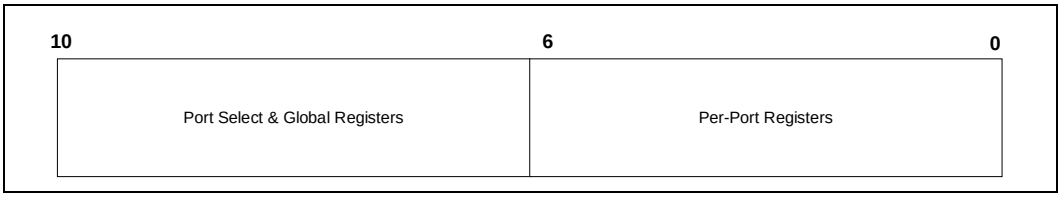


8.4 Per Port Registers

The following section covers all of the registers that are replicated in each of the 10 ports in the IXF1110. These registers perform an identical function in each port.

The address vector for the IXF1110 is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 43.

Figure 43. Register Overview



8.5 Memory Map

Table 51 through Table 59 on page 131 provide theIXF1110memory maps. A number of global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All registers in the IXF1110 are 32 bits.

Table 51. MAC Control Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
“Station Address Low ($ Port_Index + 0x00)”	32	R/W	132	0x00
“Station Address High ($ Port_Index + 0x01)”	32	R/W	132	0x01
Reserved	32	RO	–	0x02
“FDFC Type ($ Port_Index + 0x03)”	32	R/W	132	0x03
Reserved	32	R	–	0x04
Reserved	32	RO	–	0x05
Reserved	32	RO	–	0X06
“FC TX Timer Value ($ Port_Index + 0x07)”	32	R/W	132	0x07
“FDFC Address Low ($ Port_Index + 0x08)”	32	R/W	133	0x08
“FDFC Address High ($ Port_Index + 0x09)”	32	R/W	133	0x09
Reserved	32	R	–	0x0A
Reserved	32	R	–	Ox0B
“IPG Transmit Time ($ Port_Index + 0x0C)”	32	R/W	133	0x0C
Reserved	32	R/W	--	0x0D

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 51. MAC Control Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
“Pause Threshold ($ Port_Index + 0x0E)”	32	R/W	134	0x0E
“Max Frame Size ($ Port_Index + 0x0F)”	32	R/W	134	0x0F
Reserved	32	RO	–	0x10
Reserved	32	RO	–	0x11
“FC Enable ($ Port_Index + 0x12)”	32	R/W	135	0x12
Reserved	32	RO	–	0x13-0x14
“Discard Unknown Control Frame ($ Port_Index + 0x15)”	32	R/W	135	0x15
“RX Config Word ($ Port_Index + 0x16)”	32	R/W	135	0x16
“TX Config Word ($ Port_Index + 0x17)”	32	R/W	136	0x17
“Diverse Config ($ Port_Index + 0x18)”	32	R/W	137	0x18
“RX Packet Filter Control ($ Port_Index + 0x19)”	32	R/W	138	0x19
“Port Multicast Address Low ($ Port_Index + 0x1A)”	32	R/W	139	0x1A
“Port Multicast Address High ($ Port_Index + 0x1B)”	32	R/W	139	0x1B
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 52. MAC RX Statistics Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RXOctetsTotalOK	32	CoR	140	0x20
RXOctetsBAD	32	CoR	140	0x21
RXUCPckts	32	CoR	140	0x22
RXMCPkts	32	CoR	140	0x23
RXBCPkts	32	CoR	140	0x24
RXPkts64Octets	32	CoR	140	0x25
RXPkts65to127Octets	32	CoR	140	0x26
RXPkts128to255Octets	32	CoR	140	0x27
RXPkts256to511Octets	32	CoR	140	0x28
RXPkts512to1023Octets	32	CoR	140	0x29
RXPkts1024to1518Octets	32	CoR	140	0x2A
RXPkts1519toMaxOctets	32	CoR	140	0x2B
RXFCSErrors	32	CoR	140	0x2C
RXTagged	32	CoR	140	0x2D
RXDataError	32	CoR	140	0x2E
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 52. MAC RX Statistics Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RXAlignErrors	32	CoR	140	0x2F
RXLongErrors	32	CoR	140	0x30
RXJabberErrors	32	CoR	140	0x31
RXPauseMacControlCounter	32	CoR	140	0x32
RXUnknownMacControlFrameCounter	32	CoR	140	0x33
RXVeryLongErrors	32	CoR	140	0x34
RXRuntErrors	32	CoR	140	0x35
RXShortErrors	32	CoR	140	0x36
RXCarrierExtendError	32	CoR	140	0x37
RXSequenceErrors	32	CoR	140	0x38
RXSymbolErrors	32	CoR	140	0x39
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 53. MAC TX Statistics Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC TX Statistics Registers (Port Index + Offset)				
TXOctetsTotalOK	32	CoR	144	0x40
TXOctetsBad	32	CoR	144	0x41
TXUCPkts	32	CoR	144	0x42
TXMCPkts	32	CoR	144	0x43
TXBCPkts	32	CoR	144	0x44
TXPkts64Octets	32	CoR	144	0x45
TXPkts65to127Octets	32	CoR	144	0x46
TXPkts128to255Octets	32	CoR	144	0x47
TXPkts256to511Octets	32	CoR	144	0x48
TXPkts512to1023Octets	32	CoR	144	0x49
TXPkts1024to1518Octets	32	CoR	144	0x4A
TXPkts1519toMaxOctets	32	CoR	144	0x4B
TXDeferred	32	CoR	144	0x4C
TXTotalCollisions	32	CoR	144	0x4D
TXSingleCollisions	32	CoR	144	0x4E
TXMultipleCollisions	32	CoR	144	0x4F
TXLateCollisions	32	CoR	144	0x50
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 53. MAC TX Statistics Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC TX Statistics Registers (Port Index + Offset)				
TXExcessiveCollisionErrors	32	CoR	144	0x51
TXExcessiveDeferralErrors	32	CoR	144	0x52
TXExcessiveLengthDrop	32	CoR	144	0x53
TXUnderrun	32	CoR	144	0x54
TXTagged	32	CoR	144	0x55
TXCRCError	32	CoR	144	0x56
TXPauseFrames	32	CoR	144	0x57
TXFlowControlCollisionsSend	32	CoR	144	0x58
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 54. Global Status and Configuration Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Global Status and Configuration Registers				
“Port Enable ($ 0x500)”	32	R/W	148	0x500
Reserved	32	R	–	0x501
“Link LED Enable ($ 0x502)”	32	R/W	149	0x502
Reserved	32	RO	–	0x503
“Core Clock Soft Reset ($ 0x504)”	32	R/W	149	0x504
“MAC Soft Reset ($ 0x505)”	32	R/W	150	0x505
Reserved	32	RO	–	0x506
Reserved	32	R	–	0x507
“CPU Interface ($ 0x508)”	32	R/W	150	0x508
“LED Control ($ 0x509)”	32	R/W	151	0x509
“LED Flash Rate ($ 0x50A)”	32	R/W	151	0x50A
“LED Fault Disable ($ 0x50B)”	32	R/W	151	0x50B
“JTAG ID Revision ($ 0x50C)”	32	R/W	152	0x50C
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 55. RX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
RX Block Registers				
RX FIFO High Watermark Port 0	32	R/W	153	0x580
RX FIFO High Watermark Port 1	32	R/W	153	0x581
RX FIFO High Watermark Port 2	32	R/W	153	0x582
RX FIFO High Watermark Port 3	32	R/W	153	0x583
RX FIFO High Watermark Port 4	32	R/W	153	0x584
RX FIFO High Watermark Port 5	32	R/W	153	0x585
RX FIFO High Watermark Port 6	32	R/W	153	0x586
RX FIFO High Watermark Port 7	32	R/W	153	0x587
RX FIFO High Watermark Port 8	32	R/W	153	0x588
RX FIFO High Watermark Port 9	32	R/W	153	0x589
RX FIFO Low Watermark Port 0	32	R/W	154	0x58A
RX FIFO Low Watermark Port 1	32	R/W	154	0x58B
RX FIFO Low Watermark Port 2	32	R/W	154	0x58C
RX FIFO Low Watermark Port 3	32	R/W	154	0x58D
RX FIFO Low Watermark Port 4	32	R/W	154	0x58E
RX FIFO Low Watermark Port 5	32	R/W	154	0x58F
RX FIFO Low Watermark Port 6	32	R/W	154	0x590
RX FIFO Low Watermark Port 7	32	R/W	154	0x591
RX FIFO Low Watermark Port 8	32	R/W	154	0x592
RX FIFO Low Watermark Port 9	32	R/W	154	0x593
RX FIFO Number of Frames Removed on Port 0	32	CoR	156	0x594
RX FIFO Number of Frames Removed on Port 1	32	CoR	156	0x595
RX FIFO Number of Frames Removed on Port 2	32	CoR	156	0x596
RX FIFO Number of Frames Removed on Port 3	32	CoR	156	0x597
RX FIFO Number of Frames Removed on Port 4	32	CoR	156	0x598
RX FIFO Number of Frames Removed on Port 5	32	CoR	156	0x599
RX FIFO Number of Frames Removed on Port 6	32	CoR	156	0x59A
RXFIFO Number of Frames Removed on Port 7	32	CoR	156	0x59B
RX FIFO Number of Frames Removed on Port 8	32	CoR	156	0x59C
RX FIFO Number of Frames Removed on Port 9	32	CoR	156	0x59D
“RX FIFO Port Reset ($ 0x59E)”	32	R/W	158	0x59E
“RX FIFO Errored Frame Drop Enable ($ 0x59F)”	32	R/W	159	0x59F
“RX FIFO Overflow Event ($ 0x5A0)”	32	CoR	160	0x5A0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 56. TX Block Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO High Watermark Port 0	32	R/W	162	0x600
TX FIFO High Watermark Port 1	32	R/W	162	0x601
TX FIFO High Watermark Port 2	32	R/W	162	0x602
TX FIFO High Watermark Port 3	32	R/W	162	0x603
TX FIFO High Watermark Port 4	32	R/W	162	0x604
TX FIFO High Watermark Port 5	32	R/W	162	0x605
TX FIFO High Watermark Port 6	32	R/W	162	0x606
TX FIFO High Watermark Port 7	32	R/W	162	0x607
TX FIFO High Watermark Port 8	32	R/W	162	0x608
TX FIFO High Watermark Port 9	32	R/W	162	0x609
TX FIFO Low Watermark Port 0	32	R/W	162	0x60A
TX FIFO Low Watermark Port 1	32	R/W	163	0x60B
TX FIFO Low Watermark Port 2	32	R/W	163	0x60C
TX FIFO Low Watermark Port 3	32	R/W	163	0x60D
TX FIFO Low Watermark Port 4	32	R/W	163	0x60E
TX FIFO Low Watermark Port 5	32	R/W	163	0x60F
TX FIFO Low Watermark Port 6	32	R/W	163	0x610
TX FIFO Low Watermark Port 7	32	R/W	163	0x611
TX FIFO Low Watermark Port 8	32	R/W	163	0x612
TX FIFO Low Watermark Port 9	32	R/W	163	0x613
TX FIFO MAC Transfer Threshold Port 0	32	R/W	165	0x614
TX FIFO MAC Transfer Threshold Port 1	32	R/W	165	0x615
TX FIFO MAC Transfer Threshold Port 2	32	R/W	165	0x616
TX FIFO MAC Transfer Threshold Port 3	32	R/W	165	0x617
TX FIFO MAC Transfer Threshold Port 4	32	R/W	165	0x618
TX FIFO MAC Transfer Threshold Port 5	32	R/W	165	0x619
TX FIFO MAC Transfer Threshold Port 6	32	R/W	165	0x61A
TX FIFO MAC Transfer Threshold Port 7	32	R/W	165	0x61B
TX FIFO MAC Transfer Threshold Port 8	32	R/W	165	0x61C
TX FIFO MAC Transfer Threshold Port 9	32	R/W	165	0x61D
“TX FIFO Overflow Event ($ 0x61E)”	32	CoR	167	0x61E
Reserved	32	R	–	0x61F
“TX FIFO Drain ($0x620)”	32	R/W	168	0x620
“TX FIFO Info Out-of-Sequence ($ 0x621)”	32	CoR	169	0x621
TX FIFO Number of Frames Removed on Port 0	32	CoR	170	0x622

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 56. TX Block Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO Number of Frames Removed on Port 1	32	CoR	170	0x623
TX FIFO Number of Frames Removed on Port 2	32	CoR	170	0x624
TX FIFO Number of Frames Removed on Port 3	32	CoR	170	0x625
TX FIFO Number of Frames Removed on Port 4	32	CoR	170	0x626
TX FIFO Number of Frames Removed on Port 5	32	CoR	170	0x627
TX FIFO Number of Frames Removed on Port 6	32	CoR	170	0x628
TX FIFO Number of Frames Removed on Port 7	32	CoR	170	0x629
TX FIFO Number of Frames Removed on Port 8	32	CoR	170	0x62A
TX FIFO Number of Frames Removed on Port 9	32	CoR	170	0x62B
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 57. SPI4-2 Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
"SPI4-2 RX Burst Size ($ 0x700)"	32	R/W	172	0x700
"SPI4-2 RX Training ($ 0x701)"	32	R/W	172	0x701
"SPI4-2 RX Calendar ($ 0x702)"	32	R/W	173	0x702
"SPI4-2 TX Synchronization ($ 0x703)"	32	R/W	174	0x703
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 58. SerDes Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Reserved	32	RO	–	0x781
Reserved	32	RO	–	0x782
Reserved	32	RO	–	0x783
"SerDes Tx Driver Power Level Ports 0-6 ($ 0x784)"	32	RO	–	0x784
"SerDes Tx Driver Power Level Ports 7-9 ($ 0x785)"	32	RO	–	0x785
Reserved	32	RO	–	0x786
"SerDes TX and RX Power-Down Ports 0-9 ($ 0x787)"	32	R/W	175	0x787
Reserved	32	RO	–	0x793
Reserved	32	RO	–	0x794
Reserved	32	RO	–	0x795
Reserved	32	RO	–	0x796
Reserved	32	RO	–	0x797
Reserved	32	RO	–	0x798
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 59. Optical Module Interface Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
“Optical Module Status Ports 0-9 ($ 0x799)”	32	R	176	0x799
“Optical Module Control Ports 0-9 ($ 0x79A)”	32	R/W	176	0x79A
“I2C Control Ports 0-9 ($ 0x79B)”	32	R/W	177	0x79B
“I2C Data Ports 0-9 ($ 0x79C)”	32	R/W	177	0x79C
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

8.5.1 MAC Control Registers

Table 60 through Table 76 on page 139 provide details on the control and status registers associated with each MAC port. The register address is '**Port_index + 0x****', where the port index is set at any value from 0x000 through 0x500. All registers are 32 bits.

Table 60. Station Address Low ($ Port_Index + 0x00)

Bit	Name	Description	Type[1]	Default
31:0	Station Address Low	Source MAC address bits 31-0. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x00000000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 61. Station Address High ($ Port_Index + 0x01)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	Station Address High	Source MAC address bits 47-32. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x0000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 62. FDFC Type ($ Port_Index + 0x03)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	FDFC Type	Contains the value of the type field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x8808
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 63. FC TX Timer Value ($ Port_Index + 0x07)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	FC TX Timer Value	The pause length sent to the receiving station in 512 bit times	R/W	0x005E
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 64. FDFC Address Low ($ Port_Index + 0x08)

Bit	Name	Description	Type[1]	Default
31:0	FDFC Address Low	Contains the value of the lowest 32 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0xC2000001
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 65. FDFC Address High ($ Port_Index + 0x09)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	FDFC Address High	Contains the value of the highest 16 bits of the destination address filed transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0x0180
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 66. IPG Transmit Time ($ Port_Index + 0x0C)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	R	0x0000
9:0	IPG Transmit Time	IPG time for back-to-back transmissions (specified in multiples of 8 bit times). The value specified in this register is calculated as follows: (register value + 4) *8 = IPG length in terms of bit times. Therefore, the default value of 8 gives: (8+4) *8 = 96 bit times. 96 bit times is the minimum IPG. If a value of 8 or less is written to this register, the IPG remains 96 bit times.	R/W	0x0008
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 67. Pause Threshold ($ Port_Index + 0x0E)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	Pause Threshold	When a pause frame is sent, an internal timer checks when a new pause frame must be scheduled for transmission to keep the link partner in pause mode. The pause threshold value is the minimum time to send before the earlier pause frame is aged out (specified in multiples of 512 bit times). **Note:** The value in this register is subtracted from the value in the "FC TX Timer Value ($ Port_Index + 0x07)" to set the internal pause threshold. This value determines how often a Pause frame is sent out to keep the link partner in pause mode.	R/W	0x002F
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 68. Max Frame Size ($ Port_Index + 0x0F)

Bit	Name	Description	Type[1]	Default
31:14	Reserved	Reserved	R	0x0000
13:0	Max Frame Size	The maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. The maximum frame size is internally adjusted by +4 if VLAN is tagged.	R/W	0x05EE
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 69. FC Enable ($ Port_Index + 0x12)

Bit	Name	Description	Type[1]	Default
Register Description: Indicates which flow control mode is used for the RX and TX MAC.				0x00000007
31:2	Reserved	Reserved	R	0x00000000
1	TX FDFC	0 = Disable TX full-duplex flow control [the MAC will not generate internally any flow control frames based on the RX FIFO watermarks or the Transmit Pause Control interface 1 = Enable TX full-duplex flow control [enables the MAC to send flow control frames to the link partner based on the RX FIFO programmable watermarks or the Transmit Pause Control interface]	R/W	1
0	RX FDFC	0 = Disable RX full-duplex flow control [the MAC will not respond to flow control frames sent to it by the link partner] 1 = Enable RX full-duplex flow control [MAC will respond to flow control frames sent by the link partner and will stop packet transmission for the time specified in the flow control frame]	R/W	1
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 70. Discard Unknown Control Frame ($ Port_Index + 0x15)

Bit	Name	Description	Type[1]	Default
31:1	Reserved	Reserved	R	0x00000000
0	Discard Unknown Control Frame	0 = Keep unknown control frames 1 = Discard unknown control frames.	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 71. RX Config Word ($ Port_Index + 0x16) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in the IXF1110 only for auto-negotiation. Register bits 15:0 are the “config_word” received from the link partner, as described in IEEE 802.3, Sub clause 37.2.1.				0x00000000
31:22	Reserved		RO	0
21	An_complete	Auto-negotiation complete. This bit remains cleared from the time auto-negotiation is reset until auto-negotiation reaches the “LINK_OK” state. It remains set until auto-negotiation is disabled or restarted. (This bit is only valid if auto-negotiation is enabled.)	R	0
20	RX Sync	0 = Loss of synchronization 1 = Bit synchronization (bit remains Low until register is read)	CoR	0
19	RX Config	0 = Receiving idle/data stream 1 = Receiving /C/ ordered sets	R	
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 71. RX Config Word ($ Port_Index + 0x16) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
18	Config Changed	0 = RxConfigWord has changed since last read 1 = RxConfigWord has not changed since last read (This bit remains High until register is read)	CoR	0
17	Invalid Word	0 = Have not received an invalid symbol 1 = Have received an invalid symbol (This bit remains High until register is read)	CoR	0
16	Carrier Sense	0 = Device is not receiving idle characters (carrier sense is true). 1 = Device is receiving idle characters (carrier sense is false).	R	0
15	Next Page	Next Page request	R	0
14	Reserved	Reserved	R	0
13:12	RemoteFault[1:0]	Remote Fault Definitions: 00 = No error, link okay 01 = Offline 10 = Link failure 11 = Auto-negotiation_Error	R	00
11:9	Reserved	Reserved	R	000
8	Asym Pause	Asym Pause (ability to send pause frames)	R	0
7	Sym Pause	Sym Pause (ability to send and receive pause frames)	R	0
6	Half Duplex	Half-duplex	R	0
5	Full Duplex	Full-duplex	R	0
4:0	Reserved	Reserved	R	00000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 72. TX Config Word ($ Port_Index + 0x17) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in the IXF1110 for auto-negotiation only. The contents of this register are sent as the config_word.				0x000001A0
31:16	Reserved	Reserved	R	0x0000
15	NextPage	Next Page request	R/W	0
14	Reserved[3]	Write as 0, ignore on Read	R/W	0
13:12[2]	Remote Fault [1:0]	Remote fault definitions: 00 = No error, link okay 01 = Offline 10 = Link failure 11 = Auto-negotiation_Error	R/W	00
11:9	Reserved[3]	Write as 0, ignore on Read	R/W	000
8	Asym Pause	Ability to send pause frames	R/W	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. There is no way to automatically update the state of the Remote Fault bits for transmission. The state of these bits must be set by the system controller through the uP interface prior to enabling auto-negotiation.
3. Reserved bits must be written to '0' to prevent illegal advertisement.

Table 72. TX Config Word ($ Port_Index + 0x17) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
7	Sym Pause	Ability to send and receive pause frames	R/W	1
6	Half Duplex	Half-duplex	R/W	0
5	Full Duplex	Full-duplex	R/W	1
4:0	Reserved[3]	Write as 0, ignore on Read	R/W	00000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. There is no way to automatically update the state of the Remote Fault bits for transmission. The state of these bits must be set by the system controller through the uP interface prior to enabling auto-negotiation.
3. Reserved bits must be written to '0' to prevent illegal advertisement.

Table 73. Diverse Config ($ Port_Index + 0x18)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains various configuration bits for general use.				0x0000110D
31:19	Reserved	Reserved	R	0x0000
18:13	Reserved	Write as 0, ignore on Read	R/W	000000
12	Reserved[2]	Write as 1, ignore on Read	R/W	1
11:9	Reserved[2]	Write as 0, ignore on Read	R/W	000
8	Reserved[2]	Write as 1, ignore on Read	R/W	1
7	pad_enable	Enable padding of undersized packets	R/W	0
6	crc_add	Enable automatic CRC appending	R/W	0
5	AN_enable	Auto-negotiation enable: 1 = Setting this bit to 1 puts the port in an auto-negotiation mode and starts auto-negotiation. 0 = Setting this bit to 0 disables auto-negotiation and puts the IXF1110 in forced mode. Note: Since default = 0, this bit must be changed to a 1 via the CPU to enable auto-negotiation. Auto-negotiation can be restarted by de-asserting this bit, then re-asserting.	R/W	0
4[2]	Reserved	Write as 0, ignore on Read	R/W	0
3:2[2]	Reserved	Write as 1, ignore on Read	R/W	11
1[2]	Reserved	Write as 0, ignore on Read	R/W	0
0[2]	Reserved	Write as 1, ignore on Read	R/W	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. Reserved bits must be written to the default value for proper operation

Table 74. RX Packet Filter Control ($ Port_Index + 0x19) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register allows for specific packet types to be marked for filtering, and is used in conjunction with the RX FIFO Errored Frames Drop Enable Register				0x00000000
31:6	Reserved	Reserved	R	0x000000
5	CRC Error Pass[2]	This bit enables a Global filter on frames with a CRC Error. When CRCErrorPASS = 0, all frames with a CRC Error are marked as bad. **NOTE:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 92 on page 159). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When the CRC Error Pass Filter bit = 0, it takes precedence over the other filter bits. Any packet regardless if it is a Pause, Unicast, Multicast or Broadcast packet with a CRC error will be marked as bad frames when CRC Error Pass = 0 When CRCErrorPASS = 1, frames with a CRC Error are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
4	Pause Frame Pass	This bit enables a Global filter on Pause frames. When PauseFramePass = 0, all Pause frames are marked as bad. **NOTE:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 92 on page 159). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. **NOTE:** When PauseFramePass = 1, all Pause frames are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
3	VLAN Drop En[2]	This bit enables a Global filter on VLAN frames. When VLANDropEn = 0, all VLAN frames are passed to the SPI4-2 Interface. When VLANDropEn = 1, all VLAN frames are dropped.[3]	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 74. RX Packet Filter Control ($ Port_Index + 0x19) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	B/Cast Drop En[2]	This bit enables a Global filter on Broadcast frames. When B/CastDropEn = 0, all broadcast frames are passed to the SPI4-2 Interface. When B/CastDropEn = 1, all broadcast frames are dropped.[3]	R/W	0
1	M/Cast Match En[2]	This bit enables a filter on multicast frames. If this bit = 0, all multicast frames are good and are passed to the SPI4-2 Interface. If this bit = 1, only multicast frames with a destination address that matches the PortMulticastAddress is forwarded. All other multicast frames are dropped.[3]	R/W	0
0	U/Cast Match En[2]	This bit enables a filter on unicast frames. If this bit = 0, all unicast frames are good and are passed to the SPI4-2 interface. If this bit = 1, only unicast frames with a destination address that matches the Station Address is forwarded. All other unicast frames are dropped.[3] **NOTE:** The VLAN filter overrides the Unicast filter. Thus, a VLAN frame cannot be filtered based on the Unicast address.	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 75. Port Multicast Address Low ($ Port_Index + 0x1A)

Bit	Name	Description	Type[1]	Default
31:0	Port Multicast Address Low	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	R/W	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 76. Port Multicast Address High ($ Port_Index + 0x1B)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	Port Multicast Address High	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	R/W	0x0000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.2 MAC RX Statistics Register Overview

The MAC RX Statistics Registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 77 covers the MAC RX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 77. MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 1 of 4)

Name	Description	Address	Type[1]	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x20	CoR	0x00000000
RxOctetsBAD[2]	Counts the bytes received in all bad frames of a size greater than or equal to 64 bytes. A bad frame is defined as a properly framed packet containing a CRC, alignment error, or code violation. The 64-byte value is measured from the destination address, up to and including CRC. The initial preamble and SFD are not included in this value. **Note:** This register does not increment the Bad Octet count on undersized receive packets.	Port_Index + 0x21	CoR	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets) **Note:** This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x22	CoR	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets) **Note:** This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	CoR	0x00000000
RxBCPkts	The total number of Broadcast packets received (excluding bad packets)	Port_Index + 0x24	CoR	0x00000000
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x25	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size ($ Port_Index + 0x0F)" on page 134.

Table 77. MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 2 of 4)

Name	Description	Address	Type[1]	Default
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x26	CoR	0x00000000
RxPkts128to255 Octets	The total number of packets received (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field	Port_Index + 0x27	CoR	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x28	CoR	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were [512-1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x29	CoR	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x2A	CoR	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x2B	CoR	0x00000000
RxFCSErrors	Number of frames received with legal size, but with wrong CRC field (also called FCS field) **Note:** Legal size is 64 bytes through the value stored in the "Max Frame Size ($ Port_Index + 0x0F)" on page 134.	Port_Index + 0x2C	CoR	0x00000000
RxTagged	Number of frames with VLAN tag (Type field = 0x8100)	Port_Index + 0x2D	CoR	0x00000000
RxDataError	Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII) **NOTE:** The IXF1110 does not support an RGMII interface; thus, this counter is not applicable to the IXF1110.	Port_Index + 0x2E	CoR	0x00000000
RxAlignErrors	**NOTE:** Number of frames with a legal frame size, but containing less than 8 additional bits. This occurs when a frame is not byte-aligned. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, the frame is not counted, but treated as an OK frame.The IXF1110 does not support an RGMII interface; thus, this counter is not applicable to the IXF1110	Port_Index + 0x2F	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size ($ Port_Index + 0x0F)" on page 134.

Table 77. MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 3 of 4)

Name	Description	Address	Type[1]	Default
RxLongErrors[2]	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x30	CoR	0x00000000
RxJabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x31	CoR	0x00000000
RxPauseMac ControlCounter	Number of Pause MAC control frames received This statistic register increments on any valid 64byte Pause frame with valid CRC and will also increment on 64byte Pause Frames with an invalid CRC if bit 5 of the "RX Packet Filter Control ($ Port_Index + 0x19)" is set to 1.	Port_Index + 0x32	CoR	0x00000000
RxUnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause)	Port_Index + 0x33	CoR	0x00000000
RxVeryLongErrors[2]	Frames bigger than the larger of 2*MaxFrameSize and 50000 bits	Port_Index + 0x34	CoR	0x00000000
RxRuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times. **Note:** RxRuntErrors is not supported in the IXF1110. Any runt or short packets received are not counted in this register. **Note:** The "ShortRuntsThreshold" Register controls the byte count used to determine the difference between Runts and Shorts, and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames.	Port_Index + 0x35	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size ($ Port_Index + 0x0F)" on page 134.

Table 77. MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 4 of 4)

Name	Description	Address	Type[1]	Default
RxShortErrors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well formed preamble and SFD. This counter indicates fragment sizes illegal in all modes, and is only fully updated after reception of a good frame following a fragment. **Note:** RxShortErrors is not supported in the IXF1110. Any runt or short packets received are not counted in this register.	Port_Index + 0x36	CoR	0x00000000
RxCarrierExtend Error	Gigabit half-duplex event only Note: N/A - half-duplex only	Port_Index + 0x37	CoR	0x00000000
RxSequenceErrors	Records the number of sequencing errors that occur.	Port_Index + 0x38	CoR	0x00000000
RxSymbolErrors	Records the number of symbol errors encountered.	Port_Index + 0x39	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the “Max Frame Size ($ Port_Index + 0x0F)” on page 134.

8.5.3 MAC TX Statistics Register Overview

The MAC TX Statistics Registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 78 covers the MAC TX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 78. MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 1 of 4)

Name	Description	Address	Type[1]	Default
TXOctetsTotalOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x40	CoR	0x00000000
TXOctetsBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. TX underrun counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded. TX CRC error counted: All bytes not sent with success are counted by this counter	Port_Index + 0x41	CoR	0x00000000
TXUCPkts	The total number of unicast packets transmitted (excluding bad packets)	Port_Index + 0x42	CoR	0x00000000
TXMCPkts	The total number of multicast packets transmitted (excluding bad packets) **Note:** This count includes pause control packets which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	CoR	0x00000000
TXBCPkts	The total number of broadcast packets transmitted (excluding bad packets)	Port_Index + 0x44	CoR	0x00000000
TXPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x45	CoR	0x00000000
TXPkts65to127Octets	The total number of packets transmitted (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x46	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 78. MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 2 of 4)

Name	Description	Address	Type[1]	Default
TXPkts128to255Octets	The total number of packets transmitted (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128 - 255 bytes, including tag field	Port_Index + 0x47	CoR	0x00000000
TXPkts256to511Octets	The total number of packets transmitted (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x48	CoR	0x00000000
TXPkts512to1023Octets	The total number of packets transmitted (including bad packets) that were [512 - 1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x49	CoR	0x00000000
TXPkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x4A	CoR	0x00000000
TXPkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x4B	CoR	0x00000000
TXDeferred	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. **Note**: N/A - half-duplex only	Port_Index + 0x4C	CoR	0x00000000
TXTotalCollisions	Sum of all collision events **Note**: N/A - half-duplex only	Port_Index + 0x4D	CoR	0x00000000
TXSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4E	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 78. MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 3 of 4)

Name	Description	Address	Type[1]	Default
TXMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4F	CoR	0x00000000
TXLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. **Note**: N/A - half-duplex only	Port_Index + 0x50	CoR	0x00000000
TXExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions Note: N/A - half-duplex only	Port_Index + 0x51	CoR	0x00000000
TXExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize due to another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. **Note**: N/A - half-duplex only	Port_Index + 0x52	CoR	0x00000000
TXExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	CoR	0x00000000
TXUnderrun	Internal TX error which causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	CoR	0x00000000
TXTagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	CoR	0x00000000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 78. MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 4 of 4)

Name	Description	Address	Type[1]	Default
TXCRCError	Number of frames transmitted with a legal size, but with the wrong CRC field (also called FCS field)	Port_Index + 0x56	CoR	0x00000000
TXPauseFrames	Number of pause MAC frames transmitted	Port_Index + 0x57	CoR	0x00000000
TXFlowControlCollisions Send	Collisions generated on purpose on incoming frames, to avoid reception of traffic, while the port is in half-duplex and has flow control enabled, and do not have sufficient memory to receive more frames. Note: Due to the internal counting technique, a last frame might have to be transmitted after last flow control collision send to get the correct statistic. **Note**: N/A - half-duplex only	Port_Index + 0x58	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.4 Global Status and Configuration Register Overview

Table 79 through Table 86 on page 151 provide an overview of the Global Control and Status Registers.

Table 79. Port Enable ($ 0x500)

Bit	Name	Description	Type[1]	Default
Register Description: A control register for each port in the IXF1110. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 disables the port. The default state for this register is for all 10 ports to be active.				0x000003FF
31:10	Reserved	Reserved	R	0x00000
9	Port 9 Enable	Port 9 0 = Disable 1 = Enable	R/W	1
8	Port 8 Enable	Port 8 0 = Disable 1 = Enable	R/W	1
7	Port 7 Enable	Port 7 0 = Disable 1 = Enable	R/W	1
6	Port 6 Enable	Port 6 0 = Disable 1 = Enable	R/W	1
5	Port 5 Enable	Port 5 0 = Disable 1 = Enable	R/W	1
4	Port 4 Enable	Port 4 0 = Disable 1 = Enable	R/W	1
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	1
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	1
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	1
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. If a port is disabled mid-packet on the receive side in SerDes mode, the RX Stats will not update for that packet due to power-down of SerDes when the port is disabled.

Table 80. Link LED Enable ($ 0x502)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port bit should be set upon detection of link by system CPU to enable proper operation of the link LEDs.				0x00000000
31:10	Reserved	Reserved	R	0x00000
9	Link LED Enable Port 9	Port 9 link 0 = No link 1 = Link	R/W	0
8	Link LED Enable Port 8	Port 8 link 0 = No link 1 = Link	R/W	0
7	Link LED Enable Port 7	Port 7 link 0 = No link 1 = Link	R/W	0
6	Link LED Enable Port 6	Port 6 link 0 = No link 1 = Link	R/W	0
5	Link LED Enable Port 5	Port 5 link 0 = No link 1 = Link	R/W	0
4	Link LED Enable Port 4	Port 4 link 0 = No link 1 = Link	R/W	0
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 81. Core Clock Soft Reset ($ 0x504)

Bit	Name	Description	Type[1]	Default
Register Description: A soft reset register for the core clock system (for example, the SYS125 clock).				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	Core Soft Reset	0 = CoreSoftReset reset is inactive 1 = CoreSoftReset reset is active	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 82. MAC Soft Reset ($ 0x505)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port software activated reset of the MAC core.				0x00000000
31:10	Reserved	Reserved	R	0x00000
9	MAC Soft Reset Port 9	Port 9 0 = Reset inactive 1 = Reset active	R/W	0
8	MAC Soft Reset Port 8	Port 8 0 = Reset inactive 1 = Reset active	R/W	0
7	MAC Soft Reset Port 7	Port 7 0 = Reset inactive 1 = Reset active	R/W	0
6	MAC Soft Reset Port 6	Port 6 0 = Reset inactive 1 = Reset active	R/W	0
5	MAC Soft Reset Port 5	Port 5 0 = Reset inactive 1 = Reset active	R/W	0
4	MAC Soft Reset Port 4	Port 4 0 = Reset inactive 1 = Reset active	R/W	0
3	MAC Soft Reset Port 3	Port 3 0 = Reset inactive 1 = Reset active	R/W	0
2	MAC Soft Reset Port 2	Port 2 0 = Reset inactive 1 = Reset active	R/W	0
1	MAC Soft Reset Port 1	Port 1 0 = Reset inactive 1 = Reset active	R/W	0
0	MAC Soft Reset Port 0	Port 0 0 = Reset inactive 1 = Reset active	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 83. CPU Interface ($ 0x508)

Bit	Name	Description	Type[1]	Default
Register Description: CPU interface Endian select. This register allows the user to select the Endian of the CPU interface to allow various different CPUs to be connected to the IXF1110.				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	Endian	0 = Little Endian 1 = Big Endian	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 84. LED Control ($ 0x509)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the LED mode.				0x00000000
31-2	Reserved	Reserved	R	0x00000000
1	LED Enable	0 = Disable LEDs 1 = Enable LEDs	R/W	0
0	LED_SEL_MODE	0 = Enable LED Mode 0 for use with SGS Thompson M5450 LED driver (Default) 1 = LED Mode 1 for use with Standard Octal Shift Register	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 85. LED Flash Rate ($ 0x50A)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the flash rate.				0x00000000
31:3	Reserved	Reserved	R	0x00000000
2:0	LED Flash Rate	000 = 100 ms flash rate 001 = 200 ms flash rate 010 = 300 ms flash rate 011 = 400 ms flash rate 100 = 500 ms flash rate 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 86. LED Fault Disable ($ 0x50B) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port fault disable: Disables the LED flashing for local or remote faults				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	LED Fault Disable Port 9	Port 9 0 = Fault enabled 1 = Fault disabled	R/W	0
8	LED Fault Disable Port 8	Port 8 0 = Fault enabled 1 = Fault disabled	R/W	0
7	LED Fault Disable Port 7	Port 7 0 = Fault enabled 1 = Fault disabled	R/W	0
6	LED Fault Disable Port 6	Port 6 0 = Fault enabled 1 = Fault disabled	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 86. LED Fault Disable ($ 0x50B) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
5	LED Fault Disable Port 5	Port 5 0 = Fault enabled 1 = Fault disabled	R/W	0
4	LED Fault Disable Port 4	Port 4 0 = Fault enabled 1 = Fault disabled	R/W	0
3	LED Fault Disable Port 3	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0
2	LED Fault Disable Port 2	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Fault Disable Port 1	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Fault Disable Port 0	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 87. JTAG ID Revision ($ 0x50C)

Bit	Name	Description	Type	Default
Register Description: The value of this register follows the same scheme as the device identification register found in the IEEE 1149.1 specification. The upper 4 bits correspond to silicon stepping. The next 16 bits store a Part ID Number. The next 11 bits contain a JEDEC Manufacturer ID. Bit zero = 1 if the chip is the first in a stack. The encoding scheme used for the Product ID field is implementation dependent.				0x40456013
31:28	Version[2]	Version[2]	R	0100
27:12	Part ID	Part ID	R	0000010001010110
11:8	JEDEC Cont.	JEDEC Cont.	R	0000
7:1	JEDEC ID	JEDEC ID	R	0001001
0	Reserved	Reserved	R	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. See the IXF1110 Specification Upate for the latest version.

8.5.5 Global RX Block Register Overview

Table 88 through Table 93 on page 160 provide an overview of the RX Block Registers, which include the RX FIFO High and Low watermarks.

Table 88. RX FIFO High Watermark Ports 0 to 9 ($ 0x580 - 0x589) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 0	High watermark for RX FIFO port 0. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x580	R/W	0x00000740
RX FIFO High Watermark Port 1	High watermark for RX FIFO port 1. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x581	R/W	0x00000740
RX FIFO High Watermark Port 2	High watermark for RX FIFO port 2. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x582	R/W	0x00000740
RX FIFO High Watermark Port 3	High watermark for RX FIFO port 3. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x583	R/W	0x00000740
RX FIFO High Watermark Port 4	High watermark for RX FIFO port 4. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x584	R/W	0x00000740
RX FIFO High Watermark Port 5	High watermark for RX FIFO port 5. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x585	R/W	0x00000740
RX FIFO High Watermark Port 6	High watermark for RX FIFO port 6. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x586	R/W	0x00000740

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and R.
   Bits 14:0 - Described above.

Table 88. RX FIFO High Watermark Ports 0 to 9 ($ 0x580 - 0x589) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 7	High watermark for RX FIFO port 7. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x587	R/W	0x00000740
RX FIFO High Watermark Port 8	High watermark for RX FIFO port 8. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC	0x588	R/W	0x00000740
RX FIFO High Watermark Port 9	High watermark for RX FIFO port 9. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x589	R/W	0x00000740

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and R.
   Bits 14:0 - Described above.

Table 89. RX FIFO Low Watermark Ports 0 to 9 ($ 0x58A - 0x593) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 0	Low watermark for RX FIFO port 0. The default value is 1840 bytes. When the port is in flow control, and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58A	R/W	0x00000730
RX FIFO Low Watermark Port 1	Low watermark for RX FIFO port 1. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58B	R/W	0x00000730
RX FIFO Low Watermark Port 2	Low watermark for RX FIFO port 2. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58C	R/W	0x00000730
RX FIFO Low Watermark Port 3	Low watermark for RX FIFO port 3. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58D	R/W	0x00000730
RX FIFO Low Watermark Port 4	Low watermark for RX FIFO port 4. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58E	R/W	0x00000730

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and R.
   Bits 14:0 - Described above.

Table 89. RX FIFO Low Watermark Ports 0 to 9 ($ 0x58A - 0x593) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 5	Low watermark for RX FIFO port 5. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58F	R/W	0x00000730
RX FIFO Low Watermark Port 6	Low watermark for RX FIFO port 6. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x590	R/W	0x00000730
RX FIFO Low Watermark Port 7	Low watermark for RX FIFO port 7. The default value is 1840 bytes.When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x591	R/W	0x00000730
RX FIFO Low Watermark Port 8	Low watermark for RX FIFO port 8. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x592	R/W	0x00000730
RX FIFO Low Watermark Port 9	Low watermark for RX FIFO port 9. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x593	R/W	0x00000730

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and R.
   Bits 14:0 - Described above.

Table 90. RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 0	This register counts all frames removed from the RX FIFO for port 0 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x594	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 1	This register counts all frames removed from the RX FIFO for port 1 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x595	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 2	This register counts all frames removed from the RX FIFO for port 2 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x596	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 3	This register counts all frames removed from the RX FIFO for port 3 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x597	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 4	This register counts all frames removed from the RX FIFO for port 4 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x598	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and R.
   Bits 21:0 - Described above.

Table 90. RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 5	This register counts all frames removed from the RX FIFO for port 5 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x599	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 6	This register counts all frames removed from the RX FIFO for port 6 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x59A	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 7	This register counts all frames removed from the RX FIFO for port 7 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x59B	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 8	This register counts all frames removed from the RX FIFO for port 8 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x59C	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 9	This register counts all frames removed from the RX FIFO for port 9 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 92 on page 159) • Frames are greater than the MaxFrameSize (Table 68 on page 134)	0x59D	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and R.
   Bits 21:0 - Described above.

Table 91. RX FIFO Port Reset ($ 0x59E)

Bit	Name	Description	Type[1]	Default
Register Description: The soft reset register for each port in the RX block. Port ID = bit position in the register. To make the reset active, the bit must be set High. For example, reset of port 4 implies register value = 0001.0000. Setting the bit to 0 de-asserts the reset.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	RXFIFOPort 9 Reset	Port 9 0 = De-assert reset 1 = Reset	R/W	0
8	RXFIFOPort 8 Reset	Port 8 0 = De-assert reset 1 = Reset	R/W	0
7	RXFIFOPort 7 Reset	Port 7 0 = De-assert reset 1 = Reset	R/W	0
6	RXFIFOPort 6 Reset	Port 6 0 = De-assert reset 1 = Reset	R/W	0
5	RXFIFOPort 5 Reset	Port 5 0 = De-assert reset 1 = Reset	R/W	0
4	RXFIFOPort 4 Reset	Port 4 0 = De-assert reset 1 = Reset	R/W	0
3	RXFIFOPort 3 Reset	Port 3 0 = De-assert reset 1 = Reset	R/W	0
2	RXFIFOPort 2 Reset	Port 2 0 = De-assert reset 1 = Reset	R/W	0
1	RXFIFOPort 1 Reset	Port 1 0 = De-assert reset 1 = Reset	R/W	0
0	RXFIFOPort 0 Reset	Port 0 0 = De-assert reset 1 = Reset	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 92. RX FIFO Errored Frame Drop Enable ($ 0x59F) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in conjunction with the RX Packet Filter Control Register bits to select whether errored or filtered frames are to be dropped.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 9: 0 = Do not drop frames 1 = Drop frames	R/W	0
8	RX FIFO Errored Frame Drop Enable Port 8	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 8: 0 = Do not drop frames 1 = Drop frames	R/W	0
7	RX FIFO Errored Frame Drop Enable Port 7	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 7: 0 = Do not drop frames 1 = Drop frames	R/W	0
6	RX FIFO Errored Frame Drop Enable Port 6	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 6: 0 = Do not drop frames 1 = Drop frames	R/W	0
5	RX FIFO Errored Frame Drop Enable Port 5	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 5: 0 = Do not drop frames 1 = Drop frames	R/W	0
4	RX FIFO Errored Frame Drop Enable Port 4	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 4: 0 = Do not drop frames 1 = Drop frames	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 92. RX FIFO Errored Frame Drop Enable ($ 0x59F) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
3	RX FIFO Errored Frame Drop Enable Port 3	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 3: 0 = Do not drop frames 1 = Drop frames	R/W	0
2	RX FIFO Errored Frame Drop Enable Port 2	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 2: 0 = Do not drop frames 1 = Drop frames	R/W	0
1	RX FIFO Errored Frame Drop Enable Port 1	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 1: 0 = Do not drop frames 1 = Drop frames	R/W	0
0	RX FIFO Errored Frame Drop Enable Port 0	These bits are used in conjunction with the "RX Packet Filter Control ($ Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 0: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 93. RX FIFO Overflow Event ($ 0x5A0) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a status if a FIFO-full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	RX FIFO Overflow Event Port 9	Port 9 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
8	RX FIFO Overflow Event Port 8	Port 8 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
7	RX FIFO Overflow Event Port 7	Port 7 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 93. RX FIFO Overflow Event ($ 0x5A0) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
6	RX FIFO Overflow Event Port 6	Port 6 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
5	RX FIFO Overflow Event Port 5	Port 5 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
4	RX FIFO Overflow Event Port 4	Port 4 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
3	RX FIFO Overflow Event Port 3	Port 3 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
2	RX FIFO Overflow Event Port 2	Port 2 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
1	RX FIFO Overflow Event Port 1	Port 1 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
0	RX FIFO Overflow Event Port 0	Port 0 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.6 TX Block Register Overview

Table 94 through Table 100 on page 170 provide an overview of the TX Block Registers, which include the TX FIFO High and Low Watermark.

Table 94. TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 0	High watermark for TX FIFO port 0. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x600	R/W	0x00000630
TX FIFO High Watermark Port 1	High watermark for TX FIFO port 1. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x601	R/W	0x00000630
TX FIFO High Watermark Port 2	High watermark for TX FIFO port 2. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x602	R/W	0x00000630
TX FIFO High Watermark Port 3	High watermark for TX FIFO port 3. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x603	R/W	0x00000630
TX FIFO High Watermark Port 4	High watermark for TX FIFO port 4. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x604	R/W	0x00000630
TX FIFO High Watermark Port 5	High watermark for TX FIFO port 5. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x605	R/W	0x00000630
TX FIFO High Watermark Port 6	High watermark for TX FIFO port 6. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x606	R/W	0x00000630

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 94. TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 7	High watermark for TX FIFO port 7. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x607	R/W	0x00000630
TX FIFO High Watermark Port 8	High watermark for TX FIFO port 8. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x608	R/W	0x00000630
TX FIFO High Watermark Port 9	High watermark for TX FIFO port 9. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x609	R/W	0x00000630

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 95. TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 0	Low watermark for TX FIFO port 0. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60A	R/W	0x000001D0
TX FIFO Low Watermark Port 1	Low watermark for TX FIFO port 1. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60B	R/W	0x000001D0
TX FIFO Low Watermark Port 2	Low watermark for TX FIFO port 2. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60C	R/W	0x000001D0
TX FIFO Low Watermark Port 3	Low watermark for TX FIFO port 3. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60D	R/W	0x000001D0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 95. TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 4	Low watermark for TX FIFO port 4. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60E	R/W	0x000001D0
TX FIFO Low Watermark Port 5	Low watermark for TX FIFO port 5. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60F	R/W	0x000001D0
TX FIFO Low Watermark Port 6	Low watermark for TX FIFO port 6. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x610	R/W	0x000001D0
TX FIFO Low Watermark Port 7	Low watermark for TX FIFO port 7. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x611	R/W	0x000001D0
TX FIFO Low Watermark Port 8	Low watermark for TX FIFO port 8. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x612	R/W	0x000001D0
TX FIFO Low Watermark Port 9	Low watermark for TX FIFO port 9. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x613	R/W	0x000001D0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 96. TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) (Sheet 1 of 3)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 0	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x614	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 1	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x615	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 2	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x616	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 3	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x617	R/W	0x00000100

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 96. TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) (Sheet 2 of 3)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 4	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x618	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 5	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x619	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 6	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61A	R/W	0x00000100

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 96. TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) (Sheet 3 of 3)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 7	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61B	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 8	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61C	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 9	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61D	R/W	0x00000100

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 97. TX FIFO Overflow Event ($ 0x61E) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides status that a FIFO- full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Overflow Event Port 9	Port 9 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
8	TX FIFO Overflow Event Port 8	Port 8 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 97. TX FIFO Overflow Event ($ 0x61E) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
7	TX FIFO Overflow Event Port 7	Port 7 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
6	TX FIFO Overflow Event Port 6	Port 6 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
5	TX FIFO Overflow Event Port 5	Port 5 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
4	TX FIFO Overflow Event Port 4	Port 4 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
3	TX FIFO Overflow Event Port 3	Port 3 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
2	TX FIFO Overflow Event Port 2	Port 2 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
1	TX FIFO Overflow Event Port 1	Port 1 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
0	TX FIFO Overflow Event Port 0	Port 0 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 98. TX FIFO Drain ($0x620) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register enables the TX FIFO drain mode for the selected port by holding the TX FIFO for that port in reset. All data stored in the TX FIFO is lost when this bit is set to 1. When this bit is set to 1, the TX FIFO status for the selected port is STARVING.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Drain Port 9	Port 9 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
8	TX FIFO Drain Port 8	Port 8 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
7	TX FIFO Drain Port 7	Port 7 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
6	TX FIFO Drain Port 6	Port 6 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 98. TX FIFO Drain ($0x620) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
5	TX FIFO Drain Port 5	Port 5 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
4	TX FIFO Drain Port 4	Port 4 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
3	TX FIFO Drain Port 3	Port 3 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
2	TX FIFO Drain Port 2	Port 2 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
1	TX FIFO Drain Port 1	Port 1 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
0	TX FIFO Drain Port 0	Port 0 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 99. TX FIFO Info Out-of-Sequence ($ 0x621) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register signals when out-of-sequence data is detected in the TX FIFO. Events such as SOP followed by another SOP cause this bit to be set and remain so until read. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Info Out-of-Sequence Port 9	Port 9 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
8	TX FIFO Info Out-of-Sequence Port 8	Port 8 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
7	TX FIFO Info Out-of-Sequence Port 7	Port 7 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
6	TX FIFO Info Out-of-Sequence Port 6	Port 6 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 99. TX FIFO Info Out-of-Sequence ($ 0x621) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
5	TX FIFO Info Out-of-Sequence Port 5	Port 5 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
4	TX FIFO Info Out-of-Sequence Port 4	Port 4 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
3	TX FIFO Info Out-of-Sequence Port 3	Port 3 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
2	TX FIFO Info Out-of-Sequence Port 2	Port 2 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
1	TX FIFO Info Out-of-Sequence Port 1	Port 1 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
0	TX FIFO Info Out-of-Sequence Port 0	Port 0 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 100. TX FIFO Number of Frames Removed Ports 0-9 ($ 0x622 - 0x62B) (Sheet 1 of 2)

Name	Description	Address	Type[1]	Default
TX FIFO Number of Frames Removed on Port 0	This register counts the number of frames removed on port 0 due to a TX FIFO overflow.	0x622	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 1	This register counts the number of frames removed on port 1 due to a TX FIFO overflow.	0x623	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 2	This register counts the number of frames removed on port 2 due to a TX FIFO overflow.	0x624	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 3	This register counts the number of frames removed on port 3 due to a TX FIFO overflow.	0x625	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 4	This register counts the number of frames removed on port 4 due to a TX FIFO overflow.	0x626	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 5	This register counts the number of frames removed on port 5 due to a TX FIFO overflow.	0x627	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 100. TX FIFO Number of Frames Removed Ports 0-9 ($ 0x622 - 0x62B) (Sheet 2 of 2)

Name	Description	Address	Type[1]	Default
TX FIFO Number of Frames Removed on Port 6	This register counts the number of frames removed on port 6 due to a TX FIFO overflow.	0x628	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 7	This register counts the number of frames removed on port 7 due to a TX FIFO overflow.	0x629	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 8	This register counts the number of frames removed on port 8 due to a TX FIFO overflow	0x62A	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 9	This register counts the number of frames removed on port 9 due to a TX FIFO overflow.	0x62B	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.7 SPI4-2 Block Register Overview

Table 101 through Table 104 on page 174 provide an overview of the SPI4-2 Block Registers.

Table 101. SPI4-2 RX Burst Size ($ 0x700)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for burst size.				0x00060002
31	idles	0 = Zero idle insertion between transfer bursts 1 = Inserts four idle control words between each burst. (This occurs not only on an EOP, but also at the end of every MaxBurst1 or MaxBurst2.	R/W	0x0
30:25	Reserved	Reserved	R	0x00
24:16	MaxBurst1	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1110, can accept when the FIFO Status channel indicates STARVING. **NOTE:** Do not program these bits below 0x2 (32 byte burst).	R/W	0x006
15:9	Reserved	Reserved	R	0x00
8:0	MaxBurst2	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1110, can accept when the FIFO Status channel indicates HUNGRY. **NOTE:** Do not program these bits below 0x2 (32 byte burst).	R/W	0x002
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 102. SPI4-2 RX Training ($ 0x701)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for training sequences				0x00000000
31:24	Reserved	Reserved	R	0x00
23:16	REP_T	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles	R/W	0x00
15:0	DATA_MAX_T[2]	Maximum interval (in number of cycles) between scheduling of training sequences on receive data path interface An all zero value disables periodic training sequences.	R/W	0x0000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write 2. The value of DATA_MAX_T is the Most Significant 16 bits of a 24-bit counter value. The Least Significant 8 bits are always 0x00. This allows for a much larger DAT_MAX_T time-out period and provides a more than adequate granularity of selection.				

Table 103. SPI4-2 RX Calendar ($ 0x702)

Bit	Name	Description	Type[1]	Default Value
Register Description: SPI4-2 RX interface start-up parameters for FIFO status calendar operation.				0x00010300
31:30	RX Train Test Modes	00 = Normal mode 01 = Do not enter training based on a repeating “11” pattern on RSTAT[1:0] 1x = Train continuously	R/W	0x0
29	RSCLK_invert	0 = The FIFO status is captured on the rising edge of the RSCLK as per the SPI4-2 specification 1 = The FIFO status is captured on the falling edge of RSCLK **NOTE:** For proper operation, set this bit to the desired setting before the RSCLK is applied to the device.	R/W	0
28	TSCLK_invert	0 = The FIFO status is launched on the rising edge of the TSCLK as per the SPI4-2 specification 1 = The FIFO status is launched on the falling edge of TSCLK	R/W	0
27:21	Reserved	Reserved	R	0x000
20	DIP2_Error	Set based on an incorrect RX DIP2 result. This bit is cleared upon a read	CoR	0x0
19:16	DIP-2_Thr	Defines how many consecutive correct DIP-2s are required to disable sending of training sequences on the RX SPI4-2.	R/W	0x1
15:14	Reserved	Reserved	R	00
13	RX SPI4-2 Sync	0 = RX SPI4 In Training (RDAT = training) RX SPI4 Out Of Training (RDAT = idles)	R	0
12	TX SPI4 Sync	0 = TX SPI4-2 Calendar is in constant Framing The TX SPI4-2 has received the valid training patterns on TDAT and is now sending a 10 port Calendar on TSAT with valid FIFO information	R	0
11:8	Loss_of_Sync	Loss-of-Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and restart training sequences.	R/W	0x3
7:4	Reserved	Reserved	R	0x0
3:0	Reserved	Write as 0, ignore on Read.	R/W	0x0
1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write				

Table 104. SPI4-2 TX Synchronization ($ 0x703)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 synchronization DIP-4 counters.				0x00000420
31:16	DIP4_Errors	DIP4_Errors is the total number of DIP4 errors detected since this register was last read.	CoR	0x0000
15:8	DIP4_UnLock[2]	DIP-4_Unlock is a SPI4-2 parameter specifying the number of incorrect DIP4 fields to be detected to declare loss of synchronization and drive the TSTAT[1:0] bus with framing.	R/W	0x04
7:0	DIP4_Lock	Number of consecutive correct DIP4 results to achieve synchronization and end training	R/W	0x20

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When Periodic Training is enabled, the actual count of DIP4 errors required to lose synchronization is 1 less than the programmed value in this register. Therefore, this value should always be programmed to be 1 more than the desired value and should never be programmed to either 0 or 1.

8.5.8 SerDes Register Overview

Table 105 through **Table 107 on page 175** define the contents of the SerDes Register Block at base location 0x780 which contain the control and status for the ten SerDes interfaces on the IXF1110.

Table 105. SerDes Tx Driver Power Level Ports 0-6 ($ 0x784)

Bit	Name	Description	Type[1]	Default
Register Description: Allows selection of various programmable drive strengths on each of the SerDes ports. **NOTE:** Refer to Table 21, "SerDes Driver TX Power Levels" on page 71 for valid SerDes power levels.				0X00000000
31:28	Reserved	Reserved	R	0x0
27:25	DRVPWR6[3:0]	Encoded input that sets Power Level for Port 6	R/W	1101
24:21	DRVPWR5[3:0]	Encoded input that sets Power Level for Port 5	R/W	1101
20:16	DRVPWR4[3:0]	Encoded input that sets Power Level for Port 4	R/W	1101
15:12	DRVPWR3[3:0]	Encoded input that sets Power Level for Port 3	R/W	1101
11:8	DRVPWR2[3:0]	Encoded input that sets Power Level for Port 2	R/W	1101
7:4	DRVPWR1[3:0]	Encoded input that sets Power Level for Port 1	R/W	1101
3:0	DRVPWR0[3:0]	Encoded input that sets Power Level for Port 0	R/W	1101

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 106. SerDes Tx Driver Power Level Ports 7-9 ($ 0x785)

Bit	Name	Description	Type[1]	Default
Register Description: Allows selection of various programmable drive strengths on each of the SerDes ports. **NOTE:** Refer to Table 21, "SerDes Driver TX Power Levels" on page 71 for valid SerDes power levels.				0X00000000
31:12	Reserved	Reserved	R	0x00000
11:8	DRVPWR9[3:0]	Encoded input that sets Power Level for Port 9	R/W	1101
7:4	DRVPWR8[3:0]	Encoded input that sets Power Level for Port 8	R/W	1101
3:0	DRVPWR7[3:0]	Encoded input that sets Power Level for Port 7	R/W	1101
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 107. SerDes TX and RX Power-Down Ports 0-9 ($ 0x787)

Bit	Name	Description	Type[1]	Default
Register Description: Tx and Rx power-down bits to allow per-port power-down of unused ports				0x00000000
31:20	Reserved	Reserved	R	0x000
19:10	TPWRDWN[9:0]	Tx power-down for Ports 0-9 (1 = Power-down)	R/W	0000000000
9:0	RPWRDWN[9:0]	Rx power-down for Ports 0-9 (1 = Power-down)	R/W	0000000000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

8.5.9 Optical Module Interface Block Register Overview

Table 108 through Table 111 provide an overview of the Optical Module Interface Block Registers. These registers provide a means to control and monitor the interface to the optical modules.

Table 108. Optical Module Status Ports 0-9 ($ 0x799)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides optical module status information.				0x00000000
31:30	Reserved	Reserved	R	00
29:20	RX_LOS_9:0	RX_LOS inputs for Ports 0-9	R	0000000000
19:10	TX_FAULT_9:0	TX_FAULT inputs for Ports 0-9	R	0000000000
9:0	MOD_DEF_9:0	MOD_DEF inputs for Ports 0-9	R	0000000000
1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write				

Table 109. Optical Module Control Ports 0-9 ($ 0x79A)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides access to optical module interrupt enables and sets the TX_DISABLE outputs.				0x00000000
31:13	Reserved	Reserved	R	0000000000 000000000
12	RX_LOS_En	Enable for RX_LOS_Int operation 0 = Disabled 1 = Enabled	R/W	0
11	TX_FAULT_En	Enable for TX_FAULT_Int operation 0 = Disabled 1 = Enabled	R/W	0
10	MOD_DEF_En	Enable for MOD_DEF_Int operation 0 = Disabled 1 = Enabled	R/W	0
9:0	TX_DISABLE_9:0	TX_DISABLE outputs for Ports 0-9	R/W	0000000000
1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write				

Table 110. I²C Control Ports 0-9 ($ 0x79B) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register controls I²C Reads and Writes.				0x00000000
31:29	Reserved	Reserved	R	000
28	Port Address Error	Port Address Error is set to 1 when an access is requested to port address > 0x9.	R	0
27	WP_Err	Write Protect error is set to 1 when a write access is requested to Device ID = 0xA and Register Address [10:8] = 0. This address combination is used solely for the read only optical module.	R	0
1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write				

Table 110. I²C Control Ports 0-9 ($ 0x79B) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
26	no_ack-err	This bit is set to 1 when a optical module has failed to assert an acknowledge cycle. This signal should be used to validate the data being read. Data is only valid if this bit is equal to zero.	R	0
25	I²CEnable	Enables device wide I²C Accesses (Enabled = 1)	R/W	0
24	I²C Start	I²C Start = 1 will initiate the I²C cycle. This bit is clear on read.	CoR	0
23	Reserved	Reserved	R	0
22	Write Complete	Write Complete is set to a 1 when the byte write cycle has completed.	R	0
21	Reserved	Reserved	R	0
20	Read Valid	Read Valid is set to a 1 when valid data is available in the DataRead7:0 field.	R	0
19:16	Port Address Select 3:0	IXF1110 port address to be accessed	R/W	0x0
15	Read/Write	0 = Write 1 = Read	R/W	1
14:11	Device ID	Most significant 4 bits of Device ID/Address field.	R/W	0xA
10:0	Register Address	Bits 10:8 define least significant 3 bits of Device ID/ Address field. Bits 7:0 define the register address.	R/W	00000000000
1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write				

Table 111. I²C Data Ports 0-9 ($ 0x79C)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides I²C Reads and Writes.				0x00000000
31:24	Reserved	Reserved	R	0x00
23:16	Write Data	Write_Data contains the data to be written during the I²C byte write cycle.	R/W	0x00
15:8	Reserved	Reserved	R	0x00
7:0	Read_Data	Read_Data contains the byte received during the last I²C Read Cycle.	R	0x00
1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write				

9.0 Package Overview

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications, having high noise immunity requirements.

9.1 Features

- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power zone offering supports core and four additional voltages
- JEDEC-compliant package

9.2 IXF1110 Package Specifics

The IXF1110 uses the following packaging (see Figure 44, “Intel® IXF1110 MAC 552-Ceramic Ball Grid Array (CBGA) Package Specifications” on page 180):

- 576-ball BGA package with 6 balls removed diagonally from each corner, for a total of 552 balls used measuring 25 mm x 25 mm
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

9.2.1 Markings

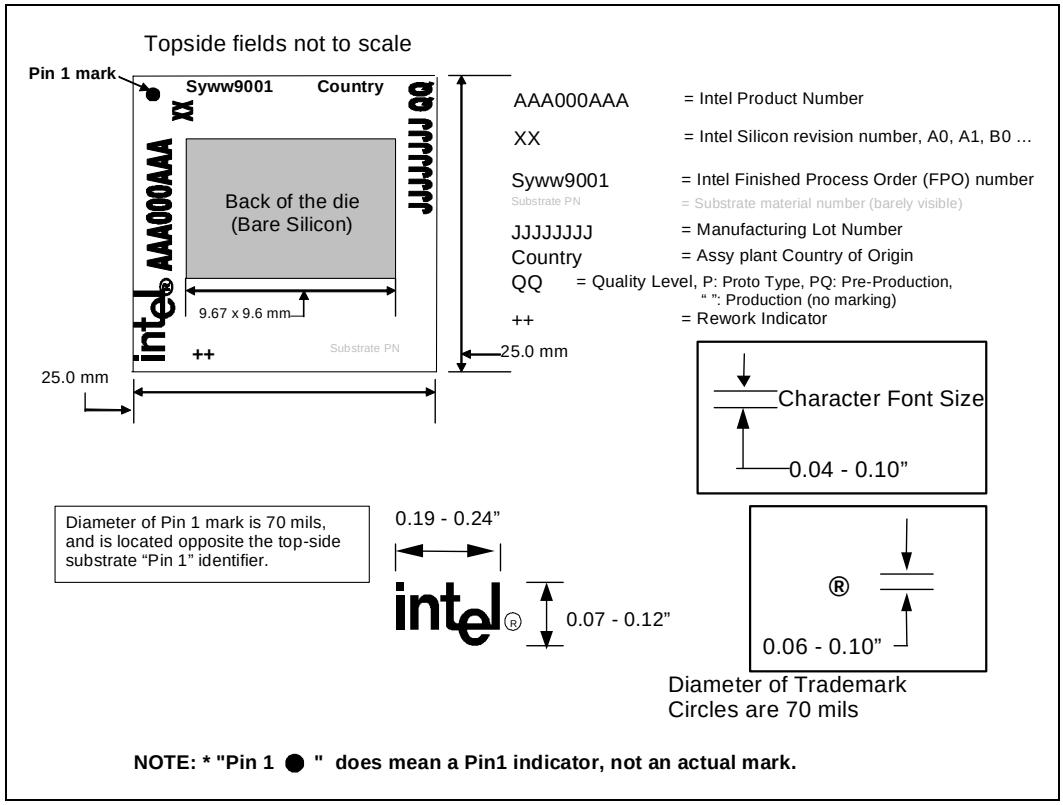
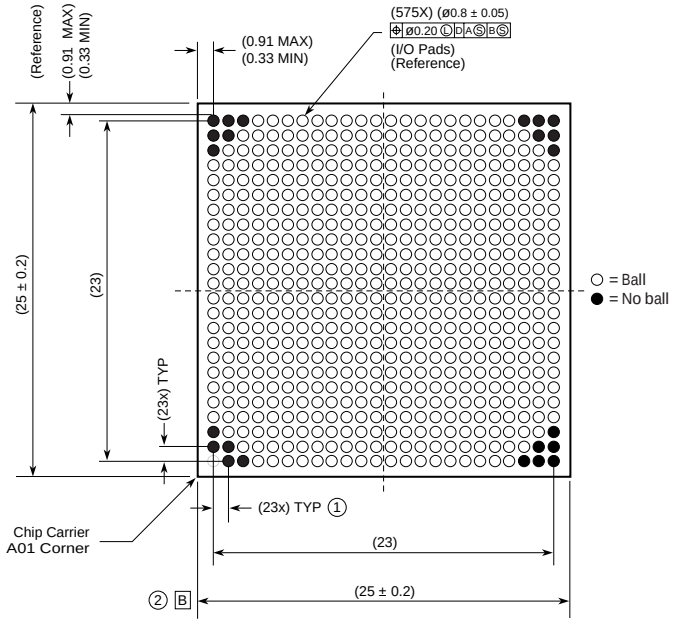
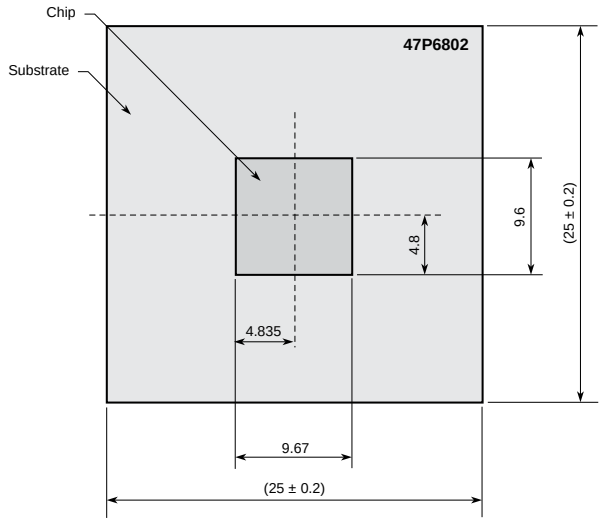


Figure 44. Intel® IXF1110 MAC 552-Ceramic Ball Grid Array (CBGA) Package Specifications



Note: All dimensions are in mm.

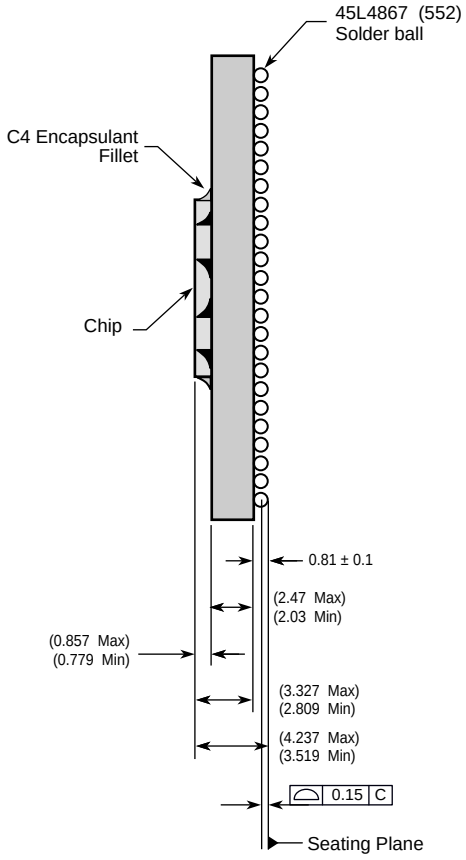
B0611-02



Note: All dimensions are in mm.

B0612-01

Figure 45. Intel®IXF1110 MAC CBGA Package Side View Diagram



Note: All dimensions are in mm.

B0610-01

10.0 Product Ordering Information

Table 112. Intel® IXF1110 MAC Product Information

Number	Revision	Qualification	MM Number	Ship Media
HFIXF1110CC B2	B2	S	860817	Tray

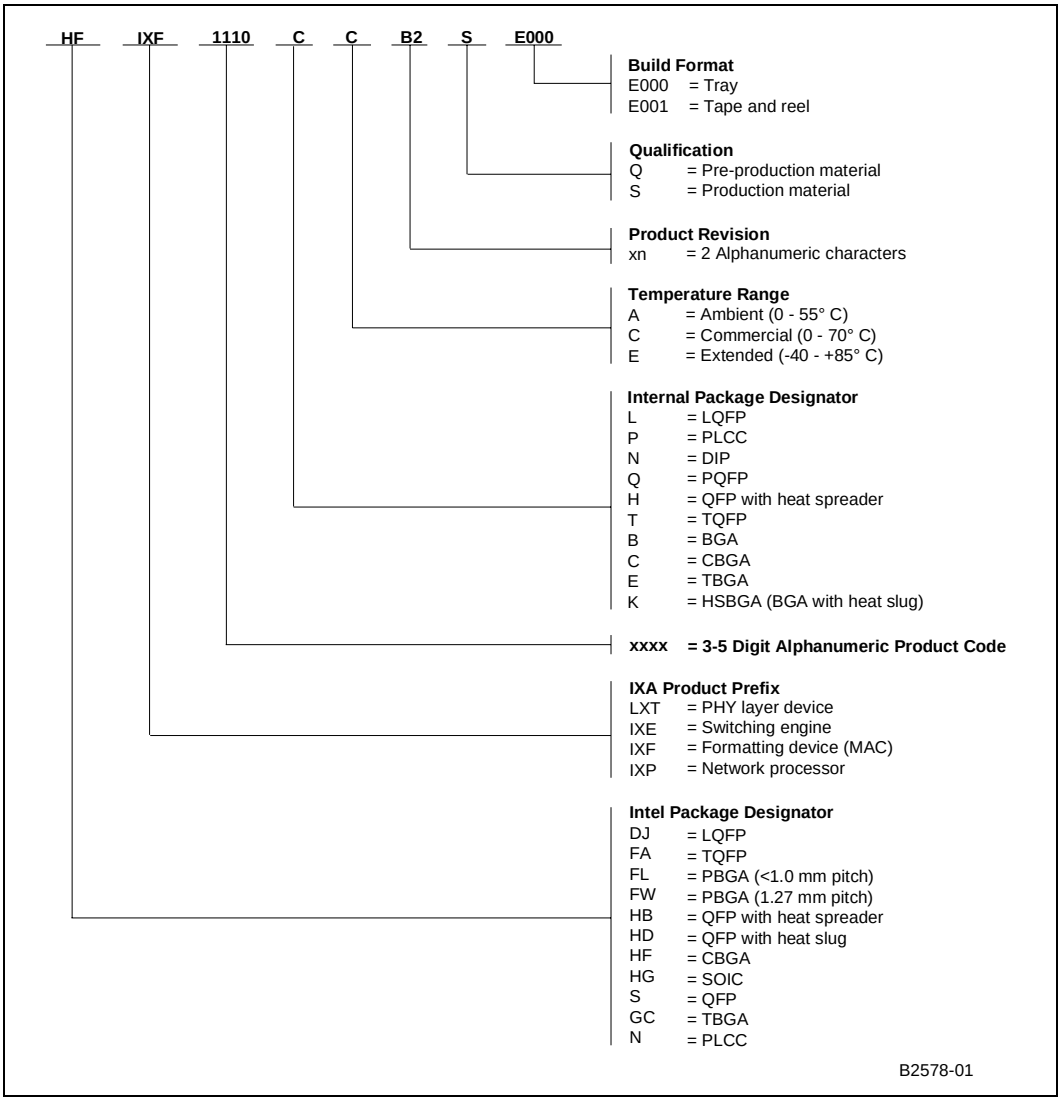



Figure 46. Intel® IXF1110 MAC Ordering Information - Sample