Contents

The S-4610A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It easily drives small heads separately because its driver enable is 32-bit×2. It is ideal for the video printer and the low-voltage-drive thermal print head because of large driver output current and small ON-state resistance.

■ Features

- Low current consumption : 0.4 mA typ.
  (f_{CLK}=5 MHz, SI : fixed)
- High speed operation : 7 MHz (chip)
  5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 70 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls
- Selectable "H/L" for latch and driver enable

■ Block Diagram

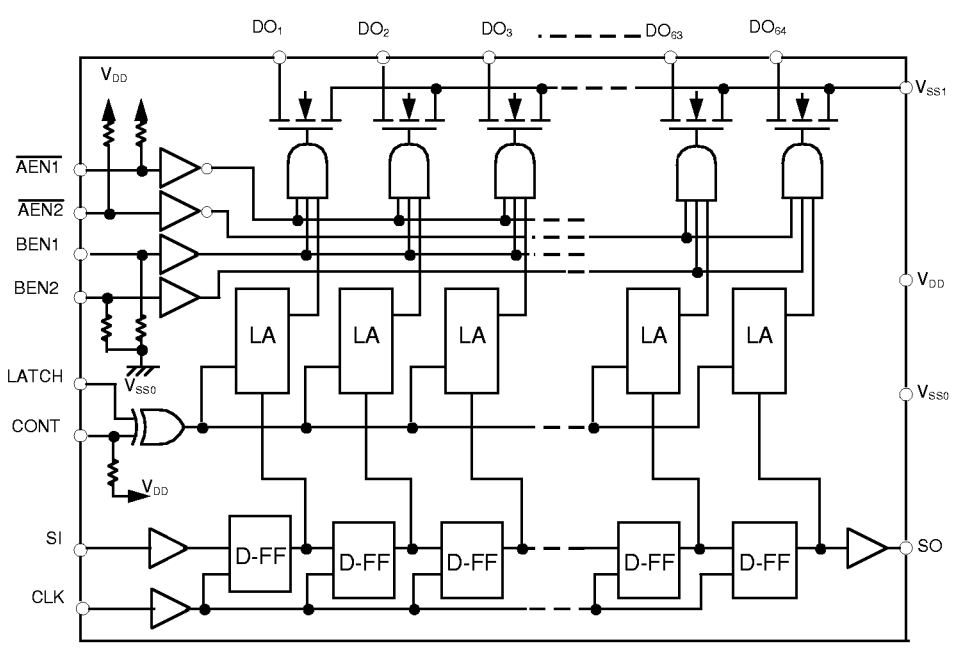

Figure 1

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit operates depending on the levels of CONT and LATCH ; it reads the data of the shift register when their levels are the same, and it holds the data of the shift register when they differ.

The latch data are output to the respective drivers when $\overline{AEN1}$and $\overline{AEN2}$ are low and BEN1and BEN2 are high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{AEN1}$and $\overline{AEN2}$ high or BEN1and BEN2 low makes all driver output transistors go off. $\overline{AEN1}$ and BEN1 control 1-bit to 32-bit of driver output and $\overline{AEN2}$ and BEN2 control 33-bit to 64-bit.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO_1 to DO_{64} (DO_n)	Driver output terminals(Nch open-drain)
65, 68, 71, 74, 77, 80, 83, 86	V_{SS1}	GND for driver (0 V)
67	V_{DD}	Positive power supply for logic (+5 V)
75, 81	V_{SS0}	GND for logic (0 V)
82	CLK	Clock input terminal for 64-bit shift register
85	SI	Serial data input terminal for 64-bit shift register
66	SO	Serial data output terminal for 64-bit shift register
84	LATCH	Data latch signal input terminal When CONT="L" LATCH="L": reads the data of the shift register LATCH="H": holds the preceding data When CONT="H" or open LATCH="L": holds the preceding data LATCH="H": reads the data of the shift register
76	CONT	Data latch signal control terminal : selects "H" or "L" for LATCH(pull-up resistor is built in)
73	$\overline{AEN1}$	Driver enable terminal : $\overline{AEN1}$ outputs the latch data of DO_1 to DO_{32} and $\overline{AEN2}$ DO_{33} to DO_{64} when low(pull-up resistor is built in)
72	$\overline{AEN2}$	
70	BEN1	Driver enable terminal : BEN1 outputs the latch data of DO_1 to DO_{32} and BEN2 DO_{33} to DO_{64} when high(pull-down resistor is built in)
69	BEN2	
78, 79	NC	Dummy terminals

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{SS0,1}$ - V_{DD}	-0.4 to +7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	70	mA
Input voltage	V_{IN}	V_{SS0}-0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	V_{SS0}-0.5 to V_{DD}+0.5	V
Max. junction temperature	T_{jMAX}	125	°C
Operating temperature	T_{opr}	-10 to +80	°C
Storage temperature	T_{stg}	-40 to +125	°C

■ DC Electrical Characteristics

Table 3

(Unless otherwise specified : V_{DD}=5.0 V±10%, Ta=-10°C to 80°C)

Parameter	Sybl	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
High level input voltage	V_{IH}			0.7×V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}			V_{SS}	—	0.3×V_{DD}	V
High level input current	I_{IH}	V_{DD}=5.0 V, V_{IH}=5.0 V, Ta=25°C	BEN1, 2	—	—	35	µA
				—	—	0.5	µA
Low level input current	I_{IL}	V_{DD}=5.0 V, V_{IL}=0 V, Ta=25°C	$\overline{AEN1, 2}$, CONT	-35	—	—	µA
				-0.5	—	—	µA
High level output voltage	V_{OH}	SO terminal, no load		4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load		—	—	0.05	V
High level output current	I_{OH}	SO terminal, V_{OH}=V_{DD}-0.4 V		—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, V_{OL}=0.4 V		0.5	—	—	mA
High level driver output voltage	V_{DOH}			—	24	26	V
Low level driver output voltage	V_{DOL}	I_{DOL}=50 mA, V_{DD}=5.0 V		—	0.5	1.1	V
Driver leakage current	I_{LEAK}	V_{DOH}=26 V, Per 1-bit of driver output		—	—	1.0	µA
Current consumption	I_{DD}	Ta=25°C	f_{CLK} =2 MHz,SI : fixed	—	0.2	0.6	mA
			f_{CLK} =5 MHz,SI : fixed	—	0.4	1.2	mA
			f_{CLK} =5 MHz, SI=1/2f_{CLK}	—	1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}			2.0	—	4.0	V

■ AC Electrical Characteristics

Table 4

(V_{DD}= 5.0 V±10%, Ta=-10°C to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	V_{IH}=V_{DD}, V_{IL}=V_{SS0}	50	—	—	ns
Data hold time	t_{HD}	V_{IH}=V_{DD}, V_{IL}=V_{SS0}	10	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	C_L=3 pF	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L=1 kΩ, V_{DOH}=24 V	—	—	6.5	µs
DOn rise time	t_{rDO}	R_L=1 kΩ, V_{DOH}=24 V	—	1.7	4.5	µs
DOn fall time	t_{fDO}	R_L=1 kΩ, V_{DOH}=24 V	—	2.0	5.0	µs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

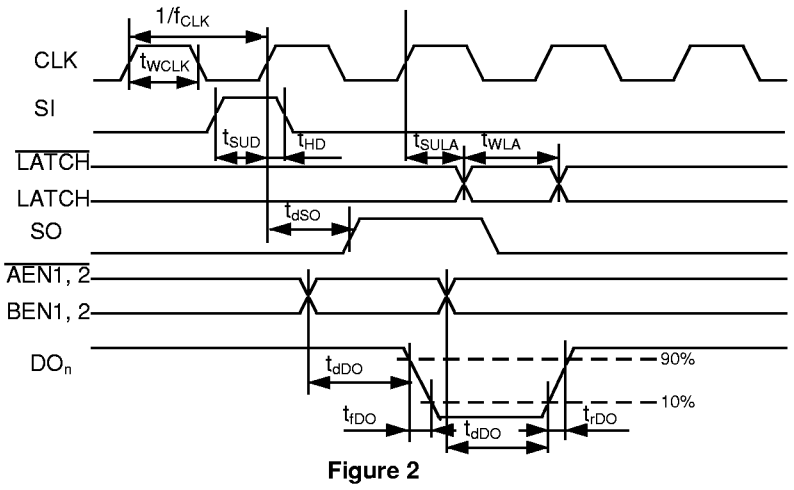

Figure 2

■ Dimensions

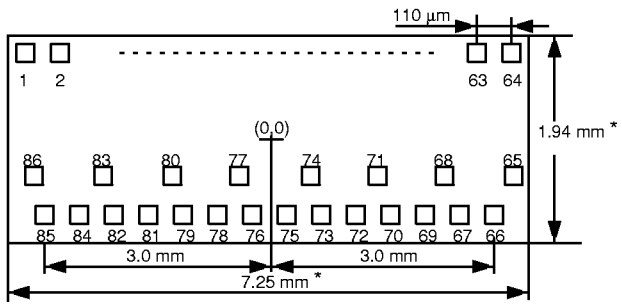

Figure 3

Pad size : 80 µm×80 µm
(passivation opening)
Pad pitch :
Driver output pad : 110 µm
Control pad : 200 µm min.
Chip thickness : 350±30 µm

*Before dicing

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5 Unit : µm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO_1	-3465	865	30	DO_{30}	-275	865	59	DO_{59}	2915	865
2	DO_2	-3355	865	31	DO_{31}	-165	865	60	DO_{60}	3025	865
3	DO_3	-3245	865	32	DO_{32}	-55	865	61	DO_{61}	3135	865
4	DO_4	-3135	865	33	DO_{33}	55	865	62	DO_{62}	3245	865
5	DO_5	-3025	865	34	DO_{34}	165	865	63	DO_{63}	3355	865
6	DO_6	-2915	865	35	DO_{35}	275	865	64	DO_{64}	3465	865
7	DO_7	-2805	865	36	DO_{36}	385	865	65	V_{SS1}	3070	-455
8	DO_8	-2695	865	37	DO_{37}	495	865	66	SO	2870	-865
9	DO_9	-2585	865	38	DO_{38}	605	865	67	V_{DD}	2455	-865
10	DO_{10}	-2475	865	39	DO_{39}	715	865	68	V_{SS1}	2190	-455
11	DO_{11}	-2365	865	40	DO_{40}	825	865	69	BEN2	1985	-865
12	DO_{12}	-2255	865	41	DO_{41}	935	865	70	BEN1	1785	-865
13	DO_{13}	-2145	865	42	DO_{42}	1045	865	71	V_{SS1}	1310	-455
14	DO_{14}	-2035	865	43	DO_{43}	1155	865	72	$\overline{AEN2}$	985	-865
15	DO_{15}	-1925	865	44	DO_{44}	1265	865	73	$\overline{AEN1}$	785	-865
16	DO_{16}	-1815	865	45	DO_{45}	1375	865	74	V_{SS1}	430	-455
17	DO_{17}	-1705	865	46	DO_{46}	1485	865	75	V_{SS0}	230	-865
18	DO_{18}	-1595	865	47	DO_{47}	1595	865	76	CONT	30	-865
19	DO_{19}	-1485	865	48	DO_{48}	1705	865	77	V_{SS1}	-450	-455
20	DO_{20}	-1375	865	49	DO_{49}	1815	865	78	NC	-870	-865
21	DO_{21}	-1265	865	50	DO_{50}	1925	865	79	NC	-1130	-865
22	DO_{22}	-1155	865	51	DO_{51}	2035	865	80	V_{SS1}	-1330	-455
23	DO_{23}	-1045	865	52	DO_{52}	2145	865	81	V_{SS0}	-1535	-865
24	DO_{24}	-935	865	53	DO_{53}	2255	865	82	CLK	-1965	-865
25	DO_{25}	-825	865	54	DO_{54}	2365	865	83	V_{SS1}	-2210	-455
26	DO_{26}	-715	865	55	DO_{55}	2475	865	84	LATCH	-2420	-865
27	DO_{27}	-605	865	56	DO_{56}	2585	865	85	SI	-2890	-865
28	DO_{28}	-495	865	57	DO_{57}	2695	865	86	V_{SS1}	-3090	-455
29	DO_{29}	-385	865	58	DO_{58}	2805	865				