82595FX
ISA BUS HIGH INTEGRATION ETHERNET CONTROLLER

- **Optimal Integration for Lowest Cost Solution**
  - — Glueless 8-Bit/16-Bit ISA Bus Interface
  - — Provides Fully 802.3 Compliant AUI and TPE Serial Interface
  - — Local SRAM Support up to 64 Kbytes
  - — Integrated ISA Bus Data Transceivers
  - — FLASH/EPROM Boot Support up to 1 Mbyte for Diskless Workstations
  - — Hardware and Software Portable between Motherboard and Adapter Card Solutions
- **High Performance Networking Functions**
  - — Advanced Concurrent Processing of Receive and Transmit Functions
  - — 16-Bit/32-Bit IO Accesses to Local SRAM with Zero Added Wait-States
  - — Ring Buffer Structure for Continuous Frame Reception and Transmit Chaining
  - — Automatic Retransmission on Collision
  - — Automatically Corrects TPE Polarity Switching Problems
  - — Auto Negotiation/Manual Full Duplex Support
- **Low Power CHMOS IV Technology**
- **Ease of Use**
  - — Auto-Negotiation of Full Duplex Functionality
  - — Fully Compatible with ISA Plug and Play Specification
  - — EEPROM Interface to Support Jumperless Designs
  - — Software Structures Optimized to Reduce Processing Steps
  - — Automatically Maps into Unused PC IO Locations to Help Eliminate LAN Setup Problems
  - — All Software Structures Contained in One 16-Byte IO Space
  - — JTAG Port for Reduced Board Testing Times
  - — Automatic or Manual Switching between TPE and AUI Ports
  - — Supports Eight IRQs
- **Power Management**
  - — Advanced Power Management Support by Power Down and Sleep Mode
  - — Both SL Compatible SMOUT Input and Non-SL Software Parameter for Power Down Mode
- **160-Lead QFP Package Provides Smallest Available Form Factor**
- **100% Backwards Software Compatible to 82595TX**

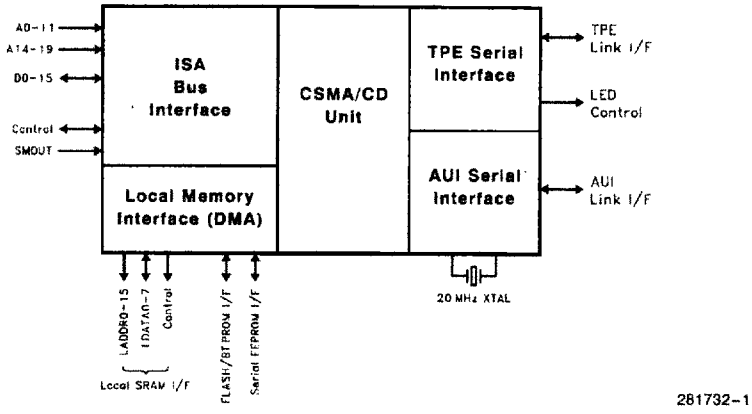

Figure 1. 82595FX Block Diagram

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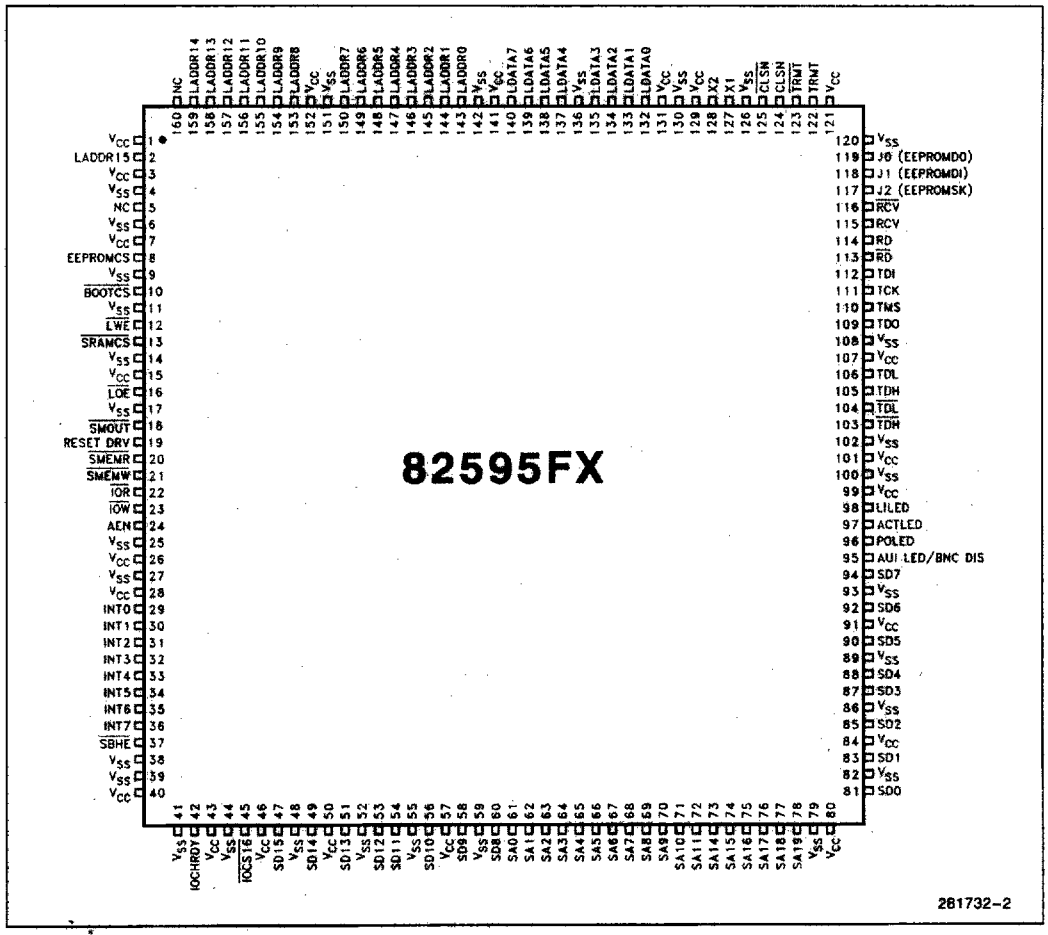


Figure 2. 82595FX Pinout

1.0 INTRODUCTION

1.1 82595FX Overview

The 82595FX is a highly integrated, high performance LAN controller which provides a cost effective LAN solution for ISA compatible Personal Computer (PC) motherboards (both desktop and portable), and add-on ISA adapter boards. The 82595FX integrates all of the major functions of a buffered LAN solution into one chip with the exception of the local buffer memory, which is implemented by adding one SRAM component to the LAN solution. The 82595FX's Concurrent Processing feature significantly enhances throughput performance. Both system bus and serial link activities occur concurrently, allowing the 82595FX to maximize network bandwidth by minimizing delays associated with transmit or receiving frames. The 82595FX's bus interface is a glueless attachment to an ISA bus. Its serial interface provides a Twisted Pair Ethernet (TPE) and an Attachment Unit Interface (AUI) connection. By integrating the majority of the LAN solution functions into one cost effective component, production cost saving can be achieved as well as significantly decreasing the design time for a solution. This level of integration also allows an 82595FX solution to be ported between different applications (PC motherboards, and adapters, while maintaining a compatible hardware and software base.

The 82595FX's software interface is optimized to reduce the number of processing steps that are required to interface to the 82595FX solution. The 82595FX's initialization and control registers are directly addressable within one 16-byte IO address block. The 82595FX can automatically resolve any conflicts to an IO block by moving its IO offset to an unused location in the case that a conflict occurs. The 82595FX's local memory is arranged in a simple ring buffer structure for efficient transfer of transmit and receive packets. The local memory, up to 64 Kbytes of SRAM, resides as either a 16-bit or 32-bit IO port in the host systems IO map programmable through configuration. The 82595FX provides direct control over the local SRAM. The 82595FX performs a prefetch to the SRAM memory allowing CPU IO cycles to this data with no added wait-states. The 82595FX also provides an interface to up to 1 Mbyte of FLASH or EPROM memory. An interface to an EEPROM, which holds solution configuration values and can also contain the Node ID, allows for the implementation of a "jumperless" design. In addition, the 82595FX contains full hardware support for the implementation of the ISA Plug N' Play specification. Plug N' Play eliminates jumpers and complicated setup utilities by allowing peripheral functions to be added to a PC automatically (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). This allows for configuration ease-of-use, which results in minimal time associated with installation.

The 82595FX's packaging and power management features are designed to consume minimal board real estate and system power. This is required for applications such as portable PC motherboard designs which require a solution with very low real estate and power consumption. The 82595FX package is a 160-lead PQFP (Plastic Quad Flat Pack). Its dimensions are 28 mm by 28 mm, and 3.5 mm in height. The 82595FX contains two power down modes; an SL compatible power down mode which utilizes the SL SMOUT input, and a POWER DOWN command for non-SL systems.

1.2 Power Management

Power management and low power consumption are two items that will allow any design using the 82595FX to be suitable for green PC use. Low power operation is initiated when software issues a SLEEP command to the device. After a short wait, it will shut off the system clock, some parts of the Backoff Randomizer, several input buffers and the two LED drivers. The 82595FX will subsequently wake up from sleep mode when software initiates an ISA cycle in the application, as well as when it receives a frame addressed to it. The total power consumption when in sleep mode can be as low as approximately 175 mW. Normal idle power consumption is 300 mW.

The software POWER DOWN command, along with its companion hardware implementation—the SMOUT I/O pin, provide additional power management capabilities. This feature allows the 82595FX to be powered down, and then at some time in the future be selectively reset without having lost the current configuration. See the 82595FX User's Guide for further details on these features.

1.3 Auto-Negotiation

Auto-negotiation functionality is a method of automatically determining the highest common operating mode (i.e., 10BaseT half duplex, 10BaseT full duplex, etc.) between two network devices. Using this functionality, two stations, each having a varying number of different operating modes, negotiate the highest possible common operating mode between them. During the power up sequence, the auto-negotiation functionality will automatically establish a link with which it can take advantage of any auto-negotiation-capable device it is connected to. An auto-negotiation capable hub can detect and automatically configure its ports to take maximum advantage of

common modes of operation without any user intervention or prior knowledge by connected stations. See the 82595FX User's Guide for details on this function.

> For further information on these enhancements and a description of all the differences between the 82595TX and 82595FX, please consult the 82595FX User's Manual, available through your local sales representative.

1.4 Compliance to Industry Standards

The 82595FX has two interfaces; the host system interface, which is an ISA bus interface, and the serial, or network interface. This interface has been standardized by the IEEE.

1.4.1 BUS INTERFACE—ISA IEEE P996

The 82595FX implements the full ISA bus interface. It is compatible with the IEEE spec P996.

1.4.2 ETHERNET/TWISTED PAIR ETHERNET INTERFACE—IEEE 802.3 SPECIFICATION

The 82595FX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop, providing a fully compliant IEEE 802.3 AUI interface. The TPE port provides a fully compliant IEEE 10BASE-T interface. The 82595FX can automatically switch to whichever port (TPE or AUI) is active.

2.0 82595FX PIN DEFINITIONS

2.1 ISA Bus Interface

Symbol	Pin No.	Type	Name and Function
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11	61 62 63 64 65 66 67 68 69 70 71 72	I	**ADDRESS BUS:** These pins provide address decoding for up to 1 Kbyte of address. These pins also provide 4 Kbytes of IO addressing to support the Plug N' Play Standard.
SA14 SA15 SA16 SA17 SA18 SA19	73 74 75 76 77 78	I	**ADDRESS BUS:** These pins provide address decoding between the 16 Kbyte and 1 Mbyte memory space. This allows for decoding of a Boot EPROM or a FLASH in 16K increments.

2.1 ISA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	81 83 85 87 88 90 92 94 60 58 56 54 53 51 49 47	I/O	**DATA BUS:** This is the data interface between the 82595FX and the host system. This data is buffered by one (8-bit design) or two (16-bit design) internal transceivers.
AEN	24	I	**ADDRESS ENABLE:** Active high signal indicates a DMA cycle is active.
$\overline{\text{SMEMR}}$	20	I	**MEMORY READ** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{SMEMW}}$	21	I	**MEMORY WRITE** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{IOR}}$	22	I	**IO READ:** Active low.
$\overline{\text{IOW}}$	23	I	**IO WRITE:** Active low.
$\overline{\text{IOCS16}}$	45	O	**IO CHIP SELECT 16:** Active low, open drain output which indicates that an IO cycle access to the 82595FX solution is 16-bit wide. Driven for IO cycles to the local memory or to the 82595FX.
IOCHRDY	42	O	**IO CHANNEL READY:** Active high, open drain output. When driven low, it extends host cycles to the 82595FX solution.
$\overline{\text{SBHE}}$	37	I	**SYSTEM BUS HIGH ENABLE:** Active low input indicates a data transfer on the high-byte (D8–D15) of the system bus (a 16-bit transfer). This pin also determines if the 82595FX is operating in an 8- or 16-bit system upon initialization.
INT0 INT1 INT2 INT3 INT4 INT5 INT6 INT7	29 30 31 32 33 34 35 36	O	**82595FX INTERRUPT 0–7:** One of these 8 pins is selected to be active one at a time (the other seven are in Hi-Z state) by configuration. These active high outputs serve as interrupts to the host system.
RESET DRV	19	I	**RESET DRIVE:** Active high reset signal.

2.2 Local Memory Interface

Symbol	Pin No.	Type	Name and Function
LADDR0 LADDR1 LADDR2 LADDR3 LADDR4 LADDR5 LADDR6 LADDR7 LADDR8 LADDR9 LADDR10 LADDR11 LADDR12 LADDR13 LADDR14 LADDR15	143 144 145 146 147 148 149 150 153 154 155 156 157 158 159 2	O	**LOCAL MEMORY ADDRESS (LADDR0–LADDR15):** These outputs contain the multiplexed address for the local SRAM. **FLASH ADDRESS 14–17 (LADDR0–LADDR5):** These pins control the FLASH addressing from 16K to 1M to allow paging of the FLASH in 16K spaces. These addresses are under direct control of the FLASH PAGING configuration register.
LDATA0 LDATA1 LDATA2 LDATA3 LDATA4 LDATA5 LDATA6 LDATA7	132 133 134 135 137 138 139 140	I/O	**LOCAL MEMORY DATA BUS (LDATA0–LDATA7):** The eight I/O signals, comprising the local data bus, are used to read or write data to or from the 8-bit wide SRAM. **FLASH MEMORY DATA BUS (LDATA0–LDATA7):** These signals also provide eight bits of data for accesses to an 8-bit FLASH/EPROM if these components are used.
$\overline{\text{SRAMCS}}$	13	O	**SRAM CHIP SELECT:** This active low output is the chip select to the SRAM.
$\overline{\text{LWE}}$	12	O	This active low output is the **Write Enable** to the SRAM. This pin also provides the active low **Write Enable** to the **FLASH.**
$\overline{\text{LOE}}$	16	O	This active low output is the **Output Enable** to the SRAM. This pin also provides the active low **Output Enable** control to the **FLASH.**
$\overline{\text{BOOTCS}}$	10	O	**BOOT EPROM/FLASH CHIP SELECT:** Active low output.
EEPROMCS	8	I/O	**EEPROM CS:** Active high signal. If no EEPROM is connected, this pin should be connected to V_{CC}. In this case it will function as an input to the 82595FX to indicate no EEPROM is connected.
EEPROMSK	117	O	**EEPROM SHIFT CLOCK:** This output is used to shift data into and out of the serial EEPROM.
EEPROMDO	119	O	**EEPROM DATA OUT**
EEPROMDI	118	O	**EEPROM DATA IN**

2.4 Miscellaneous Control

Symbol	Pin No.	Type	Name and Function
$\overline{SMOUT}$	18	I/O	This active LOW signal, when asserted, places the 82595FX into a Power Down mode. The 82595FX will remain in power down mode until $\overline{SMOUT}$ is unasserted. If this line is unconnected to $\overline{SMOUT}$ from the system bus, it can be used as an active low output which, when a POWER DOWN command is issued to the 82595FX, can be used to power down other external components (this output function is enabled by configuration).
J0 J1 J2	119 118 117	I I I	**JUMPER:** Input for selecting between 7 ISA IO spaces. These pins should be connected to either V_{CC} or GND or the EEPROM. The 82595FX reads the Jumper block during its initialization sequence. **J0 J1 J2 IO Address** Connected to EEPROM Configuration contained in EEPROM GND GND GND I/O Window Disabled V_{CC} GND GND 2A0h GND V_{CC} GND 280h V_{CC} V_{CC} GND 340h GND GND V_{CC} 300h V_{CC} GND V_{CC} 360h GND V_{CC} V_{CC} 350h V_{CC} V_{CC} V_{CC} 330h

2.4 JTAG Control

Symbol	Pin No.	Type	Name and Function
TDO	109	O	**JTAG TEST DATA OUT**
TMS	110	I	**JTAG TEST MODE SELECT**
TCK	111	I	**JTAG TEST CLOCK**
TDI	112	I	**JTAG TEST DATA IN**

2.5 Serial Interface

Symbol	Pin No.	Type	Name and Function
TRMT	122	O	Positive side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out A).
$\overline{TRMT}$	123	O	Negative side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out B).
RCV	115	I	The positive input to a differential amplifier connected to the RCV pair of the AUI cable (Data In A). It is driven with 10 Mb/s Manchester Encoded data.

2.5 Serial Interface (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RCV}$	116	I	The negative input to a differential amplifier connected to the RCV pair of the AUI cable (Data In B). It is driven with 10 Mb/s Manchester Encoded data.
CLSN	124	I	The positive input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In A).
$\overline{CLSN}$	125	I	The negative input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In B).
TDH	105	O	**TRANSMIT DATA HIGH:** Active high Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, $\overline{TDH}$, and $\overline{TDL}$ to generate the pre-conditioned twisted pair output waveform.
TDL	106	O	**TRANSMIT DATA LOW:** Twisted Pair Output Driver. Active high Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDH, $\overline{TDH}$, and $\overline{TDL}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{TDH}$	103	O	**TRANSMIT DATA HIGH INVERT:** Active low Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{TDL}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{TDL}$	104	O	**TRANSMIT DATA LOW INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{TDH}$ to generate the pre-conditioned twisted pair output waveform.
RD	114	I	Active high Manchester Encoded data received from the twisted pair.
$\overline{RD}$	113	I	Active low Manchester Encoded data received from the twisted pair.
X1	127	I	**20 MHz CRYSTAL INPUT:** This pin can be driven with an external MOS level clock when X2 is left floating. This input provides the timing for all of the 82595FX functional blocks.
X2	128	O	**20 MHz CRYSTAL OUTPUT:** If X1 is driven with an external MOS level clock, X2 should be left floating.

2.6 Serial Interface LEDs

Symbol	Pin No.	Type	Name and Function
AUI LED/BNC DIS	95	O	**AUI LED INDICATOR:** This output, when the 82595FX is used as a TPE/AUI solution, will turn on an LED when the 82595FX is actively interfaced to its AUI serial port. When the 82595FX is used as a BNC/AUI solution, this output becomes the **BNC DIS** output, which can be used to power down the BNC Transceiver section (the Transceiver and the DC to DC Converter) of the solution when the BNC port is unconnected.
LILED	98	O	**LINK INTEGRITY LED:** Normally on (low) ouput which indicates a good link integrity status when the 82595FX is connected to an active TPE port. This output will remain on when the Link Integrity function has been disabled. It turns off (driven high) when Link Integrity fails, or when the 82595FX is actively interfaced to an AUI port. The minimum off time is 100 ms.

2.6 Serial Interface LEDs (Continued)

Symbol	Pin No.	Type	Name and Function
ACTLED	97	O	**LINK ACTIVITY LED:** Normally off (high) output turns on to indicate activity for transmission, reception, or collision. Flashes at a rate dependent on the level of activity on the link.
POLED	96	O	**POLARITY LED:** If the 82595FX detects that the receive TPE wires are reversed, the POLED will turn on (low) to indicate the fault. POLED remains on even if automatic polarity correction is enabled, and the 82595FX has automatically corrected for the reversed wires.

2.7 Power and Ground

Symbol	Pin No.	Type	Name and Function
V_{CC}	1, 3, 7, 15, 26, 28, 40, 43, 46, 50, 57, 80, 84, 91, 99, 101, 107, 121, 129, 131, 141, 152	I	**POWER:** +5V ±5%.
V_{SS}	4, 6, 9, 11, 14, 17, 25, 27, 38, 39, 41, 44, 48, 52, 55, 59, 79, 82, 86, 89, 93, 100, 102, 108, 120, 126, 130, 136, 142, 151	I	**GROUND:** 0V.

2.8 Reserved Pins

Symbol	Pin No.	Type	Name and Function
N/C	5, 160		Reserved. Do not connect.

2.9 82595FX Pin Summary

ISA Bus Interface

ISA Pin Name	Pin Type	P-Down State
SA0–SA3 (In)		Inactive
SA4–SA11		Inactive/Act(1)
SA14–19 (In)		Inactive
SD0–SD15 (I/O)	TS	TS
$\overline{\text{SMEMR}}$ (In)		Inactive
$\overline{\text{SMEMW}}$ (In)		Inactive
$\overline{\text{IOR}}$ (In)		Inactive
$\overline{\text{IOW}}$ (In)		Inactive/Act(1)
INT0–7 (Out)	TS	TS
RESET DRV (In)		Act
$\overline{\text{IOCS16}}$ (Out)	OD	TS
IOCHRDY (Out)	OD	TS
$\overline{\text{SBHE}}$ (In)		Inactive
AEN (In)		Inactive/Act(1)

NOTE:
1. For hardware powerdown using $\overline{\text{SMOUT}}$, these pins will be inactive. For software powerdown, these pins remain active.

Local Memory Interface

Pin Name	MUXed Name	Pin Type	P-Down
LADDR[5:0] (Out)	FADDR[14:19]	2S	TS
LADDR[6:15] (Out)		2S	TS
LDATA[0:7] (I/O)		TS	TS
$\overline{\text{LWE}}$ (Out)		2S	TS
$\overline{\text{LOE}}$ (Out)		2S	TS
$\overline{\text{BOOTCS}}$ (Out)		2S	PU
$\overline{\text{SRAMCS}}$ (Out)		2S	PU
EEPROMCS (I/O)		TS	PD

Miscellaneous Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State	Dual Pin Name
J0(In)			ACT	EEPROM2D0 (In)
J1 (I/O)		TS	TS	EEPROM2DI (Out)
J2 (I/O)		TS	TS	EEPROM2SK (Out)
$\overline{\text{SMOUT}}$ (I/O)		TS	ACT/TS	

JTAG Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TMS (In)			In Act
TCK (In)			In Act
TDI (In)			In Act
TDO (Out)		TS	

Serial Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TRMT (Out)		Ana	TS
$\overline{\text{TRMT}}$ (Out)		Ana	TS
RCV (In)		Ana	In Act
$\overline{\text{RCV}}$ (In)		Ana	In Act
CLSN (In)		Ana	In Act
$\overline{\text{CLSN}}$ (In)		Ana	In Act
TDH (Out)		Ana	TS
TDL (Out)		Ana	TS
$\overline{\text{TDH}}$ (Out)		Ana	TS
$\overline{\text{TDL}}$ (Out)		Ana	TS
RD (In)		Ana	In Act
$\overline{\text{RD}}$ (In)		Ana	In Act
X1 (In)			In Act
X2 (Out)		2S	TS
LILED (Out)		2S	TS*
POLED (Out)		2S	TS*
ACTLED (Out)		2S	TS*
AUILED (Out)	BNC DIS (Out)	2S	TS*

*Assuming auto-negotiation disabled.

Legend:
TS—TriState.
OD—Open Drain.
2S—Two State, will be found in either a 1 or 0 logic level.
Ana—Analog pin (all serial interface signals).
Act—Input buffer is active during Power Down.
In Act—Input buffer is inactive during Power Down.
PU—Output in inactive state with weak internal Pull-up during Power Down.
PD—Output in inactive state with weak internal Pull-down during Power Down.
Dual—Dual function pin.

3.0 82595FX INTERNAL ARCHITECTURE OVERVIEW

Figure 1 shows a high level block diagram of the 82595FX. The 82595FX is divided into four main subsections; a system interface, a local memory sub-system interface, a CSMA/CD unit, and a serial interface.

3.1 System Interface Overview

The 82595FX's system interface subsection includes a glueless ISA bus interface, and the 82595FX's IO registers (including the 82595FX's command, status, and Data In/Out registers). The system interface block also interfaces with the 82595FX's local memory interface subsystem and CSMA/CD subsystem.

The bus interface logic provides the control, address, and data interface to an ISA compatible bus. The 82595FX decodes up to 1M of total memory address space. Address decoding within 16K block increments (A14–A19) are used for Flash or Boot EPROM. IO accesses are decoded throughout the 1 Kbyte PC IO address range (A10 and A11 provide up to 4K of IO addressing and are used for Plug N' Play). The 82595FX data bus interface provides either an 8- or 16-bit interface to the host system's data bus. The control interface provides complete handshaking interface with the system bus to enable transfer of data between the 82595FX solution and the host system.

The 82595FX's IO registers provide 3 banks of directly addressable registers which are used as the control and data interface to the 82595FX. There are 16 IO registers per bank, with only one bank enabled at a time. This allows the complete 82595FX software interface to be contained in one 16-byte IO space. The base address of this IO space is selectable via either software (which can be stored in a serial EEPROM), or by strapping the 82595FX IO Jumper block (J0–J2). The 82595FX can also detect conflicts to its base IO space, and automatically resolve these conflicts either by allowing the selection of one Plug N' Play card from multiple cards (using Plug N' Play software), or by mapping itself into an un-used IO space (Automatic IO Resolution). Included in the 82595FX IO registers are the Command Register, the Status Register, and the Local Memory IO Port register, which provides the data interface to the local SRAM buffer contained in an 82595FX solution. Functions such as IO window mapping, Interrupt enable, RCV and XMT buffer initialization, etc. are also configured and controlled through the IO registers.

3.1.1 CONCURRENT PROCESSING FUNCTIONALITY

The 82595FX's Concurrent Processing feature significantly enchances data throughput performance by performing both system bus and serial link activities concurrently. Transmission of a frame is started by the 82595FX before that frame is completely copied into local memory. During reception, a frame is processed by the host CPU before that frame is entirely copied to local memory. Transmit Concurrent Processing feature is enabled by writing to BANK 2, Register 1, Bit 0. A 1 written to this bit enables this functionality, a 0 (default) disables it. To enable Receive Concurrent Processing, BANK 1, Register 7 must be programmed to value other than 00h (00h disables RCV Concurrent Processing, and is default). (See Section 4.1 for the format of IO BANK 1 and 2.) Improvements in concurrent processing functionality have allowed the 82595FX to include enhancements to the throughput efficiency of the 82595TX. For details, refer to the 82595FX User's Guide. Concurrent Processing is not recommended for 8-bit interfaces. For more information on Transmit and Receive Concurrent Processing, refer to Section 7.0 and Section 8.0.

3.2 Local Memory Interface

The 82595FX's local memory interface includes a DMA unit which controls data transfers to or from the 82595FX's local SRAM, control for access to a Boot EPROM/FLASH, and two interfaces to a serial EEPROM. The local memory interface subsection also arbitrates accesses to the local memory by the host CPU and the 82595FX.

Data transfers between the 82595FX and the local SRAM are always through the 82595FX's Local Memory 16-bit/32-bit IO Port. This allows the entire SRAM memory (up to 64 Kbytes) to be mapped into one IO location in the host systems IO map. By setting a configuration bit in the 82595FX's IO Registers (32IO/HAR#), the local memory can be extended from 16 bits to a full 32 bits. During 32-bit accesses, the CPU would perform a doubleword access addressed to register 12 of BANK0. The ISA bus will break this access up into two 16-bit accesses to Registers 12/13 followed by Registers 14/15, (or 4 sequential 8-bit accesses in an 8-bit interface). The CPU always accesses the 82595FX IO Port for Receive or Transmit data transfers, while the 82595FX automatically increments the address to the SRAM after each CPU access. The SRAMs data path is an 8-bit interface (typically 64K by 8-bits wide, or 256K by 8-bits wide) to allow for the lowest possible solution cost. The 82595FX implements a

prefetch mechanism to the local SRAM so that the data is always available to the CPU as either an 8- or 16-bit word. In the case of the CPU reading from the SRAM, the 82595FX reads the next two bytes from the SRAM, the 82595FX between CPU cycles so that the data is always available as a word in the 82595FX's Local Memory IO Port register. In the case of the CPU writing to the SRAM, the data is written into the 82595FX's Local Memory IO Port then transferred to the SRAM by the 82595FX between CPU cycles. This prefetch mechanism of the 82595FX allows for IO read and writes to the local memory to be performed with no additional wait-states (3 clocks per data transfer cycle).

The DMA unit provides addressing and control to move RCV or XMT data between the 82595FX and the local SRAM. For transmission, the CPU is required only to copy the data to the local memory, initialize the 82595FX's DMA Current Address Register (CAR) to point to the beginning of the frame, and issue a Transmit Command to the 82595FX. The DMA unit facilitates the transfers from the local memory to the 82595FX as transmission takes place. The DMA unit will reset upon collision during a transmission, enabling automatic re-transmission of the transmit frame. During reception, the DMA unit implements a recyclable ring buffer structure which can receive continuous back to back frames without CPU intervention on a per frame basis (see Section 8.2 for details).

The 82595FX provides address decoding and control to allow access to an external Boot EPROM/FLASH if these components are utilized in an 82595FX design. The 82595FX also provides an interface to a serial EEPROM to replace jumper blocks used to contain configuration information. This port is used to store configuration information and in addition, it is used to store Plug N' Play information as defined in the Plug N' Play Specification.

The 82595FX arbitrates accesses to the local memory sub-system by the CPU and the 82595FX. The arbitration unit will hold off an 82595FX DMA cycle to the local memory if a CPU cycle is already in progress. Likewise, it will hold off the CPU if an 82595FX cycle is already in progress. The cycle which is held off will be completed on termination of the preceding cycle.

3.3 CSMA/CD Unit

The CSMA/CD unit implements the IEEE 802.3 CSMA/CD protocol. It performs such functions as transmission deferral to link traffic, interframe spacing, exponential backoff for collision handling, address recognition, etc. The CSMA/CD unit serves as the interface between the local memory and the serial interface. It serializes data transferred from the local memory before it is passed to the serial interface unit for transmission. During frame reception, it converts the serial data received from the serial interface to a byte format before it is transferred to local memory. The CSMA/CD unit strips framing parameters such as the Preamble and SFD fields before the frame is passes to memory for reception. For transmission, the CSMA/CD unit builds the frame format before the frame is passed to the serial interface for transmission.

3.4 Serial Interface

The 82595FX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also interface to a transceiver device to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595FX automatically enables either to the AUI or TPE interface depending on which medium is connected to the chip. Software configuration can override this automatic selection.

4.0 ACCESSING THE 82595FX

All access to the 82595FX is made through one of three banks of IO registers. Each bank contains 16 registers. Each register in a bank is directly accessible via addressing. Through the use of bank switching, the 82595FX utilizes only 16 IO locations in the host system's IO map to access each of its registers. The different banks are accessed by setting the POINTER field in the 82595FX Command Register to select each bank. The Command Register is Register for each bank.

4.1 82595FX Register Map

The 82595FX registers are contained in three banks of 16 IO registers per bank. These three banks are shown in the following three pages.

4.1.1 IO BANK 0

The format for IO Bank 0 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
RCV States		EXEC States		EXEC INT	TX INT	RX INT	RX STP INT	Reg 1
(Counter)		ID REGISTER 1	(Auto En)	0	1	0 RESERVED	0	Reg 2
0 Resvrd	0 Resvrd	Cur/$\overline{\text{Base}}$	32 IO/$\overline{\text{HAR}}$	EXEC Mask	TX Mask	RX Mask	RX STP Mask	Reg 3
RCV CAR/BAR (Low)								Reg 4
RCV CAR/BAR (High)								Reg 5
RCV STOP REG (Low)								Reg 6
RCV STOP REG (High)								Reg 7
RCV Copy Threshold REG								Reg 8
EARLY XMT THRESHOLD REGISTER (XTR)								Reg 9
XMT CAR/BAR (Low)								Reg 10
XMT CAR/BAR (High)								Reg 11
Host Address Reg (Low) /32-Bit I/O (Byte 0)								Reg 12
Host Address Reg (High) /32-Bit I/O (Byte 1)								Reg 13
Local Memory I/O Port (Low) /32-Bit I/O (Byte 2)								Reg 14
Local Memory I/O Port (High) /32-Bit I/O (Byte 3)								Reg 15

4.1.2 IO BANK 1

The format for IO Bank 1 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
$\overline{\text{Tri-ST}}$ INT	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	Host Bus Wd	0 Resvrd	Reg 1
FL/$\overline{\text{BT}}$ Present	Boot EPROM/FLASH Decode Window			Bad IRQ	INT Select			Reg 2
0	0	I/O Mapping Window						Reg 3
0	0	0	0	0	0	0	0	Reg 4
(Reserved)								
0	0	0	0	0	0	0	0	Reg 5
(Reserved)								
BACK TO BACK TRANSMIT IFS								Reg 6
RCV BOF Threshold REG								Reg 7
RCV LOWER LIMIT REG (High Byte)								Reg 8
RCV UPPER LIMIT REG (High Byte)								Reg 9
XMT LOWER LIMIT REG (High Byte)								Reg 10
XMT UPPER LIMIT REG (High Byte)								Reg 11
FLASH SELECT	PAGE HIGH	FLASH WRITE ENABLE		FLASH PAGE SELECT				Reg 12
0	0	0	0	0	$\overline{\text{SMOUT}}$ OUT EN	0 Resvrd	0 Resvrd	Reg 13
(Reserved)								
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.1.3 IO BANK 2

The format for IO Bank 2 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
Disc Bad Fr	Tx Chn $\overline{\text{ErStp}}$	Tx Chn Int Md	Res 0	0	0 (Reserved)	0	TX Con Proc En	Reg 1
LoopBack		Multi IA	No SA Ins	Length $\overline{\text{Enable}}$	RX CRC In MEM	BC DIS	PRMSC Mode	Reg 2
Test 1	Test 2	BNC/ $\overline{\text{TPE}}$	$\overline{\text{APORT}}$	Jabber Disable	TPE/ $\overline{\text{AUI}}$	Pol $\overline{\text{Corr}}$	Link In Dis	Reg 3
INDIVIDUAL ADDRESS REGISTER 0								Reg 4
INDIVIDUAL ADDRESS REGISTER 1								Reg 5
INDIVIDUAL ADDRESS REGISTER 2								Reg 6
INDIVIDUAL ADDRESS REGISTER 3								Reg 7
INDIVIDUAL ADDRESS REGISTER 4								Reg 8
INDIVIDUAL ADDRESS REGISTER 5								Reg 9
STEPPING			Turnoff Enable	EEDO	EEDI	EECS	EESK	Reg 10
RCV NO RESOURCE COUNTER								Reg 11
Reserved 0								Reg 12
Polarity $\overline{\text{LED}}$	Link $\overline{\text{LED}}$	Activity $\overline{\text{LED}}$	0 (Resvrd)	Auto-Negotiation Status		A-N Enable	FDX/ $\overline{\text{HDX}}$	Reg 13
0	0	0	0 (Reserved)	0	0	0	0	Reg 14
0	0	0	0 (Reserved)	0	0	0	0	Reg 15

4.2 Writing to the 82595FX

Writing to the 82595FX is accomplished by an IO Write instruction (such as an OUT instruction) from the host processor to one of the 82595FX registers. The 82595FX registers reside in a block of 16 contiguous addresses contained within the PC IO address space. The mapping of this address block is programmable throughout the 1 Kbyte PC IO address map.

The 82595FX registers are contained within three banks of IO registers. When writing to a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once a bank is selected, all register accesses are made in that bank until a switch to another bank is performed. Switching banks is accomplished by writing to the PTR field of Reg 0 in any bank. Reg 0 is the command register of the 82595FX and its functionality is identical in each bank. Once in the appro-

priate bank, the processor can write directly to any of the 82595FX registers by simply issuing an OUT instruction to the IO address of the register.

4.3 Reading from the 82595FX

Reading from the 82595FX is accomplished by an IO Read instruction (such as an IN instruction) from the host processor to one of the 82595FX registers. When reading from a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once in the appropriate bank, the processor can read directly from any of the 82595FX registers by simply issuing an IN instruction to the IO address of the register.

4.4 Local SRAM Accesses

IO mapping the local SRAM memory of an 82595FX solution allows it to appear as simply an IO Port to the host system. This allows an 82595FX solution to work in PCs which do not have enough space in their system memory map to accommodate the addition of LAN buffer memory (typically 16 Kbytes to 64 Kbytes) into the map. The entire local memory (up to 64 Kbytes) is mapped into one 16-bit IO Port location. For all IO-mapped accesses to the local memory of a 82595FX solution, the 82595FX performs the IO address decoding and the ISA Bus interface handshake and asserts the address and control signals to the local memory.

4.4.1 WRITING TO LOCAL MEMORY

The local memory of an 82595FX solution is written to whenever the host CPU performs a Write operation to the 82595FX Local Memory IO Port. Prior to writing a block of data to the local memory, the CPU should update the 82595FX Host Address Register with the first address to be written. The CPU then copies the data to the local memory by writing it to the 82595FX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595FX upon completion of each write cycle. This allows sequential accesses to the local memory, even though the IO port address accessed does not change.

4.4.2 READING FROM LOCAL MEMORY

The local memory of an 82595FX solution is read from whenever the host CPU performs a Read operation from the 82595FX Local Memory IO Port. Prior to reading a block of data from the local memory, the CPU should utilize the 82595FX Host Address Register to point to first address to be read. The CPU then reads the data from the local memory through the 82595FX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82596FX upon completion of each read cycle.

4.5 Serial EEPROM Interface

A Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82595FX. The use of an EEPROM enables 82595FX designs to be implemented without jumpers (the use of jumpers to select IO windows is optional.) The port interface to the serial EEPROM provides both configuration and Plug N' Play information access. Plug N' Play allows peripheral functions to be added to a PC (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). Information describing system resources are contained within the 82595FX configuration registers. This allows Auto-configuration software, which is usually contained in the BIOS or O/S, to identify system resource usage, identify conflicts and automatically re-configure the 82595FX.

The 82595FX automatically accesses Register 0 of the EEPROM upon a RESET in ISA Bus Interface mode. Register 0 contains the information that the 82595FX must be configured to allow CPU accesses to it (IO Mapping Window, FLASH Detect Enable, Auto I/O Enable, Boot EPROM/FLASH Window, Host Bus Width, and Plug N' Play Enable) following a system boot. The format for EEPROM Register 0 is shown in Figure 4-1. Note that all 0's are assumed to be reserved. In the case where an EEPROM is either unprogrammed (each bit defaults to a 1) or completely erased (all 0's), the 82595FX will default to IO Address 300h.

Word0, Bit 1, the Word 1 Enable bit, is asserted to enable the read of EEPROM Word 1 during reset. This bit is active high.

NOTE:
If Word 1 of the EEPROM is not to be read during a reset, software must wait 200 μs after the reset is issued before accessing the 82595FX, as was the case on all versions of the 82595. If Word 1 is to be read during a reset, software must wait 400 μs after reset before accessing the part. During this "blackout" period, the part will not respond to accesses on the ISA bus.

Word 0, Bit 8, is the Flash Present bit. This bit is active low to indicate the presence of flash memory, as in the 82595FX B-3. The functionality of the bit is changed from the 82595FX B-2 and prior versions. Word 0, Bit 9 is the Auto-Negotiation, or A-N, Enable bit for the negotiation process at boot time. The bit is active high.

Word 1 of the EEPROM is used to store the INT Select value to which the part will default on reset. The mapping from INT Select to IRQ is explained later in this document. The value stored in bits 0 through 2 of word 1 of the EEPROM is loaded into the INT Select register of the 82595FX, bank 1, register 2, bits 0 through 2 on any hardware or software reset. The reading of Word 1 on reset is enabled when bit 1 of word 0 of the EEPROM is set. If this bit is not set on reset, word 1 will not be read and the INT select register and Bad IRQ bit in bank 1 will be initialized to zero.

For additional information regarding a Plug N' Play implementation for the 82595FX, please consult the 82595FX User's Guide and LAN595TX Specification, available through your local sales representative. The latest Plug N' Play Specification is available by Microsoft.

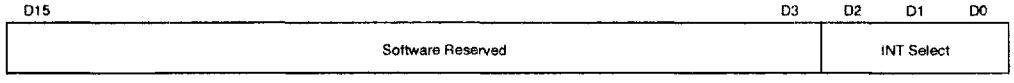


Figure 4-1. EEPROM Register 0

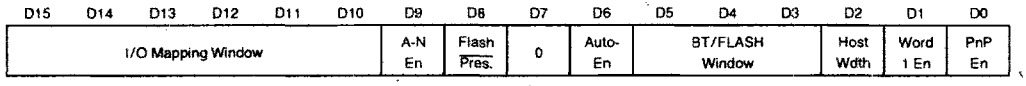


Figure 4-2. EEPROM Register 1

4.6 Boot EPROM/FLASH Interface

The Boot EPROM/FLASH of an 82595FX solution is read from or written to (FLASH only) whenever the host CPU performs a Read or a Write operation to a memory location that is within the Boot EPROM/FLASH mapping window. This window is programmable throughout the ISA PROM address range (C8000–DFFFF) by configuring the 82595FX Boot EPROM Decode Window register (Bank 1, Register 2, bits 4–6). The 82595FX asserts the BOOTCS# signal when it decodes a valid access. Up to 1 MBytes of FLASH can be addressed by the 82595FX.

5.0 COMMAND AND STATUS INTERFACE

The format for the 82595FX Command Register is shown in Figure 5-1. The Command Register resides in Register 0 of each of the three IO Banks of the 82595FX, and can be accessed in any of these banks. The Command Register is accessed by writing to or reading from the IO address for Register 0.

5.1 Command OP Code Field

Bits 0 through 4 of the Command Register comprise the Command OP Code field. A command is issued to the 82595FX by writing it into the Command OP Code field. A command can be issued to the 82595FX at any time; however in certain cases the command may be ignored (for example, issuing a Transmit command while a Transmit is already in progress). In these cases the command is not performed, and no interrupt will result from it.

The Command OP Code field can also be read. In this case it will indicate an execution status event other than TRANSMIT DONE (TDR Done, DIAGNOSE Done, MC-SETUP Done, DUMP Done, INIT Done, and POWER-UP) has been completed. This field is valid only when the EXEC INT bit (Bank 0, Reg 1, Bit 3) is set.

5.2 ABORT (Bit 5)

This bit indicates if an execution command other than TRANSMIT was aborted while in progress. This bit provides status information only. It should be written to a 0 whenever the Command Register is written to.

5.3 Pointer Field (Bits 6 and 7)

The Pointer field controls which 82595FX IO register bank is currently to be accessed (Bank 0, Bank 1, or Bank 2). Writing a 00:b to the Pointer field selects Bank 0, 01:b for Bank 1, and 10:b for Bank 2. The Pointer field is valid only when the SWITCH BANK (0h) command is issued. This field will be ignored for any other command. The 82595FX will continue to operate in a current bank until a different bank is selected. Upon power up of the device or Reset, the 82595FX will default to Bank 0.

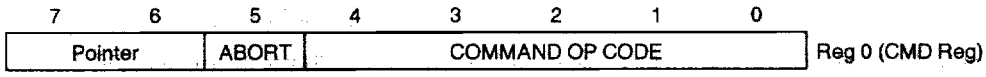


Figure 5-1. 82595FX Command Register

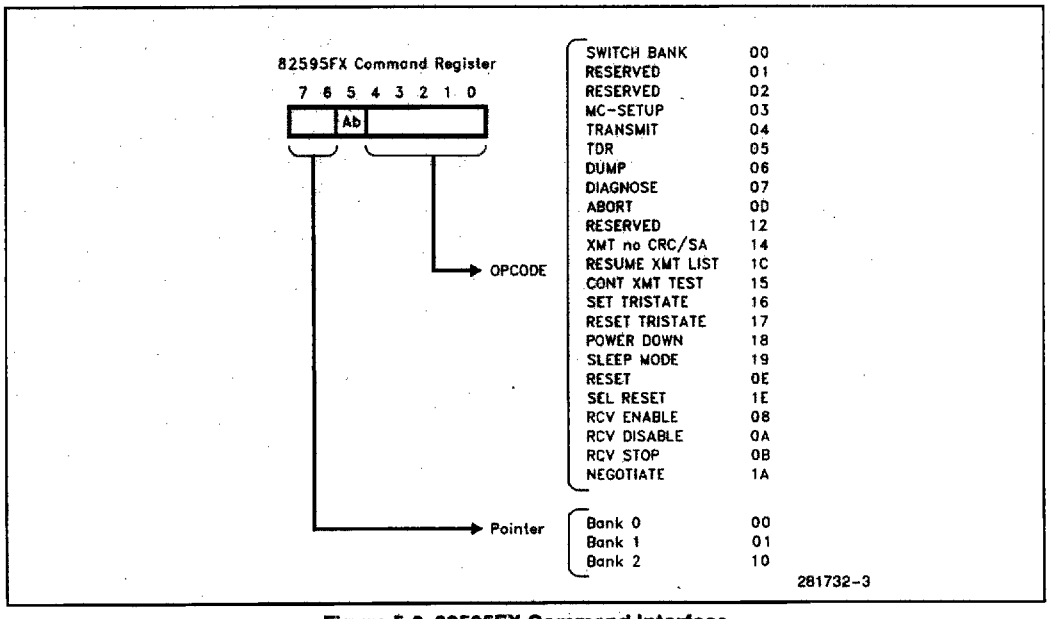


Figure 5-2. 82595FX Command Interface

5.4 82595FX Status Interface

The Status of the 82595FX can be read from Register 1 of Bank 0, with additional status information contained in Register 0 (the Command Register). Figure 5-3 shows these registers. Other information concerning the configuration and initialization of the 82595FX and its registers can be obtained by directly reading the 82595FX registers.

When read, the Command OP Code field indicates which event (MC Done, Init Done, TDR Done, or DIAG Done) has been completed. This field is valid only when the EXEC INT Bit (Bank 0, Reg 1, Bit 3) is set to a 1. Reading the Pointer field indicates which bank the 82595FX is currently operating in. Register 1 in Bank 0 contains the 82595FX interrupts status as well as the current states of the RCV and Execution units of the 82595FX. Resultant status from events such as the completion of a transmission or the reception of an incoming frame is contained in the status field of the memory structures for these particular events.

6.0 INITIALIZATION

Upon either a software or hardware RESET, the 82595FX enters into its initialization sequence. When the 82595FX is interfaced to an ISA bus, the 82595FX reads information from its EEPROM and Jumper block (if utilized) which configures critical parameters (IO Address mapping, etc.) to allow initial accesses to the 82595FX during the host system's initialization sequence and also access by the software device driver. The 82595FX can also be configured (via the EEPROM) to automatically resolve any conflicts to its IO address location either by moving its IO address offset to an unused location in the case that a conflict occurs, or by using the Plug N' Play Software to the I/O address location. This process eliminates a large majority of LAN end-user setup problems.

The 82595FX can be configured to operate with ISA systems that require early deassertion of the IOCHRDY signal to its low (not ready) state. The 82595FX, along with its software driver, can perform a test at initialization to determine if early IOCHRDY deassertion is required.

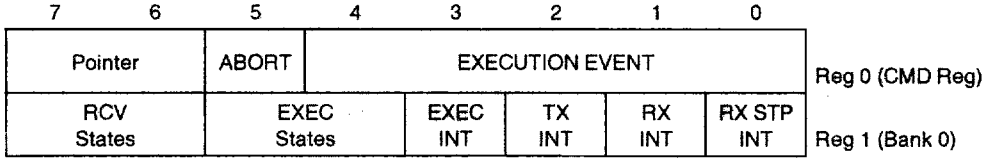


Figure 5-3. 82595FX Status Information

7.0 FRAME TRANSMISSION

The 82595FX performs all of the necessary functions needed to transmit frames from its local memory. If Transmit Concurrent Processing is enabled, the CPU must only program the Base and Host Address Register with the starting address to be transmitted, copy a portion of the frame into the 82595FX's transmit buffer located in local memory (the number of bytes for this first portion is determined by the software driver without causing an Underrun), issue a XMT command to the 82595FX, and complete the data copies for this frame to local memory. If Transmit Concurrent Processing is disabled, the CPU must copy an entire frame into the 82595FX's transmit buffer located in local memory, set up the 82595FX's Current Address Registers to point to that frame, and issue a XMT command to the 82559TX. The 82595FX performs all the link management functions, DMA operations, and statistics keeping to handle transmission onto the link and communicate the status of the transmission to the CPU. The 82595FX performs automatic retransmission on collision with no CPU interaction.

7.1 82595FX XMT Block Memory Format

The format in which a XMT block is written to memory by the CPU is shown in Figure 7-1 for a 16-bit interface. Figure 7-2 shows this structure for an 8-bit interface.

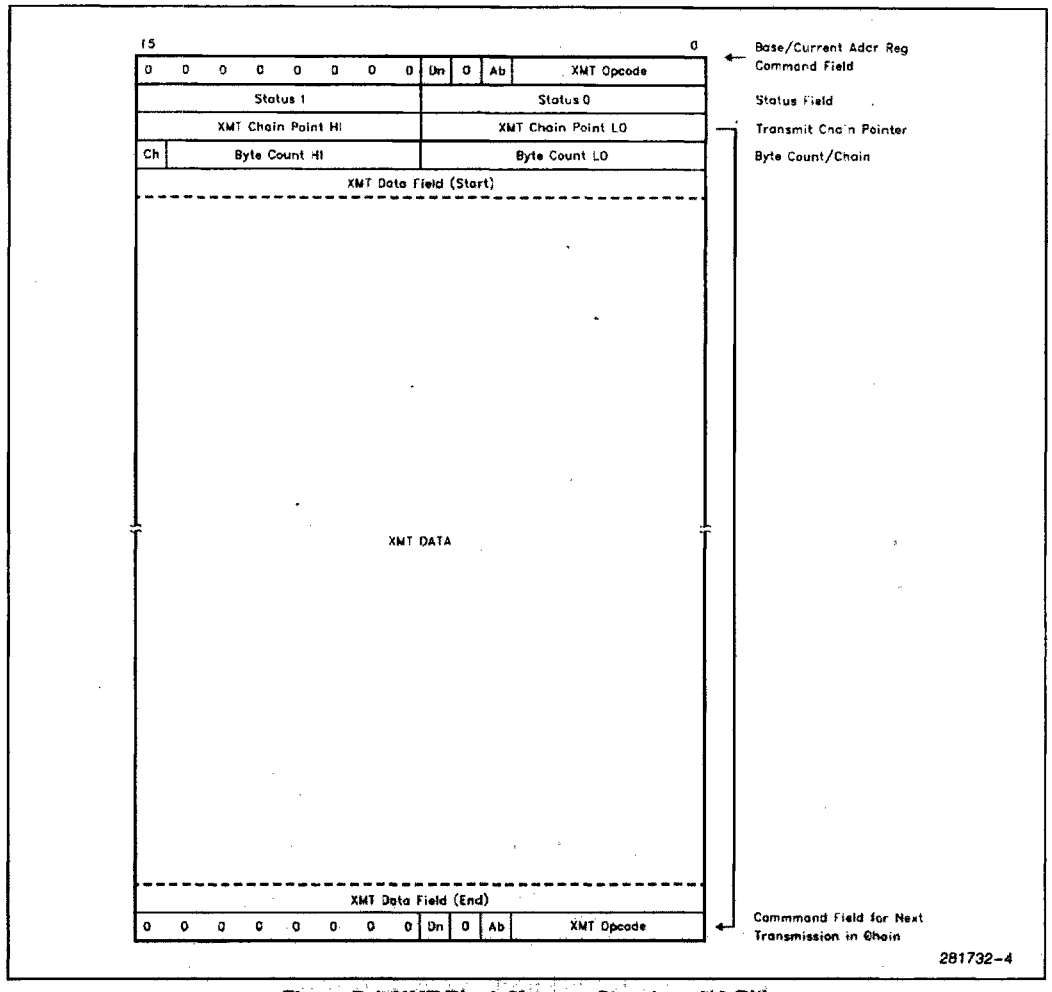


Figure 7-1. XMT Block Memory Structure (16-Bit)

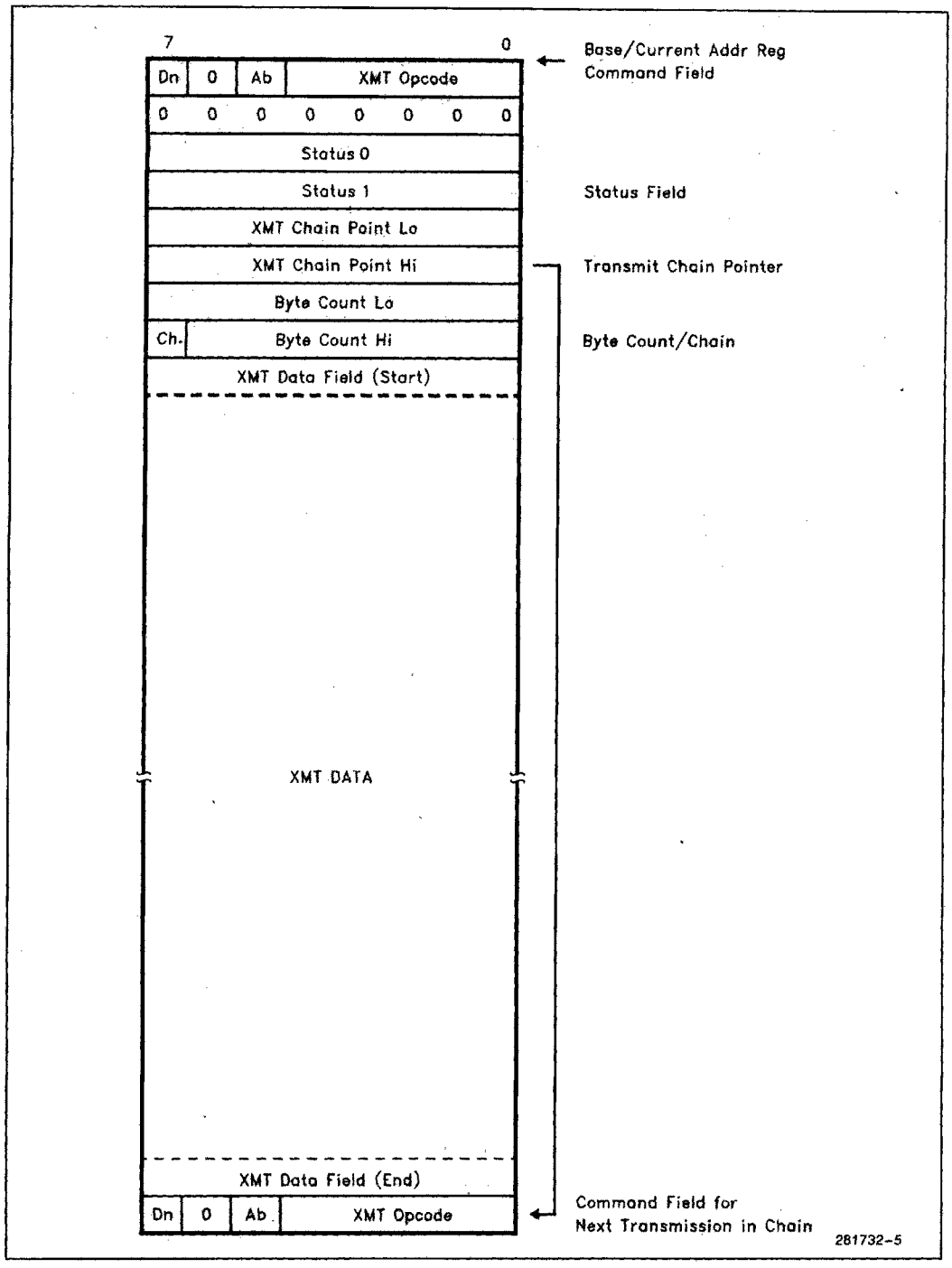


Figure 7-2. XMT Block Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 7-3. In a 16-bit wide interface, these two bytes will combine to form one word. This field is originally set to all 0's by the CPU as the XMT block is copied to memory. It is updated by the 82595FX upon completion of the transmission.

7.2 XMT Chaining

The 82595FX can transmit consecutive frames without the CPU having issued a separate Transmit command for each frame. This is called Transmit Chaining. The 82595FX Transmit Chaining memory structure for a 16-bit interface is shown in Figure 7-4, with an 8-bit interface shown in Figure 7-5. The 82595FX registers which control the memory structure are also shown. The CPU places multiple XMT blocks in the Transmit buffer. The 82595FX will transmit each frame in the chain, reporting the status for each frame in its status field. If Concurrent Processing is enabled, the copy of additional frames in a chain will take place while the first portion of the chain (one or more frames) is being transmitted by the 82595FX. This chain can be dynamically updated by the CPU to add more frames to the chain. The transmit chain can be configured to terminate upon an errored frame (maximum collisions, underrun, lost CRS, etc.) or it can continue to the next frame in the chain. The 82595FX can be configured to interrupt upon completion of each transmission or to interrupt at the end of the transmit chain only (it always interrupts upon an errored condition).

7	6	5	4	3	2	1	0	
TX DEF	HRT BET	MAX COL	X	No OF COLLISIONS				Status 0
COLL	X	TX OK	0	LTCOL	LST CRS	X/JERR(1)	UND RUN	Status 1

NOTE:
1. Only functional in full duplex operations.

Figure 7-3. Transmit Result

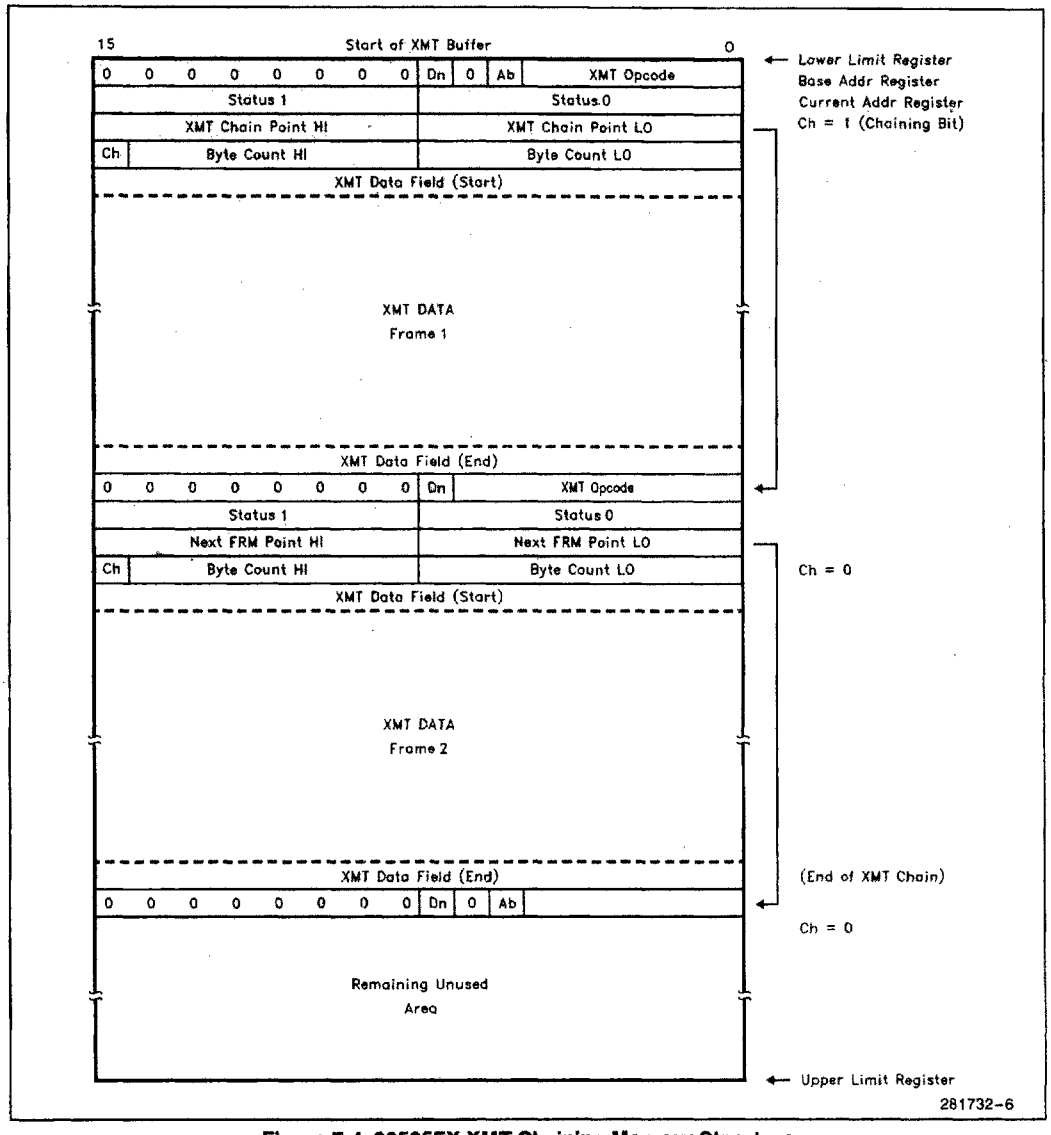


Figure 7-4. 82595FX XMT Chaining Memory Structure

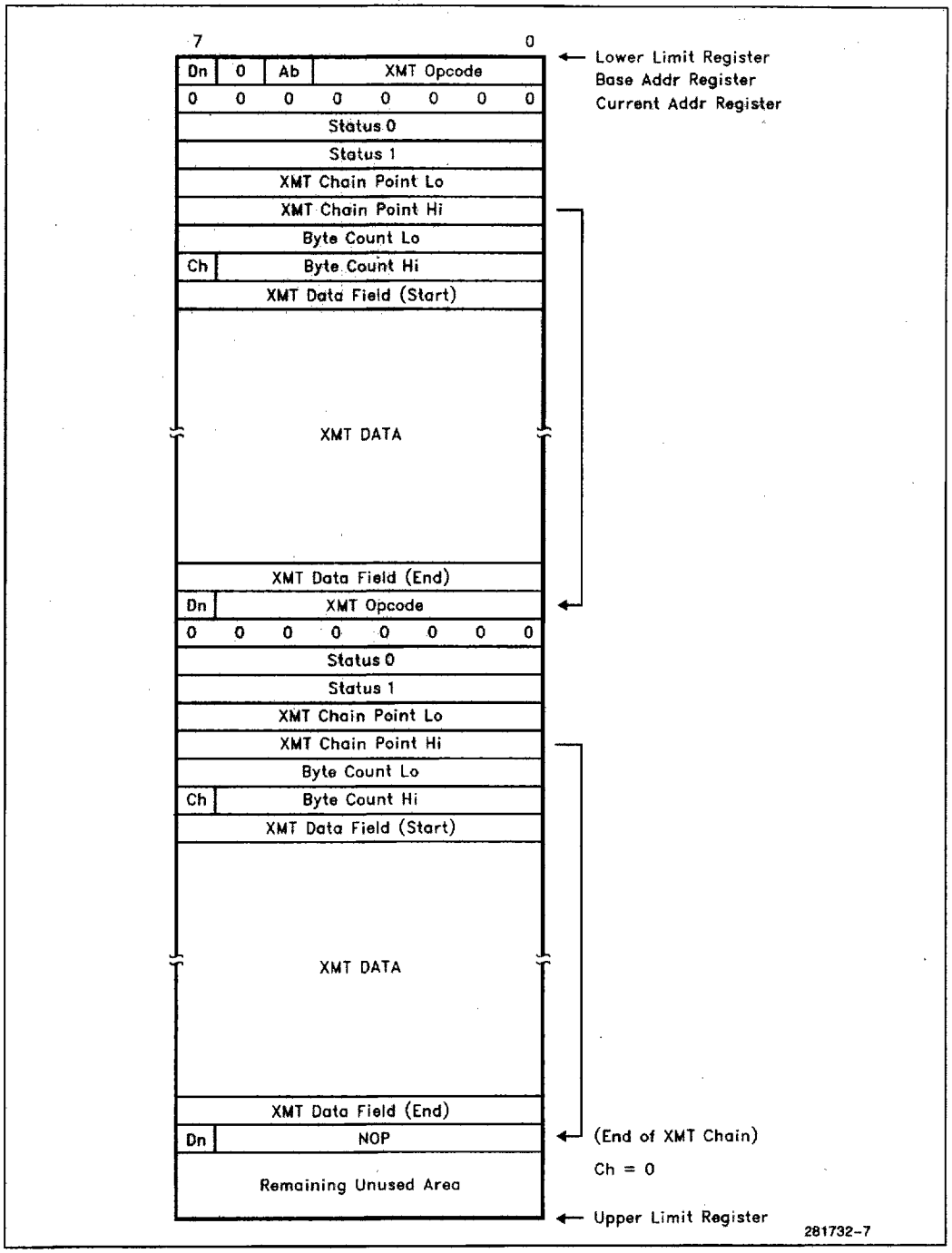


Figure 7-5. XMT Block Memory Structure (8-Bit)

7.3 Automatic Retransmission on Collision

The 82595FX performs automatic retransmission when a collision is experienced within the first slot time of the transmission with no intervention by the CPU. The 82595FX performs jamming, exponential backoff, and retransmission attempts as specified by the IEEE 802.3 spec. The 82595FX reaccesses its local memory automatically on collision. This allows the 82595FX to retransmit up to 15 times after the initial collision with no CPU interaction.

The 82595FX reaccesses the data in its transmit buffer by simply resetting the value of its Current Address Register back to the value of the Base Address Register (the beginning of the XMT block) and repeating the DMA process to access the data in the transmit buffer again. Once it regains access to the link, retransmission is attempted. When Transmit Chaining is utilized, the process for retransmission is exactly the same. Only the current frame in the chain will be retransmitted, since the Base Address Register is updated upon transmission of each frame.

8.0 FRAME RECEPTION

The 82595FX implements a recyclable ring buffer DMA structure to support the reception of back to back incoming RCV frames with minimal CPU overhead. The structure of the RCV frames in memory is optimized to allow the CPU to process each frame with as few software processing steps as possible. The frame format is arranged so that all of the required infomation for each frame (status, size, etc.) is located at the beginning of the frame.

8.1 82595FX RCV Memory Structure

The 82595FX RCV memory structure for a 16-bit interface is shown in Figure 8-1. Figure 8-2 shows this structure for the 8-bit interface. Once an incoming frame passes the 82595FX's address filtering, the 82595FX deposits the frame into the RCV Data field of the RCV Memory Structure. The fields which precede the RCV Data field, Event, Status, Byte Count, Next Frame Pointer, and the Event field of the following frame, are updated upon the end of the frame after all of the incoming data has been deposited in the RCV Data field. If Receive Concurrent Processing is enabled, the CPU processes the receive frame without the entire frame being deposited by the 82595FX to the RCV Data Field. The 85295FX, along with the software driver, determines the portion of the frame being copied to host memory before the rest of that frame is copied to local memory. An interrrupt is asserted by the 82595FX (EOF) after frame reception has been completed.

If the 82595FX is configured to Discard Bad Frames, it will discard all incoming errored frames by resetting its DMA Current Address Register back to the value of the Base Address Register and not updating any of the fields in the RCV frame structure. This area will now be reused to store the next incoming frame.

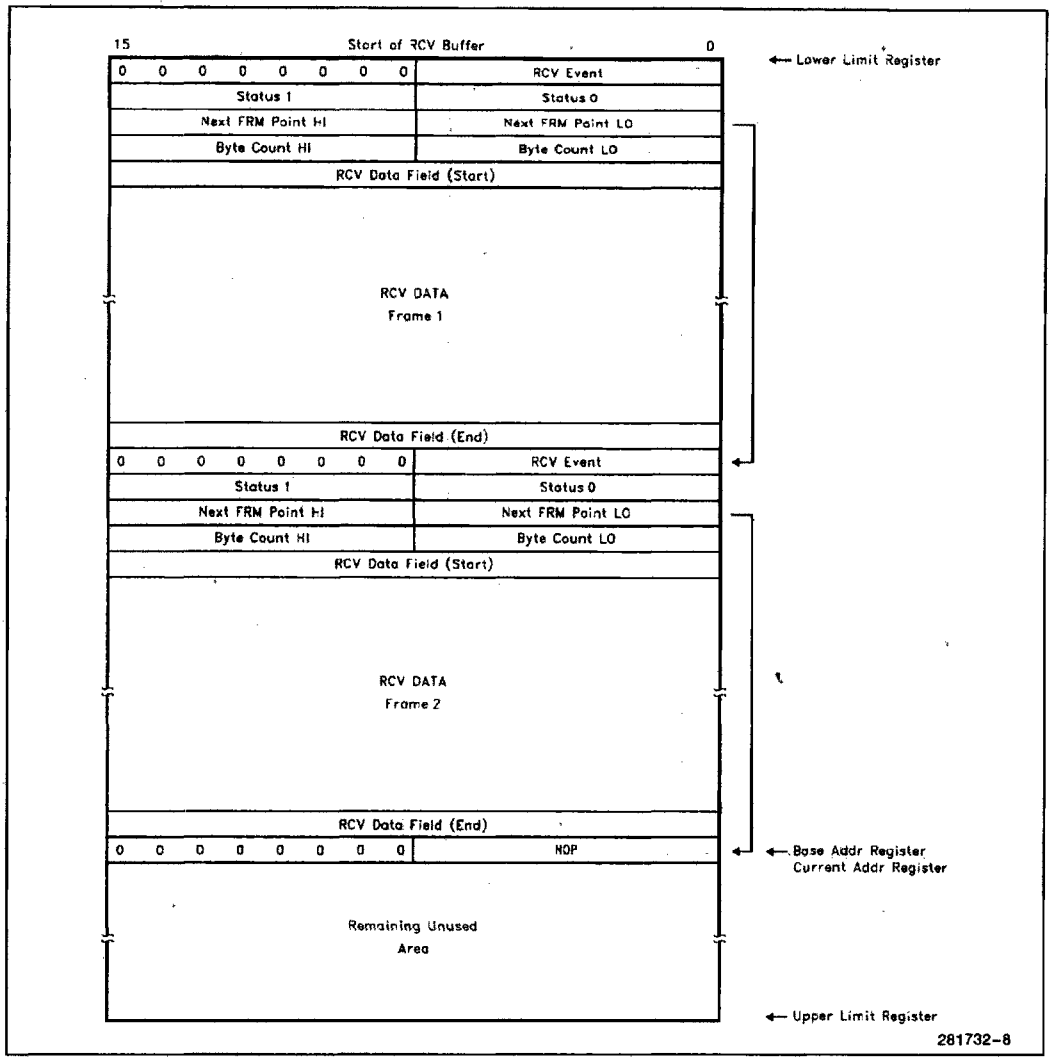


Figure 8-1. 82595FX RCV Memory Structure (16-Bit)

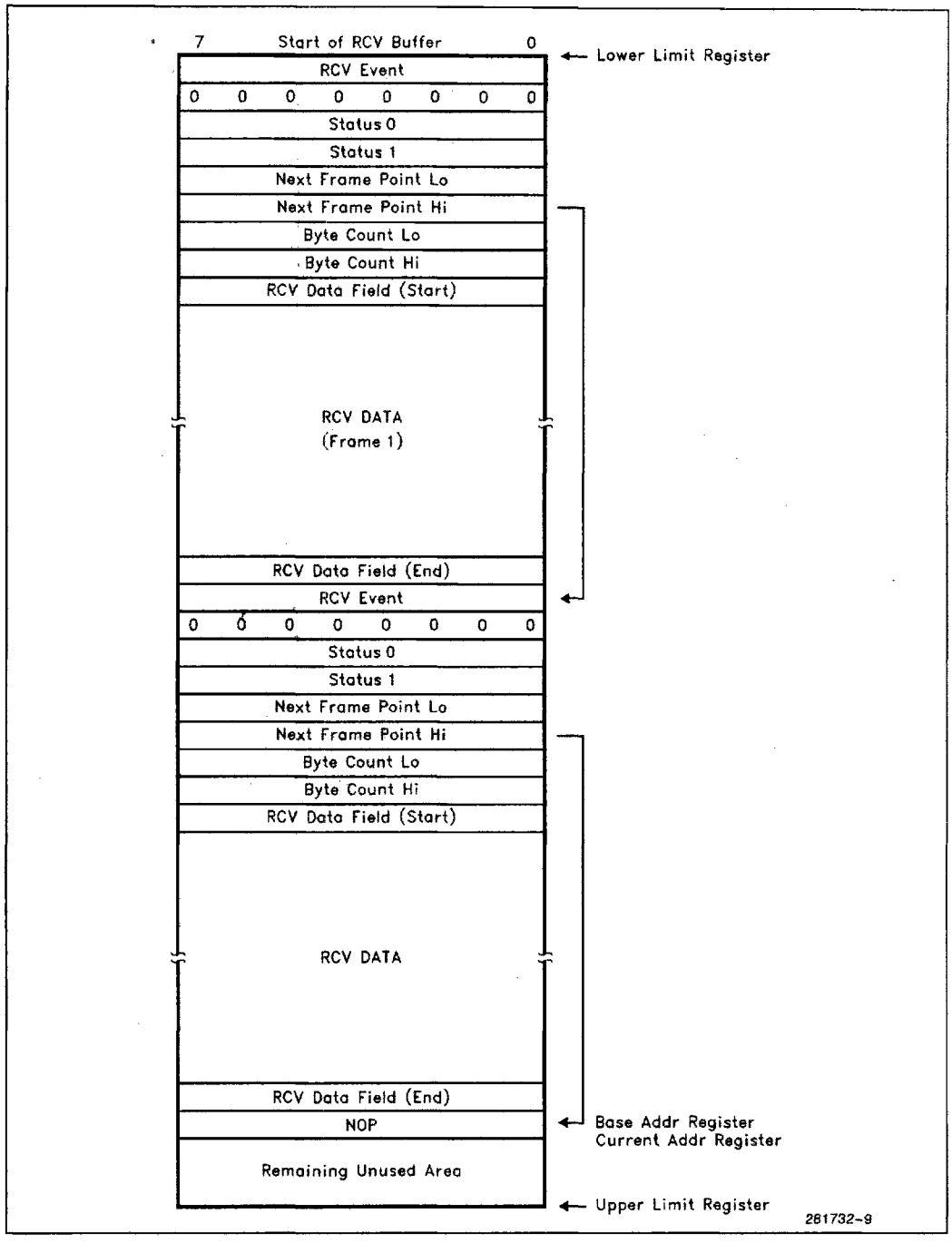


Figure 8-2. 82595FX RCV Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 8-3. In a 16-bit wide interface, these two bytes will combine to form one word. The 82595FX provides this field for each incoming frame.

8.2 RCV Ring Buffer Operation

The 82595FX RCV Ring Buffer operation is illustrated in Figure 8-4. The 82595FX copies received frames sequentially into the RCV Buffer area of the local memory. The CPU processes these frames by copying the frames from the local memory. After a frame is processed, the CPU updates the 82595FX's Stop Register to point to the last location processed. This indicates that the RCV Buffer memory which precedes the value programmed in the Stop Register is now free area (it has been processed by the CPU). When the 82595FX reaches the end of the RCV Buffer (the Upper Limit Register value) it will now wrap around back to the beginning of the buffer, and continue to copy RCV frames into the buffer, beginning at the value pointed to by the Lower Limit Register. The 82595FX will continue to copy frames into the RCV Buffer area as long as it does not reach the address pointed to by the Stop Register (if this does occur, the 82595FX stops copying the frames into memory and issues an Interrupt to the CPU). As the CPU processes additional incoming frames, the Stop Register value continues to be moved. This action allows the CPU to keep ahead of the incoming frames and allows the Ring Buffer to be continually recycled as the memory space consumed by an incoming frame is reused as that frame is processed.

7	6	5	4	3	2	1	0	
SRT FRM	X	X	1	X	X	IA MCH	RCLD	Status 0
TYP/$\overline{\text{LEN}}$	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RN	Status 1

Figure 8-3. RCV Status Field

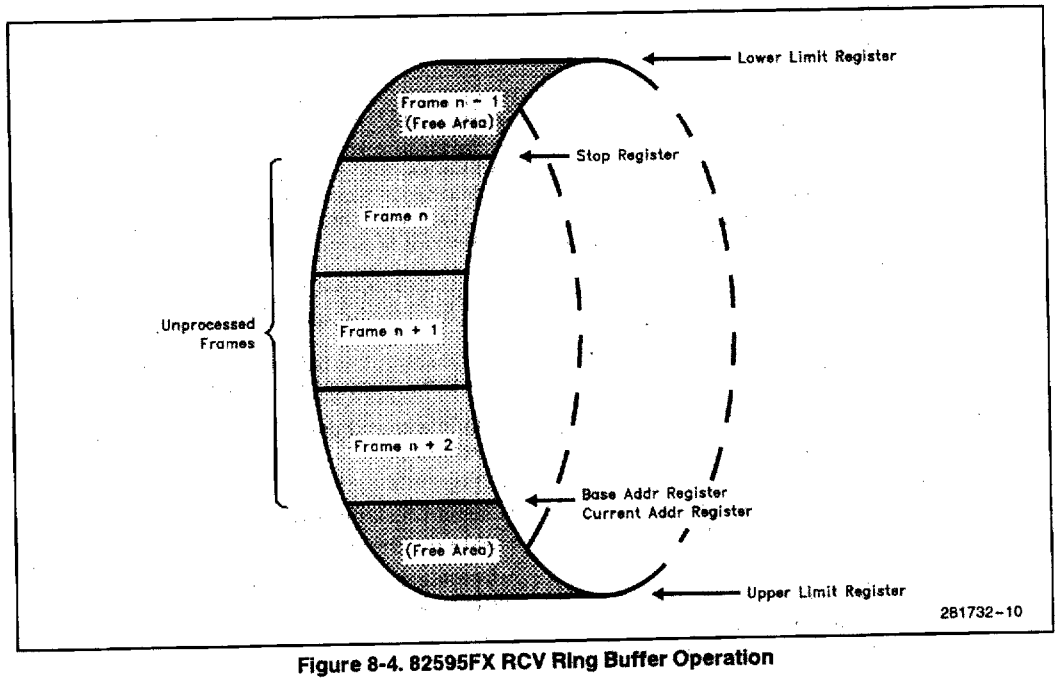


Figure 8-4. 82595FX RCV Ring Buffer Operation

9.0 SERIAL INTERFACE

The 82595FX's serial interface subsystem incorporates all the active circuitry required to interface the 82595FX to 10BASE-T networks or to the attachment unit (AUI) interface. It includes on-chip AUI and TPE drivers and receivers as well as Manchester Encoder/Decoder and Clock Recovery circuitry. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also be interfaced to a transceiver to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595FX automatically enables either the AUI or TPE interface, depending on which medium is active. This automatic selection can be overridden by software configuration. The TPE interface also features a polarity fault detection and correction circuit which will detect and correct a polarity error on the twisted pair wire, the most common wiring fault in twisted pair networks.

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

The 82595FX supports 802.3 Half Duplex Ethernet functionality, as did previous versions of the 82595. It also supports a Full Duplex Ethernet mode that complies with *Specifications for Full Duplex Ethernet*, Rev. 1.0, Sept. 9th, 1993, from Kalpana, when connected to a Full Duplex hub through the TPE port. Full-duplex provides increased network throughput (using full duplex network components) by providing dedicated channels for both Transmit and Receive data at the same time. Full Duplex operation is transparent to existing software drivers. More details on Full Duplex functionality can be found in the 82595FX User's Guide.

Auto-Negotiation (or N-Way) is a method of maximizing network operational efficiency. Auto-Negotiation works by interrogating Auto-Negotiation compliant equipment to determine the highest common mode of operation shared by all connected devices. When Auto-Negotiation is enabled, the 82595FX will negotiate the Highest Common Denominator (HCD) transmission mode with the hub to which it is attached, on a hardware reset. If the hub does not support Auto-Negotiation and Auto-Negotiation is enabled on the 82595FX, the 82595FX will revert to Half Duplex.

The 82595FX is in Auto-Negotiation mode only when the A-N Enable bit, bit 1 in register 13 of bank 2, is set. On hardware reset, the state of this bit is copied from the EEPROM A-N Enable bit, bit 9 of Word 0 of the EEPROM.

We recommend that a crystal that meets the following specifications be used:

- Quartz Crystal
- 20.00 MHz ±0.002% at 25°C
- Accuracy ±0.005% over Full Operating Temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode

Several vendors have such crystals; either off-the-shelf or custom-made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078
   Specifications:
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907
   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics; therefore, it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

A summary of the 82595FX's serial interface subsections functions is shown below:

- **Manchester Encoder/Decoder and Clock Recovery**
- **Diagnostic Loopback**
- **Reset-Low-Power Mode**
- **Network Status Indicators**
- **Defeatable Jabber Timer**
- **User Test Modes**

- **Complies with IEEE 802.3 AUI Standard**
  - **— Direct Interface to AUI Transformers**
  - **— On-Chip AUI Squelch**
- **Complies with IEEE 802.3 10BASE-T for Twisted Pair Ethernet**
  - **— Selectable Polarity Detection and Correction**
  - **— Direct Interface to TPE Analog Filters**
  - **— On-Chip TPE Squelch**
  - **— Defeatable Link Integrity for Pre-Standard Networks**
  - **— Supports 4 LEDs (Link Integrity, Activity, AUI/BNC DIS and Polarity Correction)**
  - **— Auto-Negotiation of Full Duplex Functionality**

10.0 APPLICATION NOTES

This section is intended to provide Ethernet LAN designers with a basic understanding of how the 82595FX is used in a buffered LAN design.

10.1 Bus Interface

The 82595FX Bus Interface unit integrates ISA Bus data transceivers, providing an even more cost efficient and seamless integration than that of the 82595TX. The 82595FX provides the complete control and address interface to the host system bus—implementing a complete ISA bus protocol.

10.2 Local Memory Interface

The 82595FX's local memory interface includes a DMA unit which controls data transfers between the 82595FX and the local memory SRAM. The 82595FX can support up to 64 Kbytes of local SRAM.

The 82595FX provides address decoding and control to allow access to an external Boot EPROM or a FLASH. Addition of a Boot EPROM or FLASH to an ISA solution is optional. The IA is assumed to be stored in the serial EEPROM for the ISA solution.

10.3 EEPROM Interface

The 82595FX provides a complete interface to a serial EEPROM for ISA adapter designs. For ISA motherboard designs, the EEPROM is not required. The EEPROM is used to store configuration information such as Memory and IO Mapping Window, Interrupt line selection, Plug N' Play resource data local bus width, etc. The EEPROM is used to replace jumper blocks which previously contained this type of information.

10.4 Serial Interface

The 82595FX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 10BASE5 interface. The AUI port can also be interfaced to a transceiver device on the adapter to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595FX automatically enables either the AUI or TPE interface, depending on which medium is connected to the chip. This automatic selection can be overridden by software configuration.

10.4.1 AUI CIRCUIT

When used in conjunction with pulse transformers, the 82595FX provides a complete IEEE 802.3 AUI interface. In order to meet the 16V fault tolerance specification of IEEE 802.3, a pulse transformer is recommended. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 82595FX and the DO, DI, and CI pairs of the AUI (DB-15) connector. The pulse transformer should have the following characteristics:

- 75 μH minimum inductance (100 μH recommended)
- 2000V isolation between the primary and secondary windings
- 2000V isolation between the primaries of separate transformers
- 1:1 Turns ratio

The RCV and CLSN input pairs should each be terminated by 78.7Ω $\pm$1% resistors.

10.4.2 TPE CIRCUIT

The 82595FX provides the line drivers and receivers needed to directly Fabinterface to the TPE analog filter network. The TPE receive section requires a 100Ω termination resistor, a filter section (filter, isolation transformer, and a common mode choke) as described by the 10BASE-T 802.3i-1990 specification.

The TPE transmit section is implemented by connecting the 82595FX's four TPE outputs (TDH, $\overline{TDH}$, TDL, $\overline{TDL}$) to a resistor summing network to form the differential output signal. The parallel resistance of R5 and R6 sets the transmitters maximum output voltage, while the difference (R5 − R6)/R5 + R6), is used to reduce the amplitude of the second half of the fat bit (100 ns) to a predetermined level. This predistortion reduces line overcharging, a major source of jitter in the TPE environment. The output of the summing network is then fed into the above mentioned filter and then to the 10BASE-T connector (RJ-45). Analog Front End solutions can be purchased in a single-chip solution from several manufacturers. The solution described in this data sheet uses the Pulse Engineering (PE65434) AFE.

10.4.3 LED CIRCUIT

The 82595FX's internal LED drivers support four LED indicators displaying node status and activity (i.e., Transmit data, receive data, collisions, link integrity, polarity correction, and port (TPE/AUI). To implement the LED indicators, connect the LED driver output to an LED in series with a 510Ω resistor tied to V_{CC}. Each driver can sink up to 10 mA of current with an output impedance of less than 50Ω.

10.5 Layout Guidelines

10.5.1 GENERAL

The analog section, as well as the entire board itself, should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, follow these guidelines:

Make power supply and ground traces as thick and as short as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together, only at one point on the fab—near the connection to system ground.

You must connect all V_{CC} pins to the same power supply and all V_{SS} pins to the same ground plane. Use separate decoupling per power-supply/ground pin.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

10.5.2 CRYSTAL

The crystal should be adjacent to the 82595FX and trace lengths should be as short as possible. the X1 and X2 traces should be as symmetrical as possible.

10.5.3 82595FX ANALOG DIFFERENTIAL SIGNALS

The differential signals from the 82595FX to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network should have the ground and power planes removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

10.5.4 DECOUPLING CONSIDERATIONS

Four 0.1 μF ceramic capacitors should be used. Place one on each side in the center of the I.C. adjacent to the 82595FX. Connect the capacitors directly to the V_{CC} pins and ground planes of the 82595FX.

11.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

11.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C

Storage Temperature .....−65°C to +140°C

All Output and Supply Voltages .....−0.5V to +7V

All Input Voltages .....−1.0V to +6.0V(1)

Further information on the quality and reliability of the 82595FX may be found in the *Components Quality and Reliability Handbook*, Order Number 210997.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 11-1. DC Characteristics (T_C = 0°C to +85°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input HIGH Voltage (TTL)	2.0	V_{CC} + 0.3	V	
$V_{IH(JUMPR)}$	Input HIGH Voltage (Jumpers)	3.0	V_{CC} + 0.3	V	
V_{OL1}(2)	Output LOW Voltage		0.45	V	I_{OL} = 17 mA
V_{OL2}(3)	Output LOW Voltage		0.45	V	I_{OL} = 12 mA
V_{OL4}(4)	Output LOW Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1 mA
V_{OL} (LED)(5)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH} (LED)	Output High Voltage	3.9		V	I_{OH} = −500 µA
I_{LP}(6)	Leakage Current		±10	µA	$0 \le V_I \le V_{CC}$
R_{DIFF}(7)	Input Differential-Resistance	10		KΩ	DC
V_{IDF} (TPE)(8)	Input Differential Accept Input Differential Reject	±0.5	±3.1 ±0.3	V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S (TPE)(9)	Output Source Resistance	5	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF} (AUI)(10)	Input Differential Accept Input Differential Reject	±0.3	±1.5 ±0.16	V_P V_P	
V_{ICM} (AUI)(11)	AC Input Common Mode		±0.5 ±0.1	V_P V_P	f ≤ 40 KHz 40 KHz ≤ f ≤ 10 MHz
V_{ODF} (AUI)	Output Differential Voltage	±0.45	±1.2	V	
I_{OSC} (AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
VU (AUI)	Output Differential Undershoot		−100	mV	
V_{ODI} (AUI)(12)	Differential Idle Voltage		40	mV	
I_{CC}	Power Supply Current		90	mA	
I_{CCHWPD} I_{CCSWPD} $I_{CCSLEEP}$	Hardware Power Down Software Power Down Sleep Mode		400 2 35	µA mA mA	
C_{IN}(13)	Input Capacitance		10	pF	@ f = 1 MHz

NOTES:
1. The voltage level for RCV and CLSN pairs are −0.75V to +8.5V.
2. SDx, $\overline{IOCS16}$.
3. IOCHRDY, IRQx.
4. LDATAx, LADDRx, $\overline{LOE}$, $\overline{LWE}$, $\overline{BOOTCS}$, $\overline{SRAMCS}$, EEPROMCS, $\overline{SMOUT}$, TSTCLK, TDO, J1, J2.
5. LILED, ACTLED, POLED and TPE_BNC_$\overline{AUI}$.
6. Pins: ACTLED, LILED, POLED, TPE_BNC_$\overline{AUI}$.
7. RD to $\overline{RD}$, RCV to $\overline{RCV}$ and CLSN to $\overline{CLSN}$.
8. TPE input pins: RD and $\overline{RD}$.
9. TPE output pins: TDH, $\overline{TDH}$, TDL and $\overline{TDL}$, R_S measure V_{CC} or V_{SS} to pin.
10. AUI input pins: RCV and CLSN pairs.
11. AUI output pins: TPMT pair.
12. Measured 8.0 µs after last positive transition of data packet.
13. Characterized, not tested.

11.1.1 PACKAGE THERMAL SPECIFICATIONS

The 82595FX is specified for operation when case temperature is within the range of 0°C to 85°C. The case temperature may be measured in any environment to determine whether the 82595FX is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{JA} and the θ_{JC} from the following equations:

$$T_J = T_C + P^*\theta_{JC}$$
$$T_A = T_J - P^*\theta_{JA}$$
$$T_C = T_A + P^*(\theta_{JA} - \theta_{JC})$$

θ_{JA} and θ_{JC} values for the 160 QFP package are as follows:

Thermal Resistance (°C/Watt)

θ_{JC}	θ_{JA} – VS – Airflow ft/min (m/Sec)
	0 (0)
4.9	34.4

11.2 AC Timing Characteristics

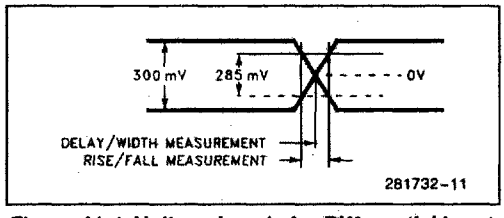


Figure 11-1. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs)

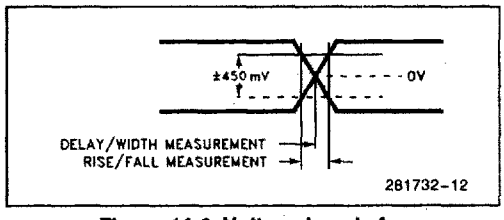


Figure 11-2. Voltage Levels for TDH, TDL, $\overline{TDH}$ and $\overline{TDL}$

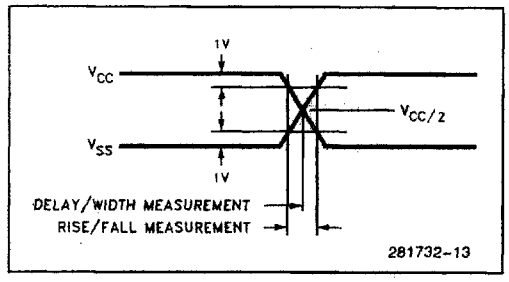


Figure 11-3. Voltage Levels for TRMT Pair Output Timing Measurements

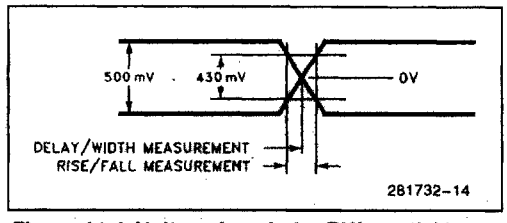


Figure 11-4. Voltage Levels for Differential Input Timing Measurements (RD Pair)

11.3 AC Measurement Conditions

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%
2. The signal levels are referred to in Figures 1, 2, 3 and 4.
3. AC Loads:
   a) AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 µH ±5% inductor between terminals.
   b) TPE: 20 pF total capacitance to ground.

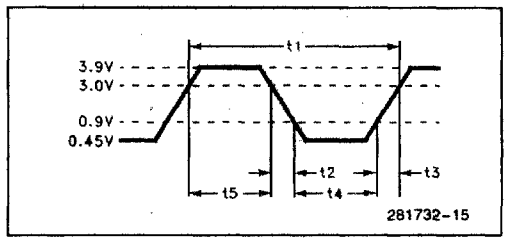


Figure 11-5. X1 Input Voltage Levels for Timing Measurements

Table 11-2. Clock Timing

Symbol	Parameter	Min	Max	Unit
t1	X1 Cycle Time	49.995	50.005	ns
t2	X1 Fall Time		5	ns
t3	X1 Rise Time		5	ns
t4	X1 Low Time	15		ns
t5	X1 High Time	15		ns

11.4 ISA Interface Timing

Table 11-3. 16-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1a	AEN Valid to I/O Command Active	100		ns	
T2a	AEN Valid from I/O Command Inactive	30		ns	
T3a	SA to CMD Active	63		ns	
T4a	SA Valid Hold from CMD Inactive	42		ns	
T5a	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T6a	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T7a	CMD Active to Inactive	125		ns	
T8a	CMD Inactive to Active	92		ns	*Before* I/O Command
T9a	Active CMD to Valid IOCHRDY		30	ns	Applies to Ready Cycles
T10a	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T11a	DATA Driven from READ CMD Active	0		ns	
T12a	Valid READ Data from CMD Active		64	ns	Applies to Standard Cycles Only
T13a	Valid READ Data from IOCHRDY Active		52	ns	Applies to Ready Cycles Only
T14a	READ Data Hold from CMD Inactive	0		ns	
T15a	READ CMD Inactive to Data Tristate		30	ns	
T16a	CMD to WRITE Data Active		62	ns	
T17a	WRITE Data Hold from CMD Inactive	15		ns	
T18a	WRITE CMD Inactive to Data Tristate		30	ns	

Table 11-4. 8-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1b	AEN Valid to I/O Command Active	100		ns	
T2b	AEN Valid from I/O Command Inactive	30		ns	
T3b	SA to CMD Active	63		ns	
T4b	SA Valid Hold from CMD Inactive	42		ns	
T5b	Valid SA to $\overline{\text{IOCS16}}$ Inactive		100	ns	
T6b	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T7b	CMD Active to Inactive	125		ns	
T8b	CMD Inactive to Active	92		ns	*Before* I/O Command
T9b	Active CMD to Valid IOCHRDY		226	ns	Applies to Ready Cycles
T10b	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T11b	DATA Driven from READ CMD Active	0		ns	
T12b	Valid READ Data from CMD Active		64	ns	Applies to Standard Cycles
T13b	Valid READ Data from IOCHRDY Active		52	ns	Applies to Ready Cycles Only
T14b	READ Data Hold from CMD Inactive	0		ns	
T15b	READ CMD Inactive to Data Tristate		30	ns	
T16b	CMD to WRITE Data Active		62	ns	
T17b	WRITE Data Hold from CMD Inactive	15		ns	
T18b	WRITE CMD Inactive to Data Tristate			ns	

Table 11-5. 8-Bit Memory Access

Parameter	Description	Min	Max	Units	Comments
T1c	AEN Valid to Command Active	100		ns	
T2c	AEN Valid from Command Inactive	30		ns	
T3c	SA to CMD Active	63		ns	
T4c	SA Valid Hold from CMD Inactive	42		ns	
T5c	CMD Active to Inactive	125		ns	
T6c	CMD Inactive to Active	60		ns	*Before* Memory Command
T7c	Active CMD to Valid IOCHRDY		226	ns	Applies to Ready Cycles
T8c	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T9c	DATA Driven from READ CMD Active	0		ns	
T10c	Valid READ Data from IOCHRDY Active		52	ns	
T11c	READ Data Hold from CMD Inactive	0		ns	
T12c	READ CMD Inactive to Data Tristate		30	ns	
T13c	CMD to WRITE Data Active		62	ns	
T14c	WRITE CMD Inactive to Data Tristate		30	ns	

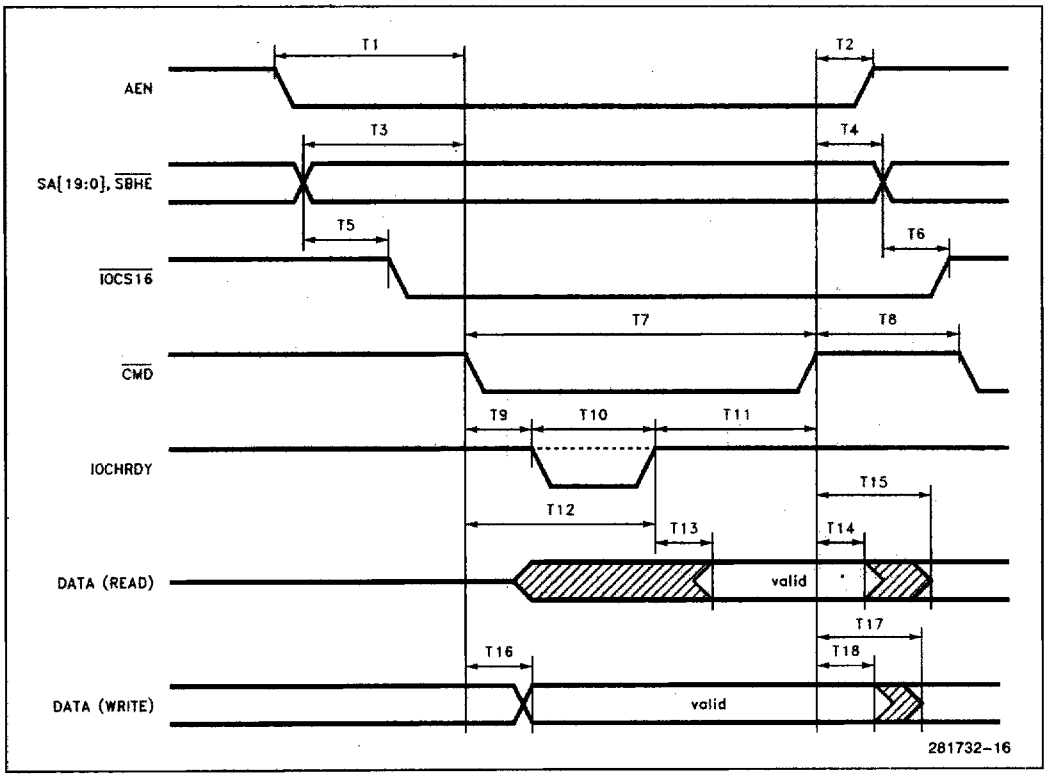


Figure 11-6. ISA Read/Write Cycle

11.6 Local Memory Timings

11.6.1 SRAM TIMINGS

- The 82595FX any SRAM up to 25 ns access time.
- SRAM type supported are 4K, 8K, 16K, 32K, 64K x 8.

Table 11-6. 82595FX SRAM—AC Characteristics

Parameter	Description	Min	Max	Units	Comments
T1w	LADDR Valid to $\overline{\text{SRAMCS}}$ Active	0		ns	
T2w	LADDR Valid to $\overline{\text{LWE}}$ Active	0		ns	
T3w	$\overline{\text{SRAMCS}}$ Active Time	25		ns	
T4w	$\overline{\text{LWE}}$ Active Time	25		ns	
T5w	Data Valid to $\overline{\text{SRAMCS}}$ Inactive	15		ns	
T6w	Data Valid to $\overline{\text{LWE}}$ Inactive	15		ns	
T7w	$\overline{\text{SRAMCS}}$ Inactive to Data Invalid	0		ns	
T8w	$\overline{\text{LWE}}$ Inactive to Data Invalid	0		ns	
T9w	$\overline{\text{SRAMCS}}$ Inactive to LADDR Invalid	0		ns	
T10w	$\overline{\text{LWE}}$ Inactive to $\overline{\text{LADDR}}$ Invalid	0		ns	
T1r	LADDR Valid to $\overline{\text{SRAMCS}}$ Active	0		ns	
T2r	LADDR Valid to $\overline{\text{LOE}}$ Active	0		ns	
T3r	$\overline{\text{SRAMCS}}$ Active Time	25		ns	
T4r	$\overline{\text{LOE}}$ Active Time	25		ns	
T5r	Data Valid to $\overline{\text{SRAMCS}}$ Active		25	ns	
T6r	Data Valid to $\overline{\text{LOE}}$ Inactive		25	ns	
T7r	Data Read Hold Time from $\overline{\text{SRAMCS}}$ Inactive	0	25	ns	
T8r	Read Data Hold Time from $\overline{\text{LOE}}$ Inactive	0	25	ns	

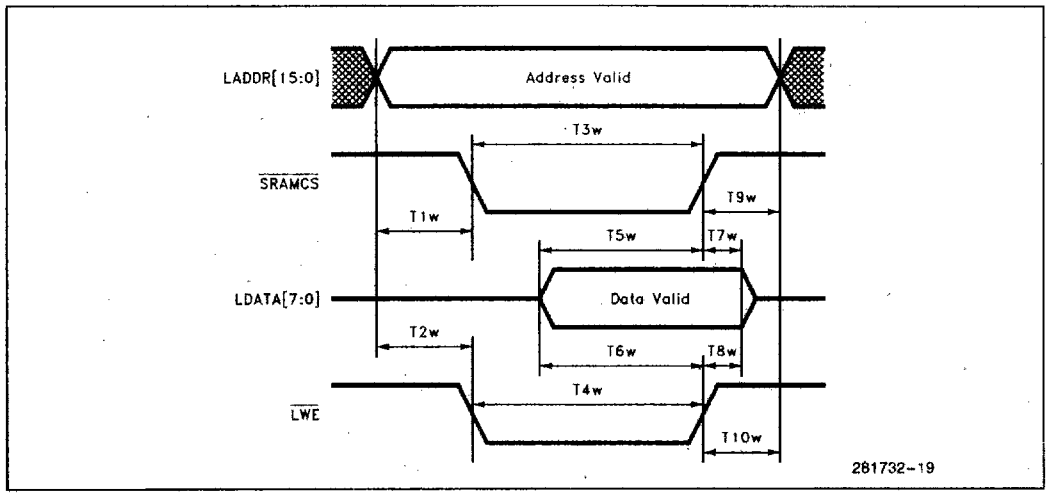


Figure 11-7. SRAM Timings—Write Cycle

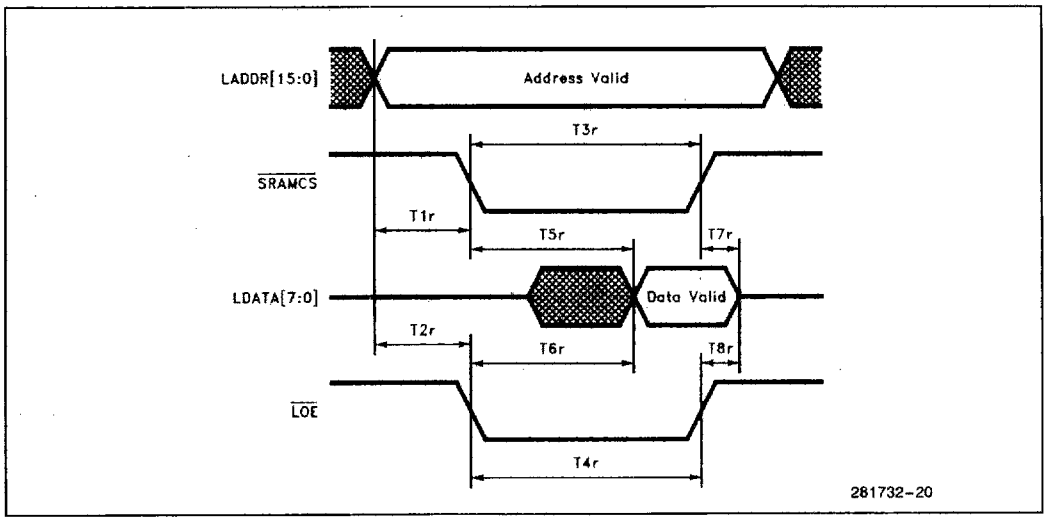


Figure 11-8. SRAM Timings—Read Cycle

11.6.2 FLASH/EPROM TIMINGS

- The 82595FX is designed to support a FLASH or EPROM up to 200 ns access time.
- Flash/EPROM types supported are 16K, 32K, 64K, 128K, 256K, 512K, 1024K x 8.

Table 11-7. FLASH—AC Characteristics

Parameter	Description	Min	Max	Units	Comments
T1w	LADDR Setup Time to $\overline{LWE}$ Active	0		ns	
T2w	LADDR Hold Time from $\overline{LWE}$ Active	75		ns	
T3w	$\overline{LWE}$ Active Time	60		ns	
T4w	$\overline{BOOTCS}$ Setup Time before $\overline{LWE}$ Active	20		ns	
T5w	$\overline{BOOTCS}$ Hold Time from $\overline{LWE}$ Inactive	0		ns	
T6w	Data Setup Time before $\overline{LWE}$ Inactive	50		ns	
T7w	Data Hold Time from $\overline{LWE}$ Inactive	10		ns	
T1r	LADDR Setup Time to $\overline{BOOTCS}$ Active	0		ns	
T2r	LADDR Setup Time to $\overline{LOE}$	0		ns	
T3r	$\overline{BOOTCS}$ Active Time	225		ns	
T4r	$\overline{LOE}$ Active Time	225		ns	
T5r	$\overline{BOOTCS}$ Active to Data Valid		200	ns	
T6r	$\overline{LOE}$ Active to Data Valid		200	ns	
T7r	Data Hold Time from $\overline{BOOTCS}$ Inactive	0	40	ns	
T8r	Data Hold Time from $\overline{LOE}$ Inactive	0	40	ns	

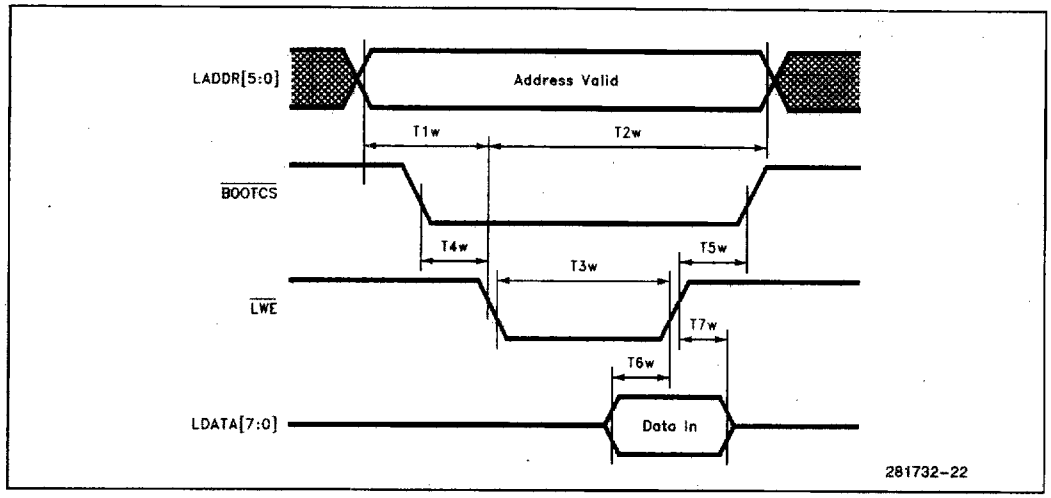


Figure 11-10. FLASH Timings—Write Cycle

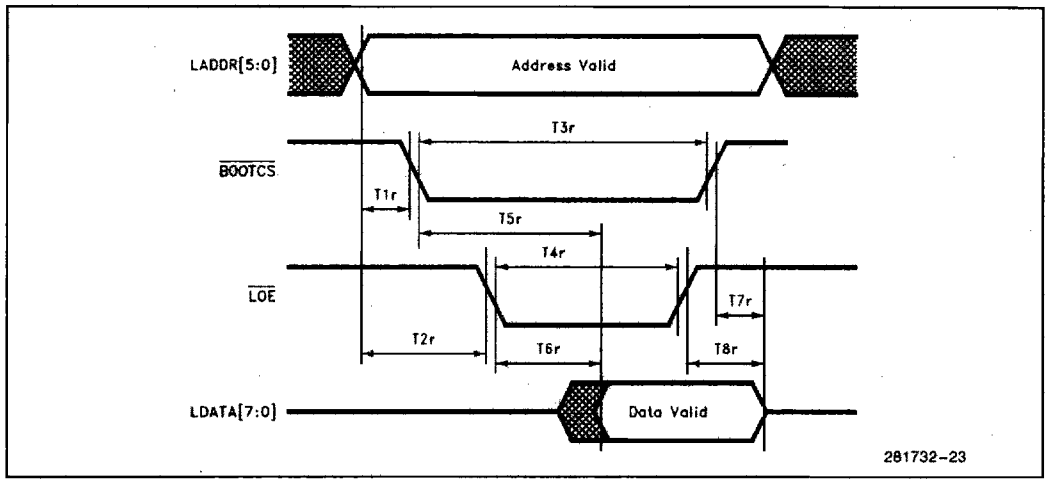


Figure 11-11. Flash Timings—Read Cycle

Table 11-8. EEPROM AC Characteristics

Parameter	Description	Min	Max	Units	Comments
T1(css)	CS Setup Time	1.0		μs	
T2(skh)	SK High Time	3.0		μs	
T3(skl)	SK Low Time	3.0		μs	
T4(csh)	CS Hold Time	0		μs	
T5(cs)	CS Low Time	1.0		μs	
T6(dis)	DI Setup Time	0.4		μs	
T7(dih)	DI Hold Time	0.4		μs	
T8(do)	DO Valid Time		0.4	μs	EEPROM Restriction
T9(df)	CS Inactive to DO Floating		0.4	μs	EEPROM Restriction

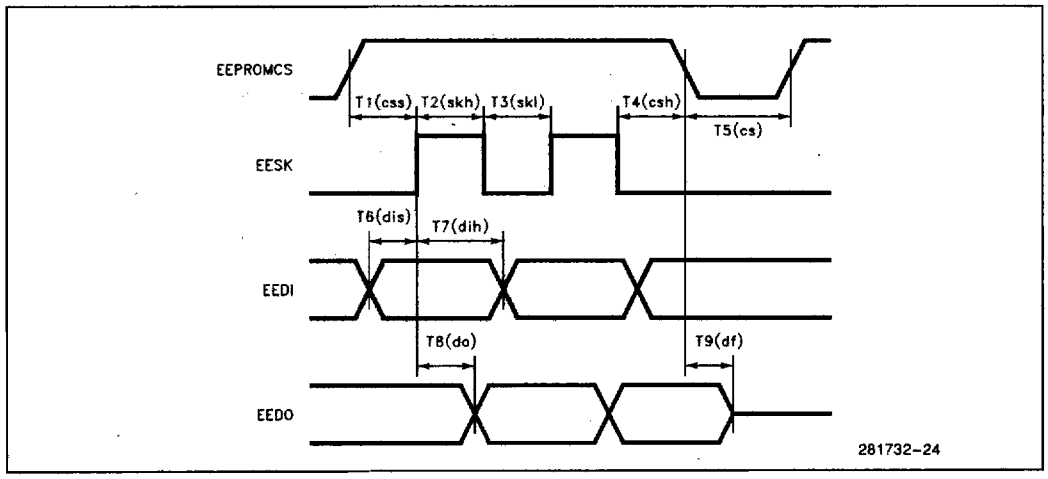


Figure 11-12. EEPROM Timings

11.7 Interrupt Timing

Table 11-9. Interrupt Timing

Parameter	Description	Min	Max	Units	Notes
T177	Interrupt Ack $\overline{CMD}$ Inactive to IRQ[0–7] Inactive		500	ns	
T178	IRQ[0–7] Inactive to IRQ[0–7] Active	100		ns	
T179	Tri-state $\overline{CMD}$ Inactive to IRQ[0–7] Tri-State		500	ns	

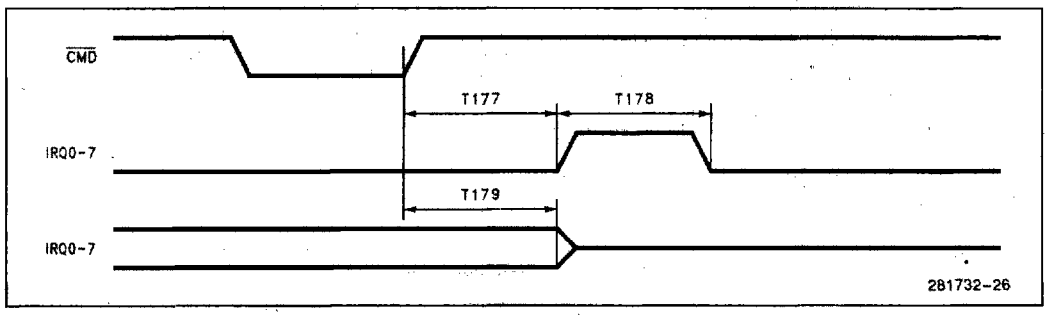


Figure 11-13. Interrupt Timing

11.8 RESET and $\overline{\text{SMOUT}}$ Timing

General Comments

- Both signals are asynchronous signals and have minimum pulse duration specification only.
- $\overline{\text{SMOUT}}$ during Hardware power down activation.

Table 11-10. RESET and $\overline{\text{SMOUT}}$ Timing

Parameter	Description	Min	Max	Units	Notes
T180	RESET Minimum Duration	32		ms	1
T181	$\overline{\text{SMOUT}}$ Minimum Duration	100		ns	2
T182	$\overline{\text{SMOUT}}$ Activation by Power Down Command	150		ns	3
T183	$\overline{\text{SMOUT}}$ Deactivation	25		ns	3

NOTES:
1. Noise spikes of maximum TBD ns are allowed on Reset.
2. $\overline{\text{SMOUT}}$ is input.
3. $\overline{\text{SMOUT}}$ is output after configuration.

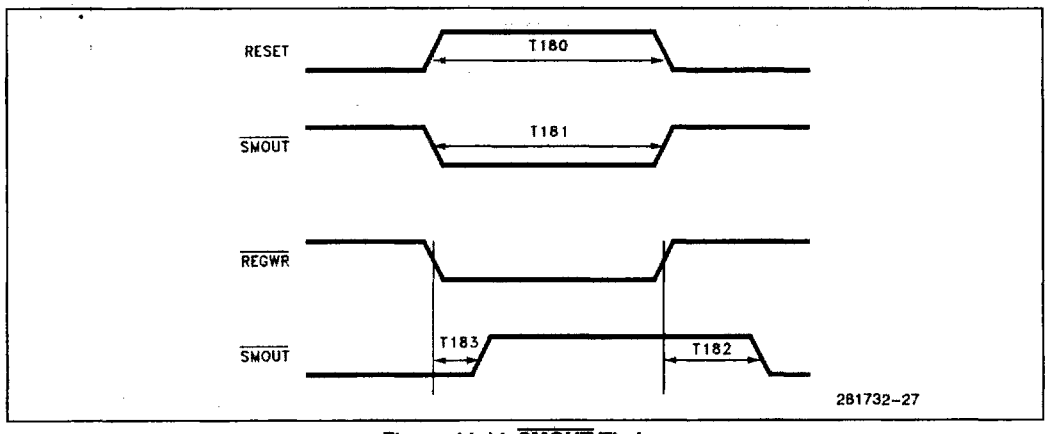


Figure 11-14. $\overline{\text{SMOUT}}$ Timing

11.9 JTAG Timing

Table 11-11. 82595FX JTAG Timing

Symbol	Parameter	Min	Max	Unit	Notes
T184	TMS Set-Up Time	30		ns	
T185	TMS Hold Time	30		ns	
T186	TDI Set-Up Time	30		ns	
T187	TDI Hold Time	30		ns	
T188	Input Signals Set-Up Time	30		ns	
T189	Input Signals Hold Time	30		ns	
T190	Outputs Valid Delay		200	ns	
T191	TDO Valid Delay		40	ns	
T192	TCK Cycle Time (Period)	100		ns	50% Duty Cycle

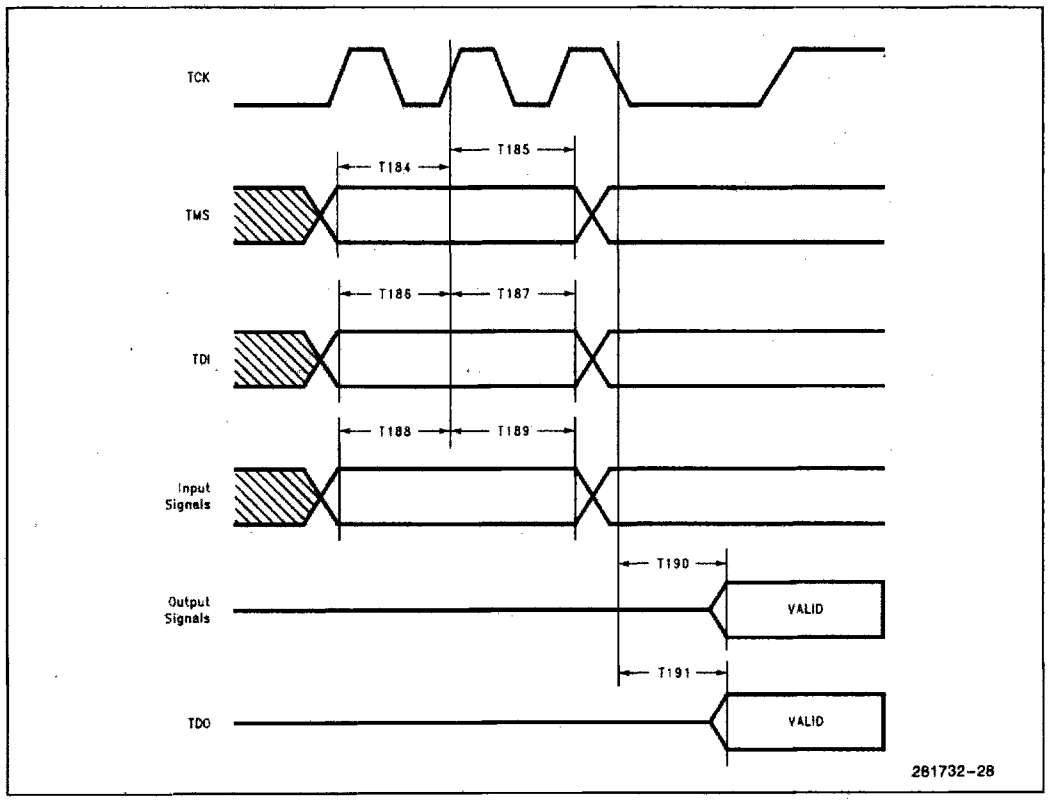
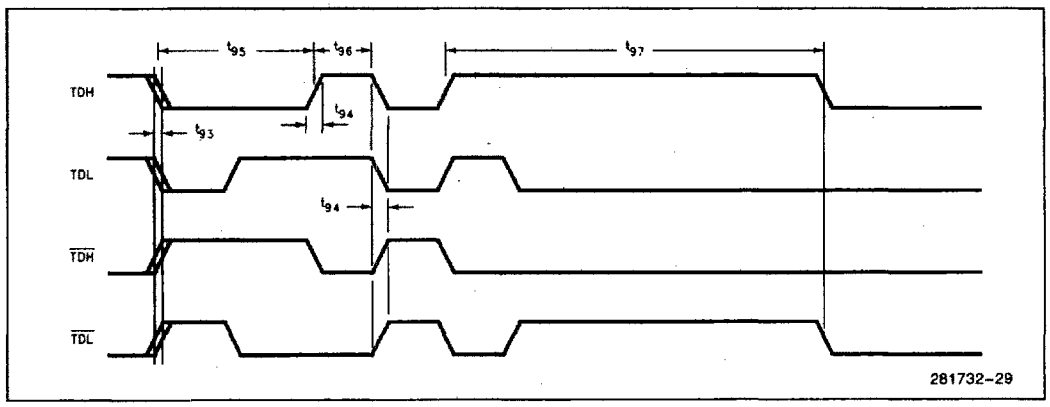


Figure 11-15. 82595FX JTAG Timing

11.10 Serial Timings

Table 11-12. TPE Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{90}	Number of TxD Bit Loss at Start of Packet			2	bits
t_{91}	Internal Steady State Propagation Delay			400	ns
t_{92}	Internal Start UP Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH	250		400	ns
t_{98}	Link Test Pulse Width	98	100	100	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns



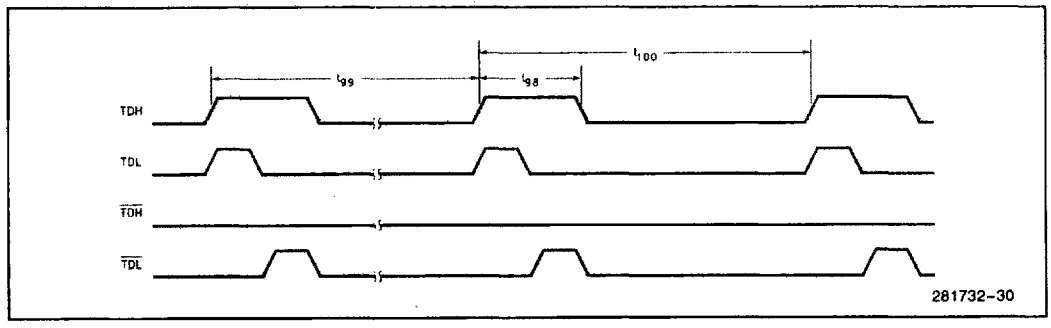


Figure 11-16. TPE Transmit Timings (Link Test Pulse)

Table 11-13. TPE Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to Internal Steady State Propagation Delay			400	ns
t_{108}	RD to Internal Start Up Delay			2.4	µs
t_{109}	RD Pair Bit Cell Center Jitter			± 13.5	ns
t_{110}	RD Pair Bit Cell Boundry Jitter			± 13.5	ns
t_{111}	RD Pair Held High from Last Valid Position Transition	230		400	ns

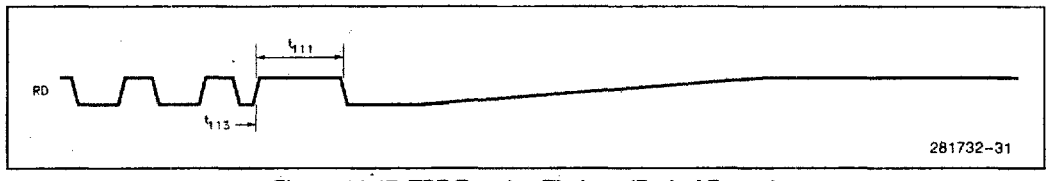


Figure 11-17. TPE Receive Timings (End of Frame)

Table 11-14. TPE Link Integrity Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(1)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(2)	25	50	150	ms

NOTES:
1. Linkbeats closer in time to this value are considered noise and rejected.
2. Linkbeats further apart in time than this value are not considered consecutive and are rejected.

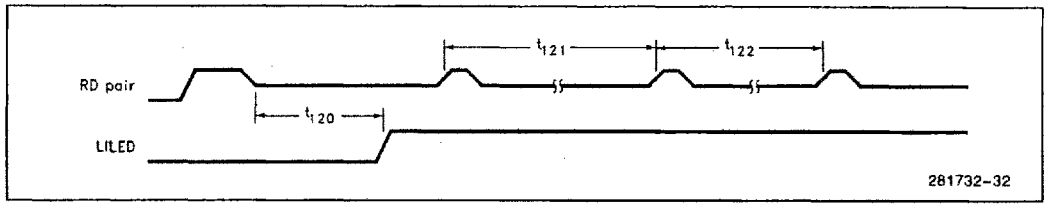


Figure 11-18. TPE Link Integrity Timings

Table 11-15. AUI Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	50	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRTM Pair Return to ≤ 40 mVp from Last Positive Transition			8.0	μs

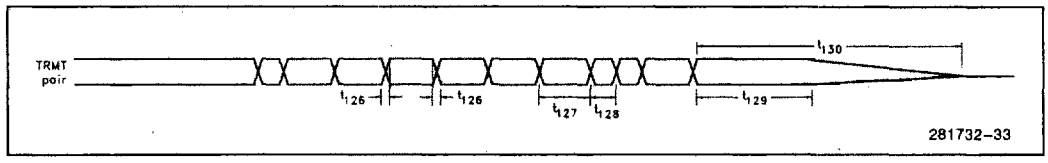


Figure 11-19. AUI Transmit Timings

Table 11-16. AUI Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			±12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			±18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns

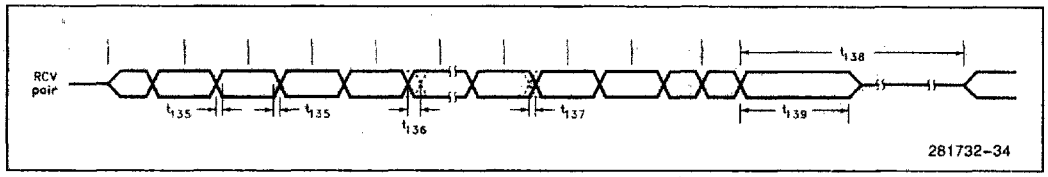


Figure 11-20. AUI Receive Timings

Table 11-17. AUI Collision Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns

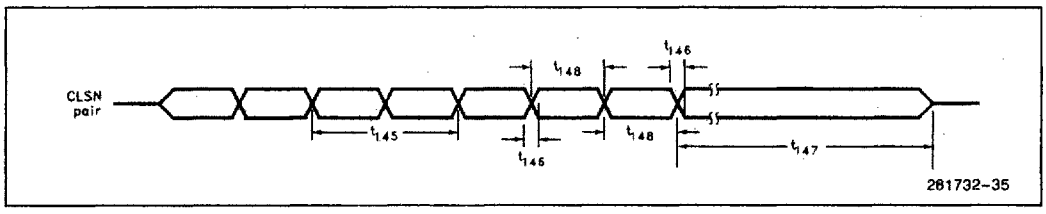


Figure 11-21. AUI Collision Timings

Table 11-18. AUI Noise Filter Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

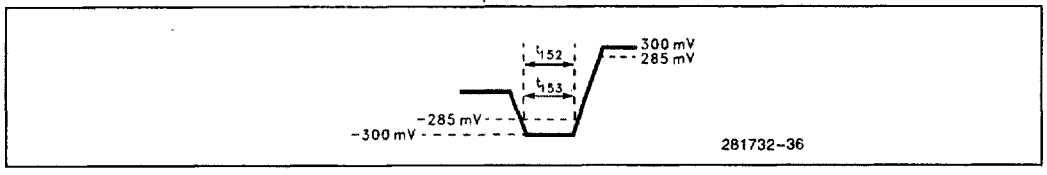


Figure 11-22. AUI Noise Filter Timings

Table 11-19. Jabber Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	275	750	ms

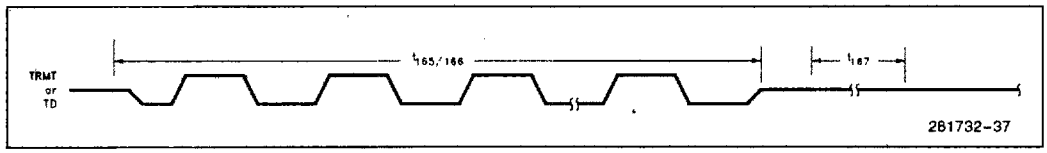


Figure 11-23. Jabber Timings

Table 11-20. LED Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{170}	ACTLED On Time	50		450	ms
t_{171}	ACTLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

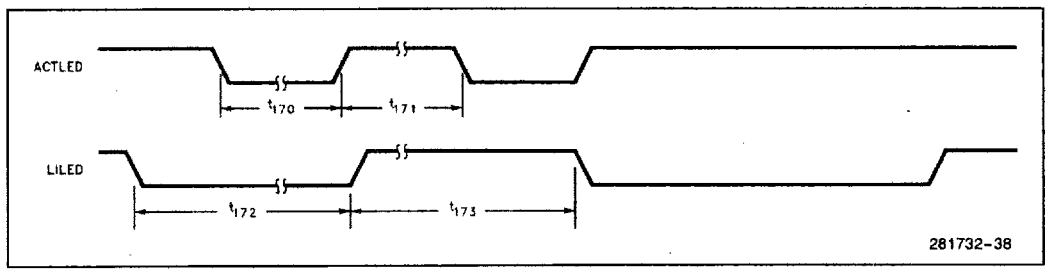


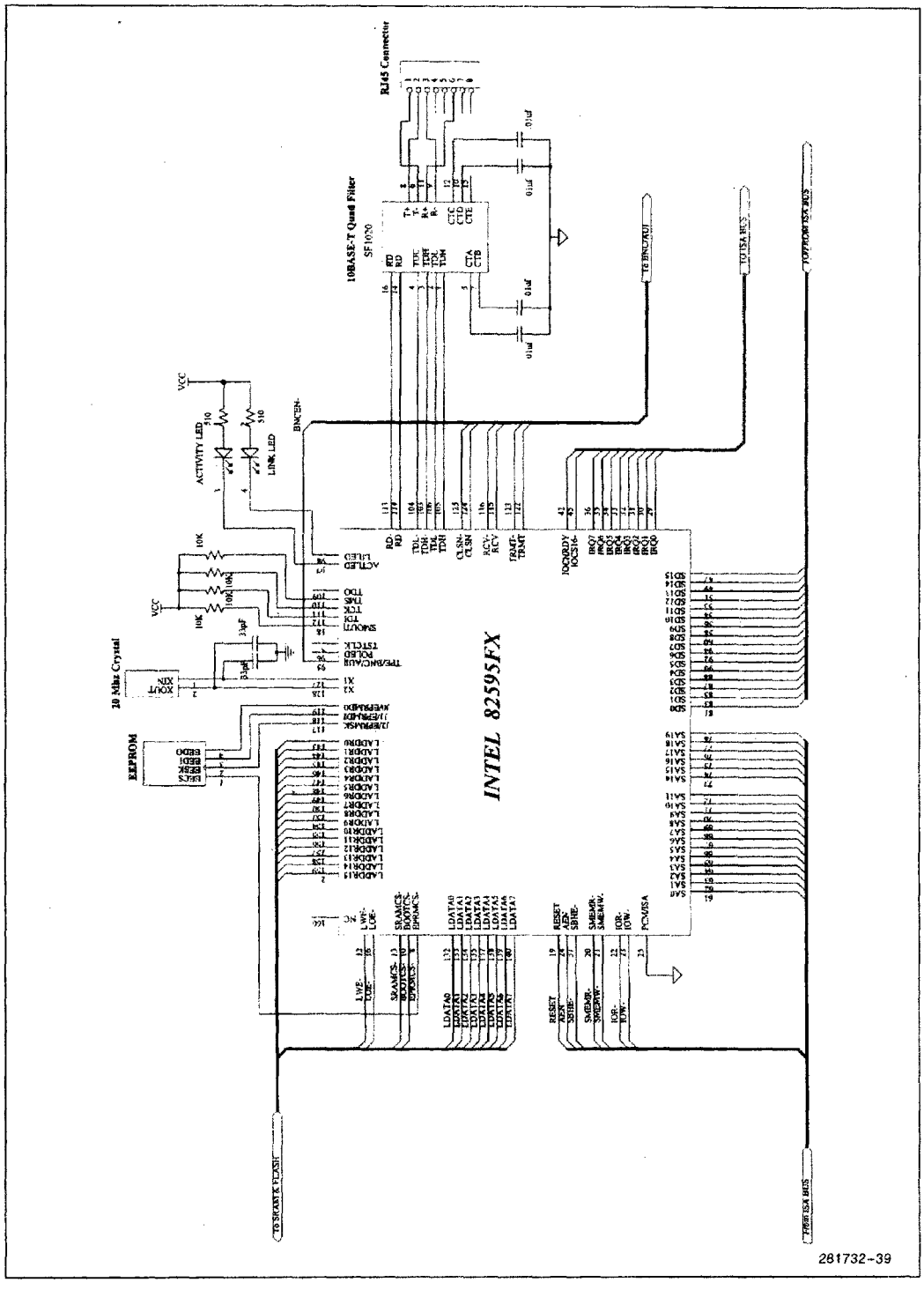
Figure 11-24. LED Timings

Additional 82595FX Documentation

This datasheet provides complete pinout and pin definitions, and electrical specifications and timings. It also includes an overview of the various subsections listed in Figure 1. For more complete information on the 82595FX, please ask your local sales representative for the 82595FX User's Guide. The 82595FX User's Guide contains detailed information on the 82595FX feature set, including register descriptions and implementation steps for various 82595FX functions (initialization, transmission, reception).

Design Example

The schematic on the next page shows a typical 82595FX design.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RJ45 Connector
10BASE-T Quad Filter
SF1070
ACTIVITY LED
LINK LED
EEPROM
20 Mhz Crystal
281732-39