

**TYPES SN54AS286, SN74AS286
9-BIT PARITY GENERATORS/CHECKER
WITH BUS DRIVER PARITY I/O PORT**

D2809, DECEMBER 1983

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port
- Glitch-Free Bus During Power Up/Down
- Package Options include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

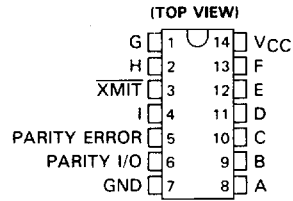
The SN54AS286 and SN74AS286 universal nine-bit parity generators/checkers feature a local output for parity checking and a 48-milliampere bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low the parity tree is disabled and PE will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

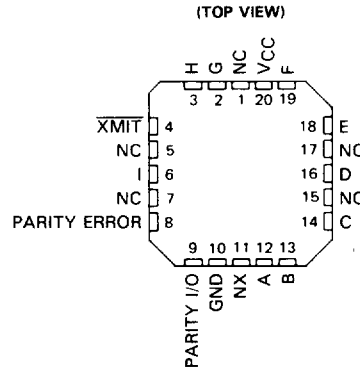
The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

The SN54AS286 is characterized for operation over the full military range of -55°C to 125°C . The SN74AS286 is characterized for operation from 0°C to 70°C .

SN54AS286 . . . J PACKAGE
SN74AS286 . . . N PACKAGE



SN54AS286 . . . FH PACKAGE
SN74AS286 . . . FN PACKAGE



NC - No internal connection

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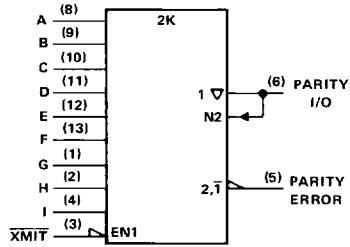
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FUNCTION TABLE

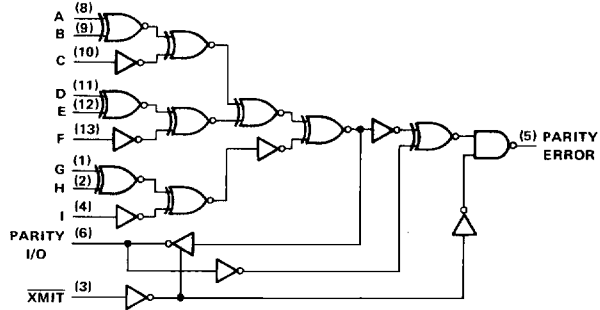
NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	I	H	H
1, 3, 5, 7, 9	I	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

logic symbol



logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS286	-55°C to 125°C
SN74AS286	0°C to 70°C
Storage temperature	-65°C to 140°C

recommended operating conditions

	SN54AS286			SN74AS286			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage	0.8			0.8			V
I_{OH} High-level output current	Parity error		-2	Parity error		-2	mA
	Parity I/O		-12	Parity I/O		-15	
I_{OL} Low-level output current	Parity error		20	Parity error		10	mA
	Parity I/O		32	Parity I/O		48	
T_A Operating free-air temperature	-55	125		0	70		°C

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electrical characteristics over recommended free-air temperature range
(unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS286			SN74AS286			UNIT	
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} - 2			V _{CC} - 2			V
	Parity I/O	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4	3.2		2.4	3.2		
		V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4						
		V _{CC} = 4.5 V, I _{OH} = -15 mA				2.4			
V _{OL}	Parity error	V _{CC} = 4.5 V, I _{OL} = 20 mA	0.35	0.5		0.35	0.5	V	
	Parity I/O	V _{CC} = 4.5 V, I _{OL} = 32 mA		0.5					
		V _{CC} = 4.5 V, I _{OL} = 48 mA					0.5		
I _I	Parity I/O	V _{CC} = 5.5 V, V _I = 5.5 V		0.1		0.1	mA		
	All other inputs	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1			
I _{IH}	Parity I/O [‡]	V _{CC} = 5.5 V, V _I = 2.7 V		50		50	μA		
	All other inputs			20		20			
I _{IL}	Parity I/O [‡]	V _{CC} = 5.5 V, V _I = 0.4 V		-0.5		-0.5	mA		
	All other inputs			-0.5		-0.5			
I _O [§]		V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	mA		
I _{CC}	Transmit	V _{CC} = 5.5 V		29		29			
	Receive			34		34			

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX						UNIT
			SN54AS286			SN74AS286			
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
t _{PLH}	Any A thru I	Parity I/O	8			8			ns
t _{PHL}			8.5			8.5			
t _{PLH}	Any A thru I	Parity error	9			9			ns
t _{PHL}			9.5			9.5			
t _{PLH}	Parity I/O	Parity error	5			5			ns
t _{PHL}			6			6			
t _{PZH}	XMIT	Parity I/O	5			5			ns
t _{PZL}			6			6			
t _{PHZ}			10			10			
t _{PLZ}			9.5			9.5			

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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TYPICAL APPLICATION DATA

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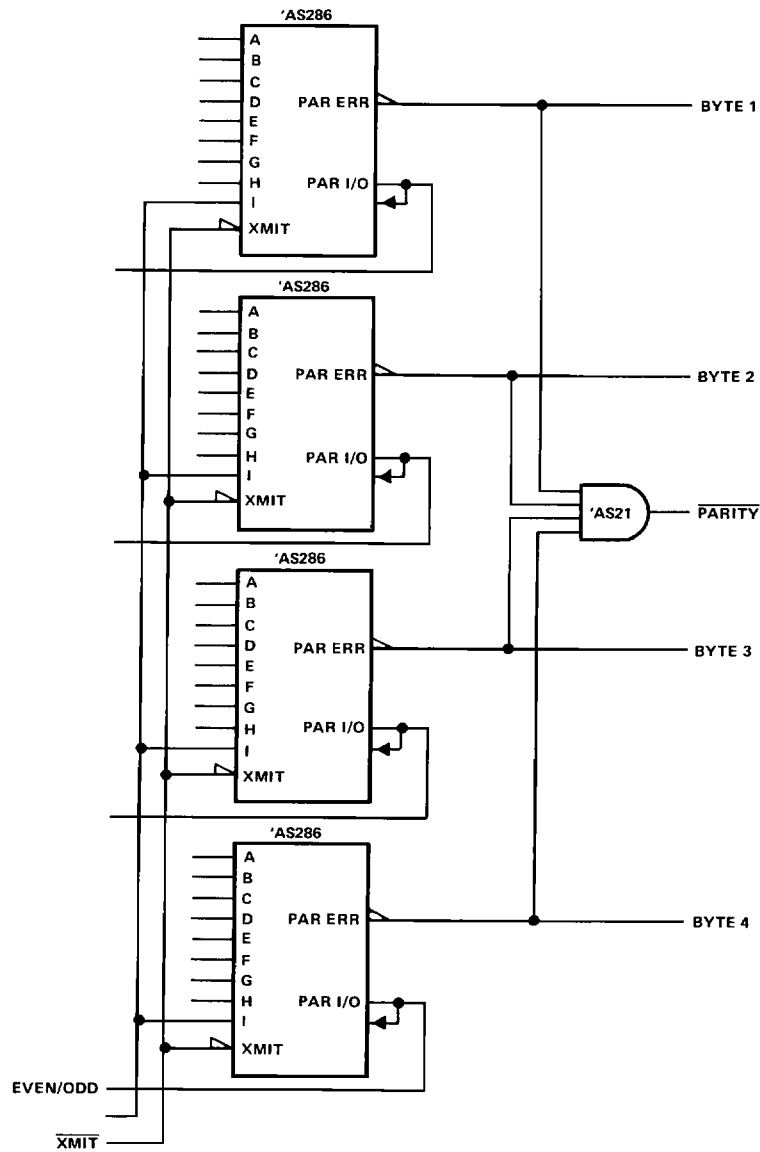


FIGURE 1—32-BIT PARITY GENERATOR/CHECKER

Figure 1 shows a 32-bit parity generator/checker with output polarity-switching, parity error detection, and parity on every byte.

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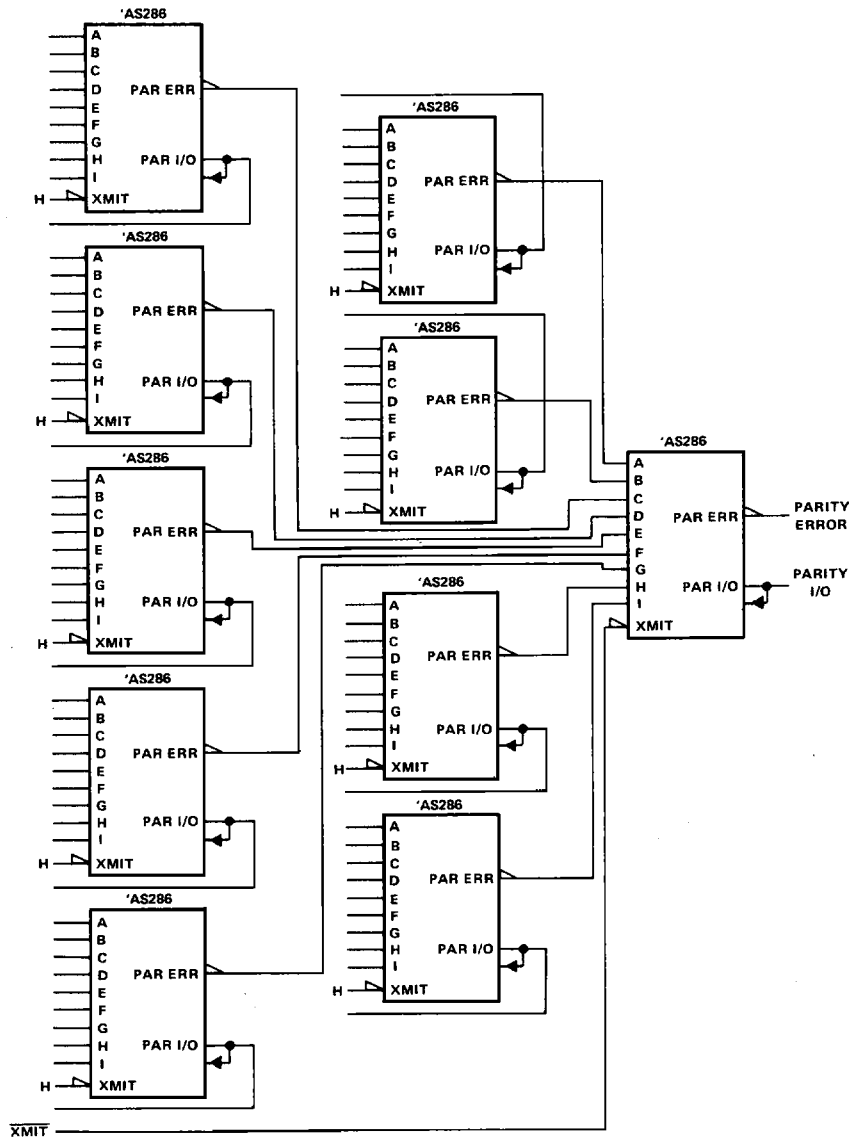


FIGURE 2—90-BIT PARITY GENERATOR/CHECKER WITH PARITY ERROR DETECTION

In Figure 2, a 90-bit parity generator/checker with the $\overline{\text{XMIT}}$ on the last stage is available for use with parity detection.

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