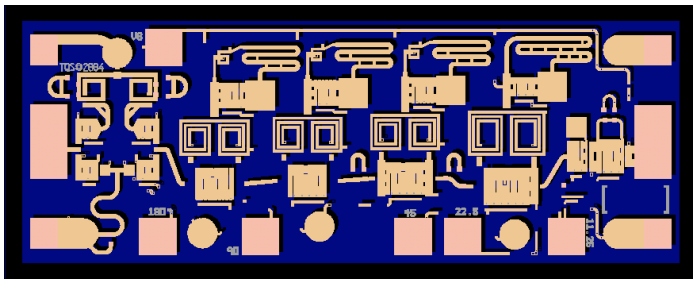
TriQuint SEMICONDUCTOR

Advance Product Information
August 9, 2004

30 GHz 5-Bit Phase Shifter

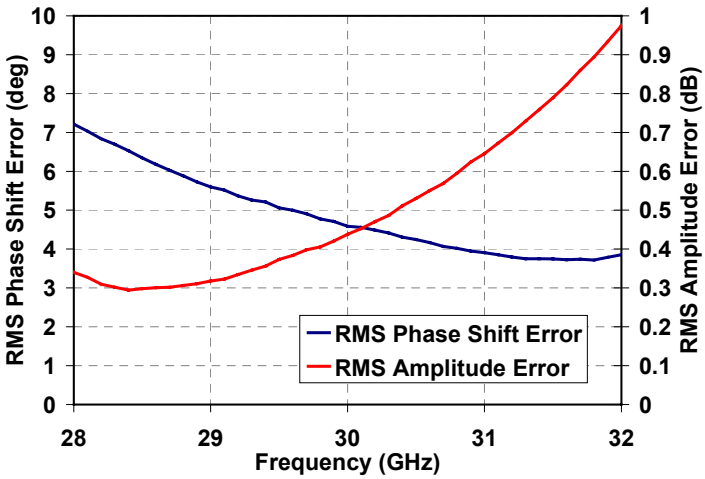
TGP2100-EPU

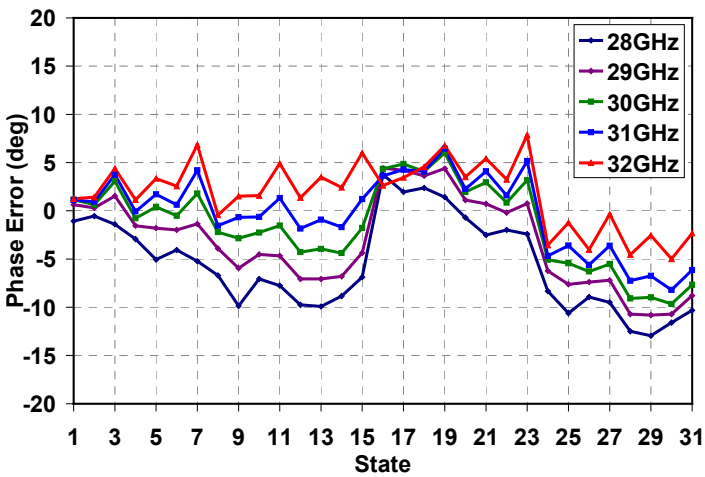


Key Features and Performance

- Positive Control Voltage
- Single-Ended Logic
- CMOS Compatible
- Frequency Range: 28 - 32 GHz
- 0.25µm pHEMT 3MI Technology
- Chip dimensions:
  1.88 x 0.75 x 0.1 mm
  (0.074 x 0.030 x 0.004 inches)

Preliminary Measured Performance





Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

TABLE I
MAXIMUM RATINGS

Symbol	Parameter	Value	Notes
V_C	Control Voltage Range	0 - +8 V	1/ 2/
I_D	Control Supply Current	1 mA	1/ 2/
P_{IN}	Input Continuous Wave Power	20 dBm	1/ 2/
P_D	Power Dissipation	0.1 W	1/ 2/
T_{CH}	Operating Channel Temperature	150 ^{0}C	3/
T_M	Mounting Temperature (30 Seconds)	320 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings represent the maximum operable values for this device

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D at a package base temperature of 70°C

3/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

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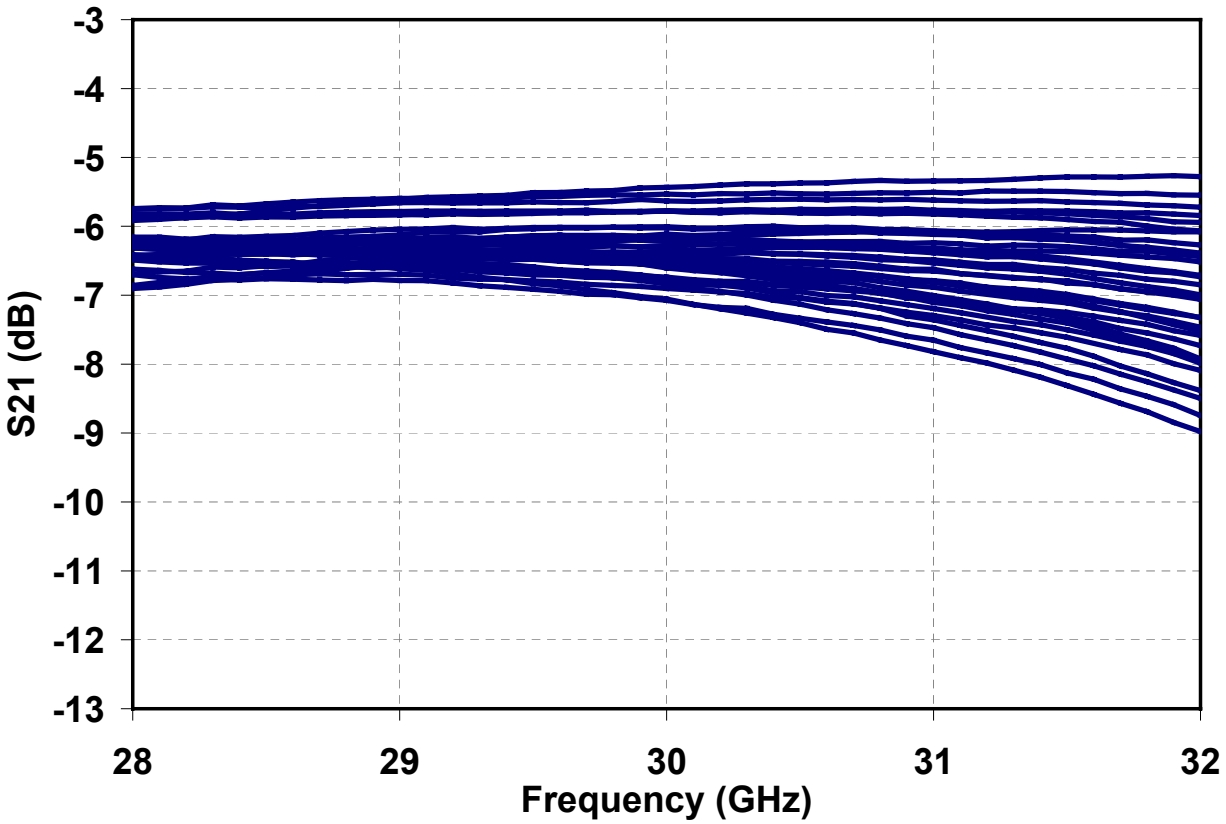
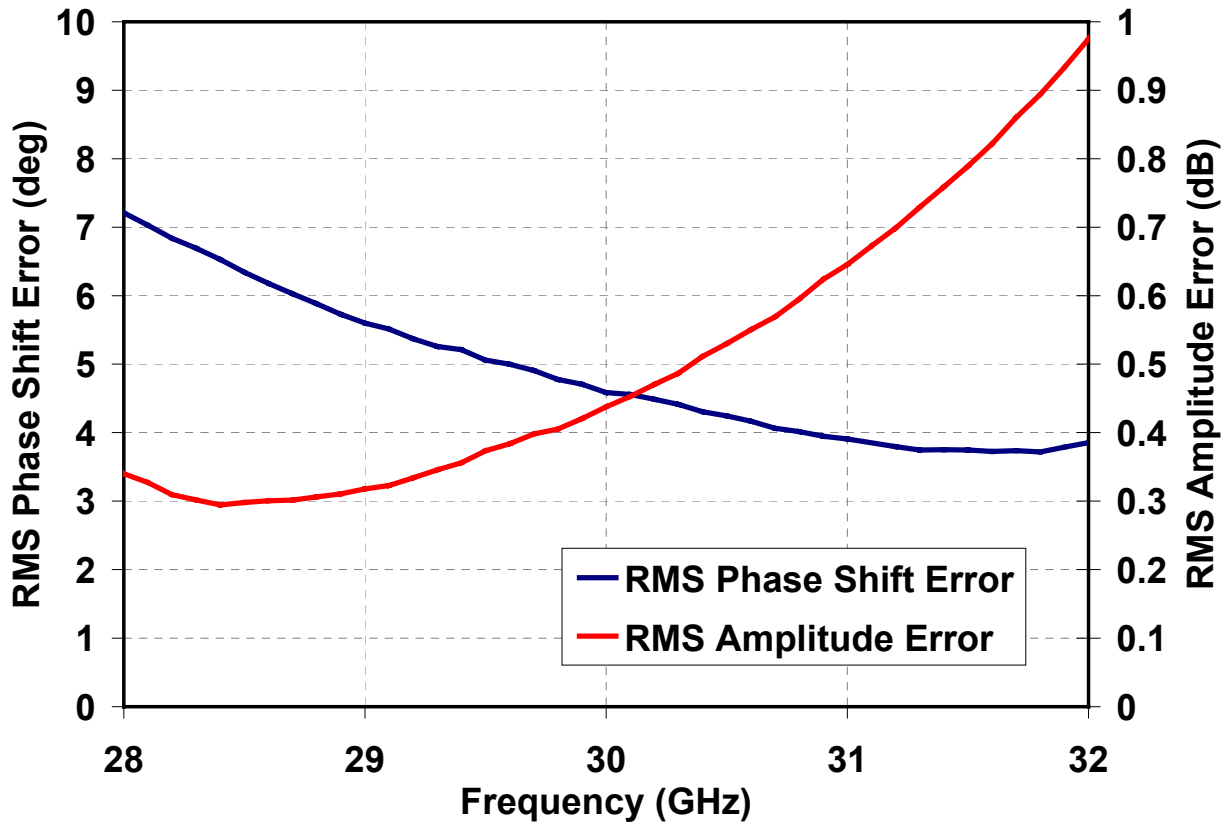
Preliminary Measured Data





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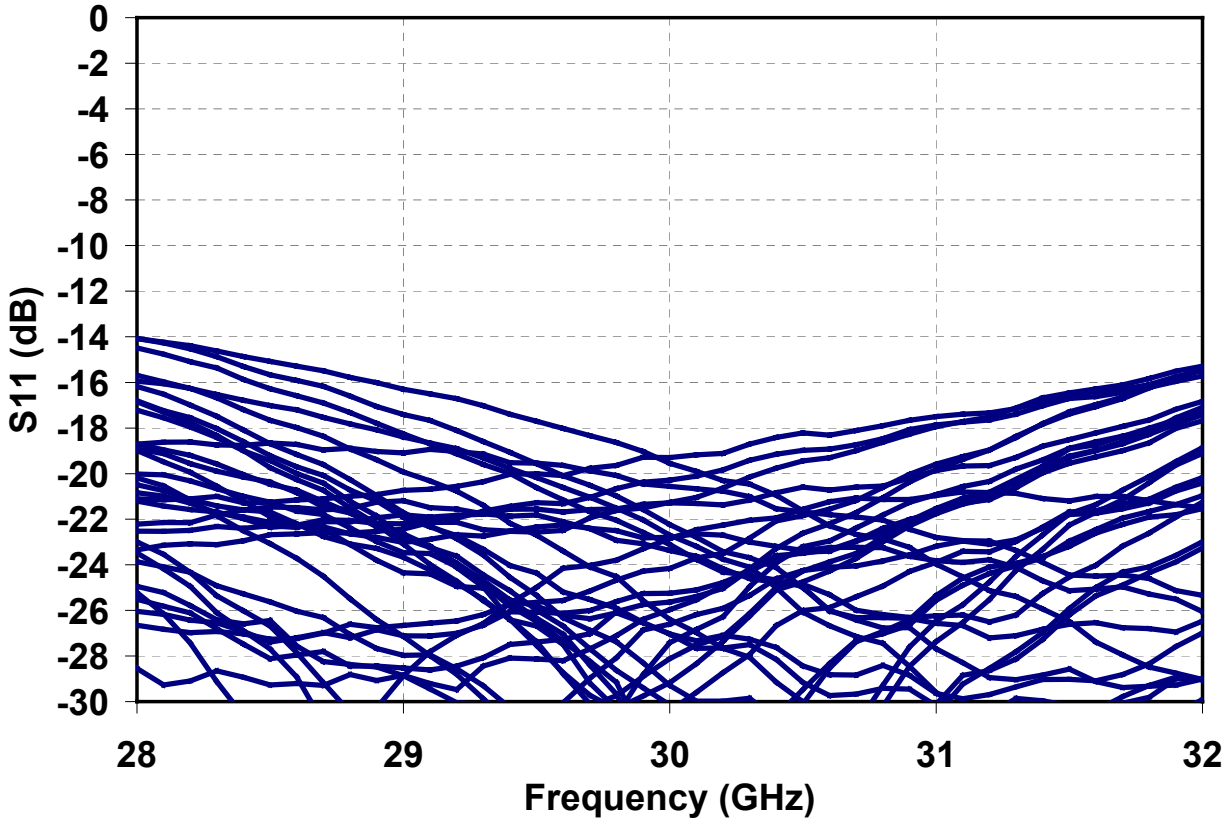

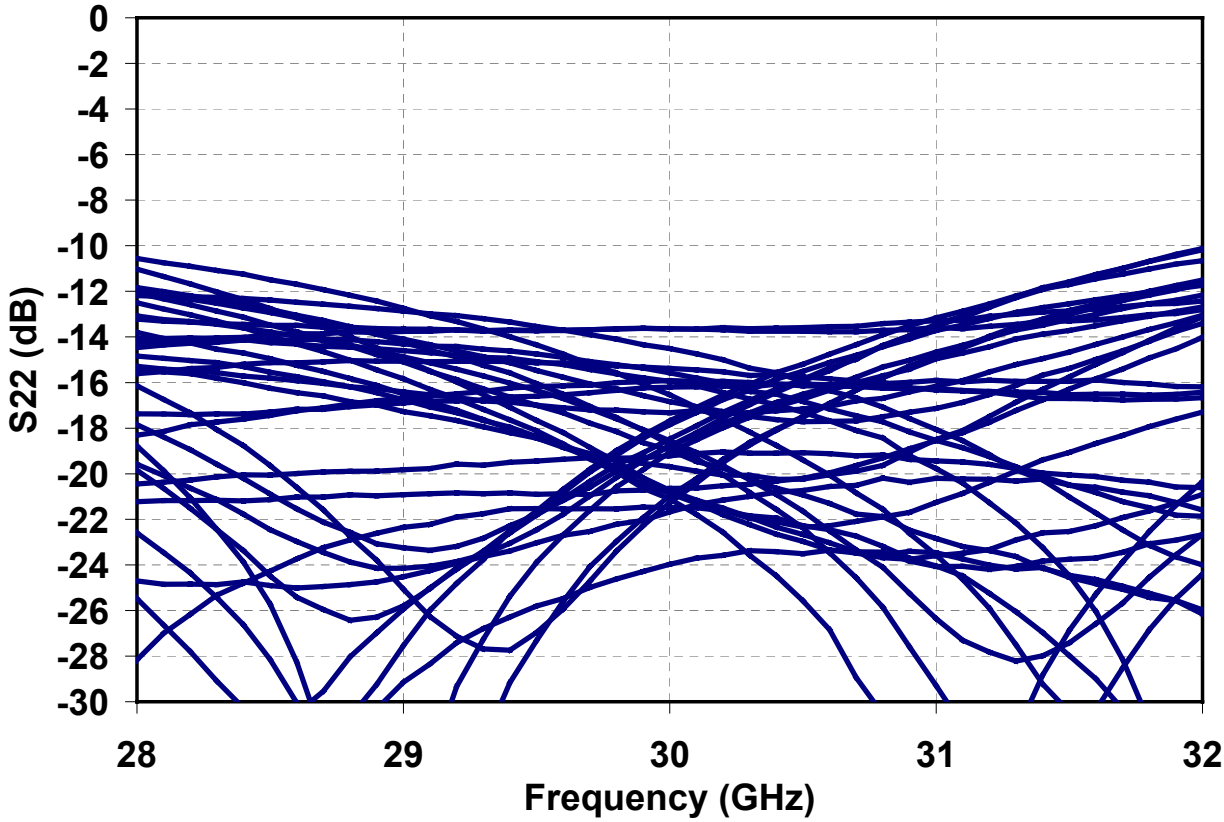

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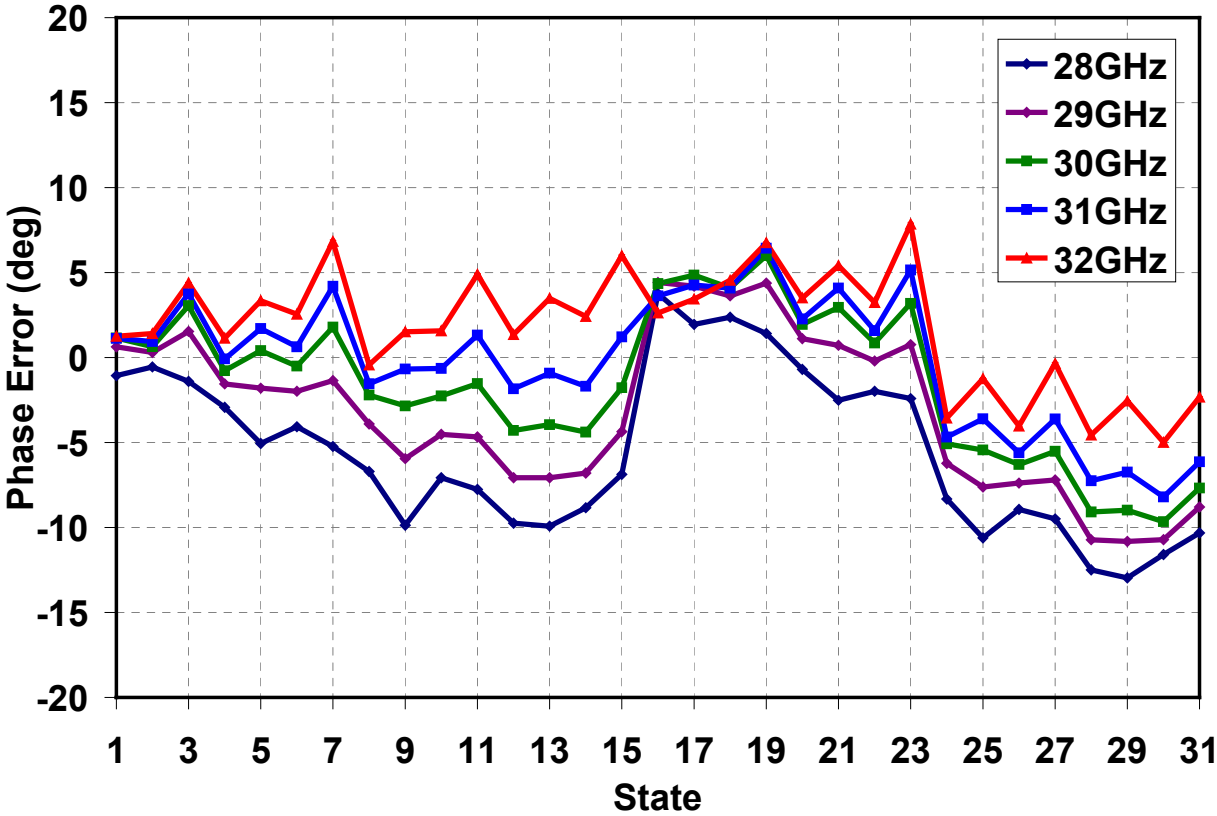

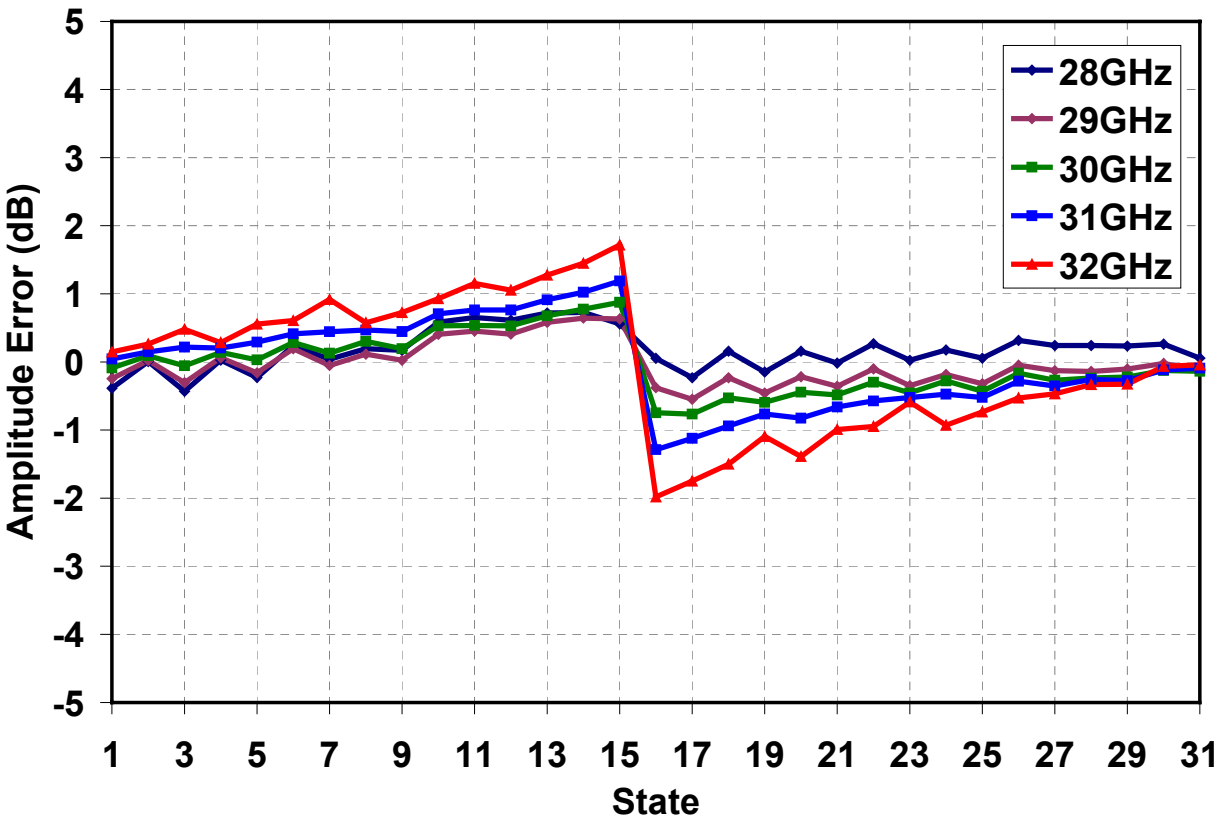

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State Table

State	V-Supply	V-11.25	V-22.5	V-45	V-90	V-180	Phase Shift
0	+5V	0V	0V	0V	0V	0V	Reference
1	+5V	+5V	0V	0V	0V	0V	11.25°
2	+5V	0V	+5V	0V	0V	0V	22.5°
3	+5V	+5V	+5V	0V	0V	0V	33.75°
4	+5V	0V	0V	+5V	0V	0V	45°
5	+5V	+5V	0V	+5V	0V	0V	56.25°
6	+5V	0V	+5V	+5V	0V	0V	67.5°
7	+5V	+5V	+5V	+5V	0V	0V	78.75°
8	+5V	0V	0V	0V	+5V	0V	90°
9	+5V	+5V	0V	0V	+5V	0V	101.25°
10	+5V	0V	+5V	0V	+5V	0V	112.5°
11	+5V	+5V	+5V	0V	+5V	0V	123.75°
12	+5V	0V	0V	+5V	+5V	0V	135°
13	+5V	+5V	0V	+5V	+5V	0V	146.25°
14	+5V	0V	+5V	+5V	+5V	0V	157.5°
15	+5V	+5V	+5V	+5V	+5V	0V	168.75°
16	+5V	0V	0V	0V	0V	+5V	180°
17	+5V	+5V	0V	0V	0V	+5V	191.25°
18	+5V	0V	+5V	0V	0V	+5V	202.5°
19	+5V	+5V	+5V	0V	0V	+5V	213.75°
20	+5V	0V	0V	+5V	0V	+5V	225°
21	+5V	+5V	0V	+5V	0V	+5V	236.25°
22	+5V	0V	+5V	+5V	0V	+5V	247.5°
23	+5V	+5V	+5V	+5V	0V	+5V	258.75°
24	+5V	0V	0V	0V	+5V	+5V	270°
25	+5V	+5V	0V	0V	+5V	+5V	281.25°
26	+5V	0V	+5V	0V	+5V	+5V	292.5°
27	+5V	+5V	+5V	0V	+5V	+5V	303.75°
28	+5V	0V	0V	+5V	+5V	+5V	315°
29	+5V	+5V	0V	+5V	+5V	+5V	326.25°
30	+5V	0V	+5V	+5V	+5V	+5V	337.5°
31	+5V	+5V	+5V	+5V	+5V	+5V	348.75°

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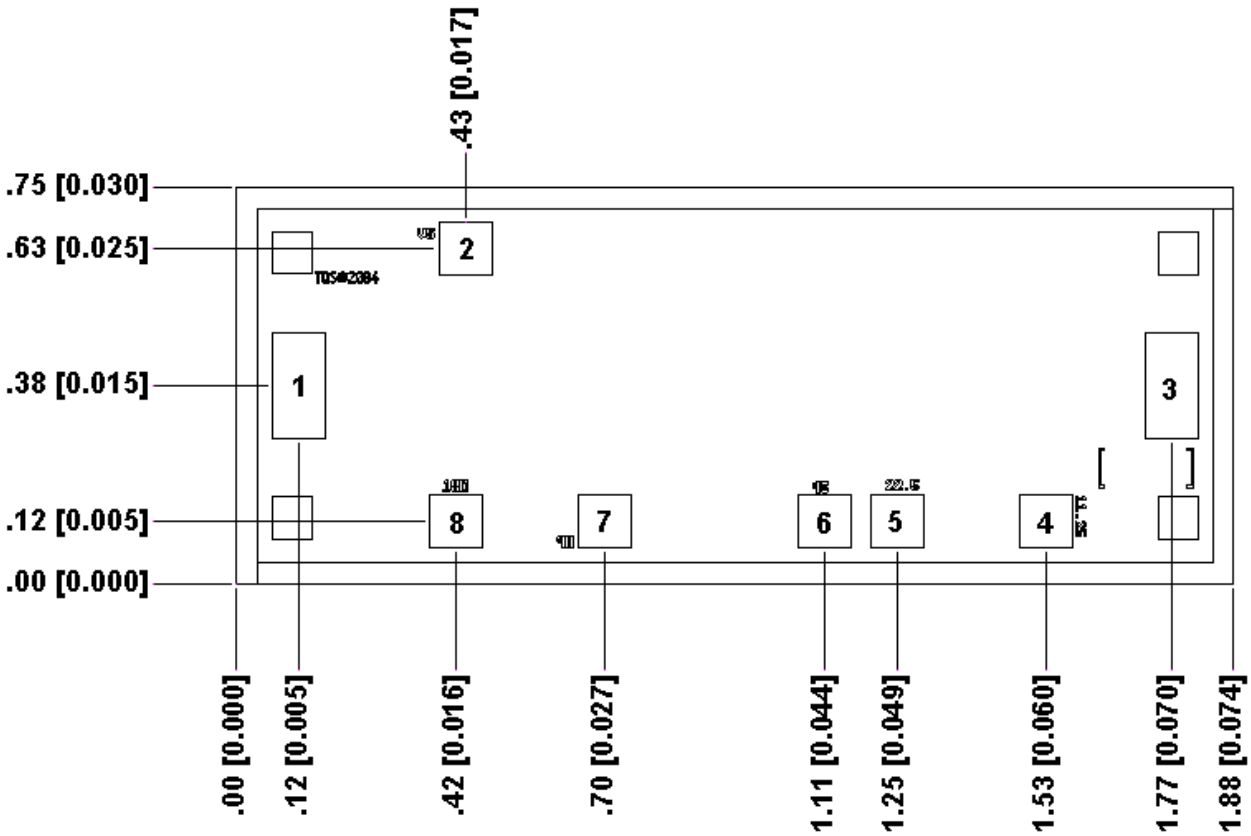
Mechanical Drawing



Units: millimeters [inches]
Thickness: 0.10 [0.004] (reference only)
Chip edge to bond pad dimensions are shown to center of bond pads.
Chip size tolerance: ±0.05 [0.002]
RF ground through backside

Bond Pad #1	**RF Input**	**0.10 x 0.20**	**[0.004 x 0.008]**
Bond Pad #2	**V-Supply (+5V)**	**0.10 x 0.10**	**[0.004 x 0.004]**
Bond Pad #3	**RF Output**	**0.10 x 0.20**	**[0.004 x 0.008]**
Bond Pad #4	**V-11.25 (ON V=+5V)**	**0.10 x 0.10**	**[0.004 x 0.004]**
Bond Pad #5	**V-22.5 (ON V=+5V)**	**0.10 x 0.10**	**[0.004 x 0.004]**
Bond Pad #6	**V-45 (ON V=+5V)**	**0.10 x 0.10**	**[0.004 x 0.004]**
Bond Pad #7	**V-90 (ON V=+5V)**	**0.10 x 0.10**	**[0.004 x 0.004]**
Bond Pad #8	**V-180 (ON V=+5V)**	**0.10 x 0.10**	**[0.004 x 0.004]**

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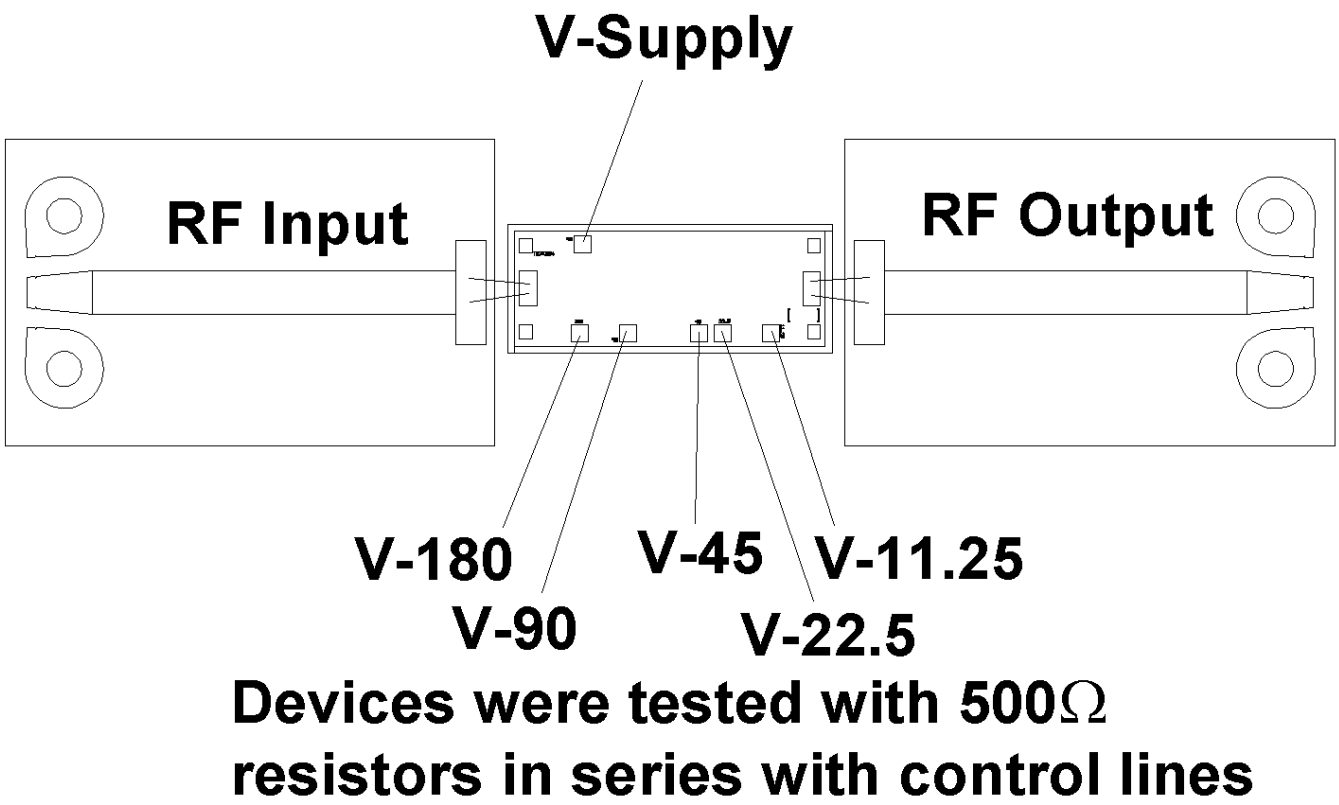
Chip Assembly & Bonding Diagram



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C. (30 seconds maximum)
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200°C.

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