

# Very Low Power Consumption High Gain Optocouplers

## Technical Data

**HCPL-4701**  
**HCPL-4731**  
**HCPL-070A**  
**HCPL-073A**

### Features

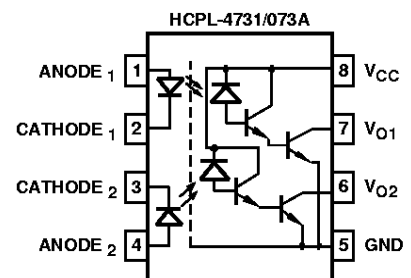
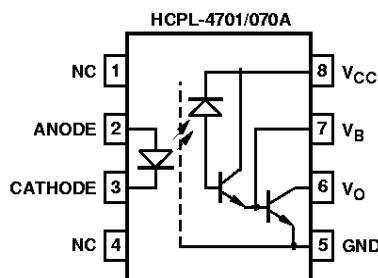
- **Ultra Low Input Current Capability - 40  $\mu$ A**
- **Specified for 3 V Operation**  
 Typical Power Consumption: <1 mW  
 Input Power: <50  $\mu$ W  
 Output Power: <500  $\mu$ W
- **Will Operate with  $V_{CC}$  as Low as 1.6 V**
- **High Current Transfer Ratio - 3500% at  $I_F = 40 \mu$ A**
- **TTL and CMOS Compatible Output**
- **Specified AC and DC Performance over Temperature: 0°C to 70°C**
- **Safety Approval**  
 UL Recognized - 2500 V rms for 1 Minute and 5000 V rms\* for 1 minute per UL1577  
 CSA Approved  
 VDE 0884 Approved with  $V_{IORM} = 630$  V peak (Option 060) for HCPL-4701
- **8-Pin Product Compatible with 6N138/6N139 and HCPL-2730/HCPL-2731**
- **Available in 8-Pin DIP and SOIC-8 Footprint**
- **Through Hole and Surface Mount Assembly Available**

### Applications

- **Battery Operated Applications**
- **ISDN Telephone Interface**
- **Ground Isolation between Logic Families - TTL, LSTTL, CMOS, HCMOS, HL-CMOS, LV-HCMOS**
- **Low Input Current Line Receiver**

- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **AC Line Voltage Status Indicator - Low Input Power Dissipation**
- **Low Power Systems - Ground Isolation**
- **Portable System I/O Interface**

### Functional Diagram



TRUTH TABLE

LED	$V_O$
ON	LOW
OFF	HIGH

\*5000 V rms/1 Minute rating is for Option 020 (HCPL-4701 and HCPL-4731) products only.  
 A 0.1  $\mu$ F bypass capacitor connected between pins 8 and 5 is recommended.

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Description

These devices are very low power consumption, high gain single and dual channel optocouplers. The HCPL-4701 represents the single channel 8-Pin DIP configuration and is pin compatible with the industry standard 6N139. The HCPL-4731 represents the dual channel 8-Pin DIP configuration and is pin compatible with the popular standard HCPL-2731. The HCPL-070A and HCPL-073A are the equivalent single and dual channel products in an SO-8 footprint. Each channel can be driven with an input current as low as 40  $\mu\text{A}$  and has a typical current transfer ratio of 3500%.

These high gain couplers use an AlGaAs LED and an integrated high gain photodetector to provide an extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage results in TTL compatible saturation voltages and high speed operation. Where desired, the  $V_{CC}$  and  $V_O$  terminals may be tied together to achieve conventional Darlington operation (single channel package only).

These devices are designed for use in CMOS, LSTTL or other low power applications. They are

especially well suited for ISDN telephone interface and battery operated applications due to the low power consumption. A 700% minimum current transfer ratio is guaranteed from 0°C to 70°C operating temperature range at 40  $\mu\text{A}$  of LED current and  $V_{CC} \geq 3 \text{ V}$ .

The SO-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

## Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8		Widebody Package (400 mil)	Minimum Input ON Current ( $I_F$ )	Minimum CTR	Absolute Maxi- mum $V_{CC}$	Hermetic
Single Channel Package	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package				Single and Dual Channel Packages HCPL-
6N139 <sup>[1]</sup>	2731 <sup>[1]</sup>	0701 <sup>[1]</sup>	0731 <sup>[1]</sup>	HCNW139 <sup>[1]</sup>	0.5 mA	400%	18 V	
6N138 <sup>[1]</sup>	2730 <sup>[1]</sup>	0700 <sup>[1]</sup>	0730 <sup>[1]</sup>	HCNW138 <sup>[1]</sup>	1.6 mA	300%	7 V	
HCPL-4701	4731	070A	0730A		40 $\mu\text{A}$	800%	18 V	
					0.5 mA	300%	20 V	5701 <sup>[1]</sup> 5700 <sup>[1]</sup> 5731 <sup>[1]</sup> 5730 <sup>[1]</sup>

### Notes:

1. Technical data are on separate HP publication.

## Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

HCPL-4701#XXX

- 020 = 5000 V rms/1 minute UL Rating Option.\*\*
- 060 = VDE 0884  $V_{IORM} = 630 \text{ V}$  peak Option†
- 300 = Gull Wing Surface Mount Option.\*
- 500 = Tape and Reel Packaging Option.

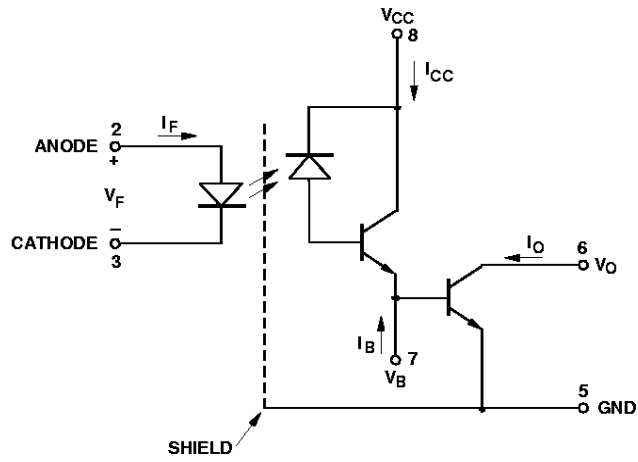
\*Gull wing surface mount option applies to through hole parts only.

\*\*For HCPL-4701 and HCPL-4731 (8-Pin DIP products) only.

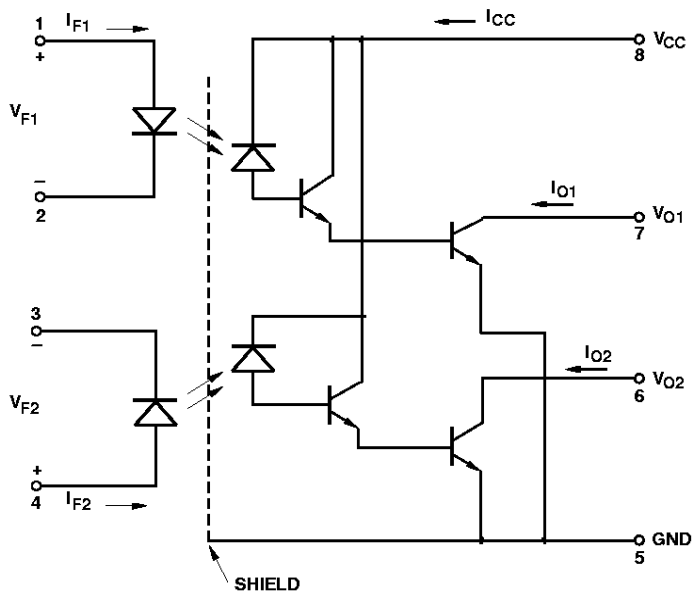
†For HCPL-4701 only. Combination of Option 020 and Option 060 is not available.

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

## Schematic HCPL-4701 and HCPL-070A

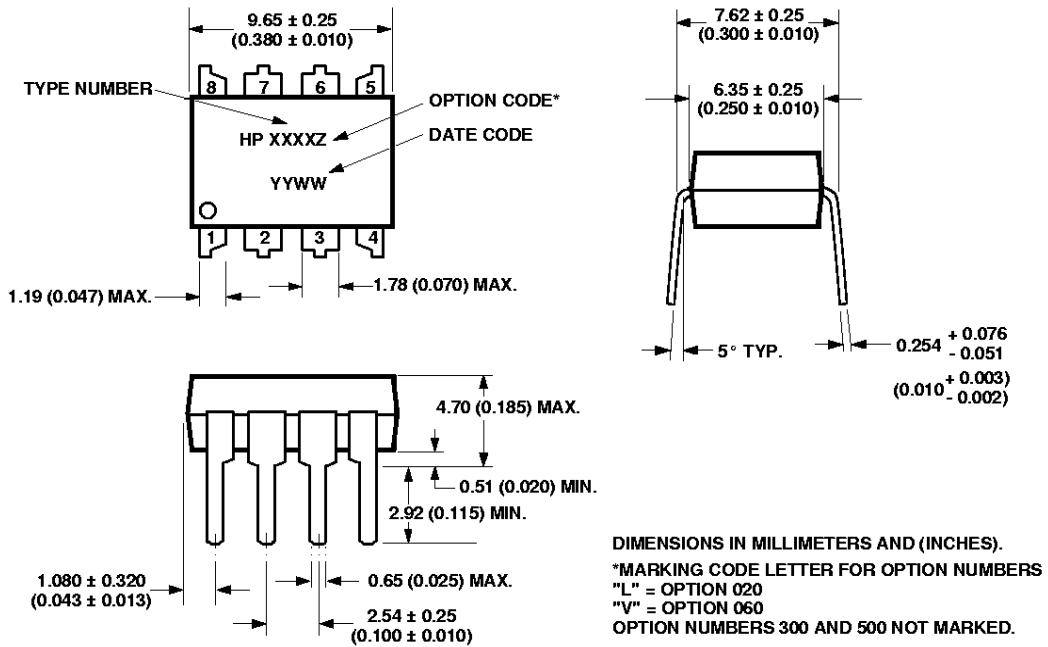


## HCPL-4731 and HCPL-073A

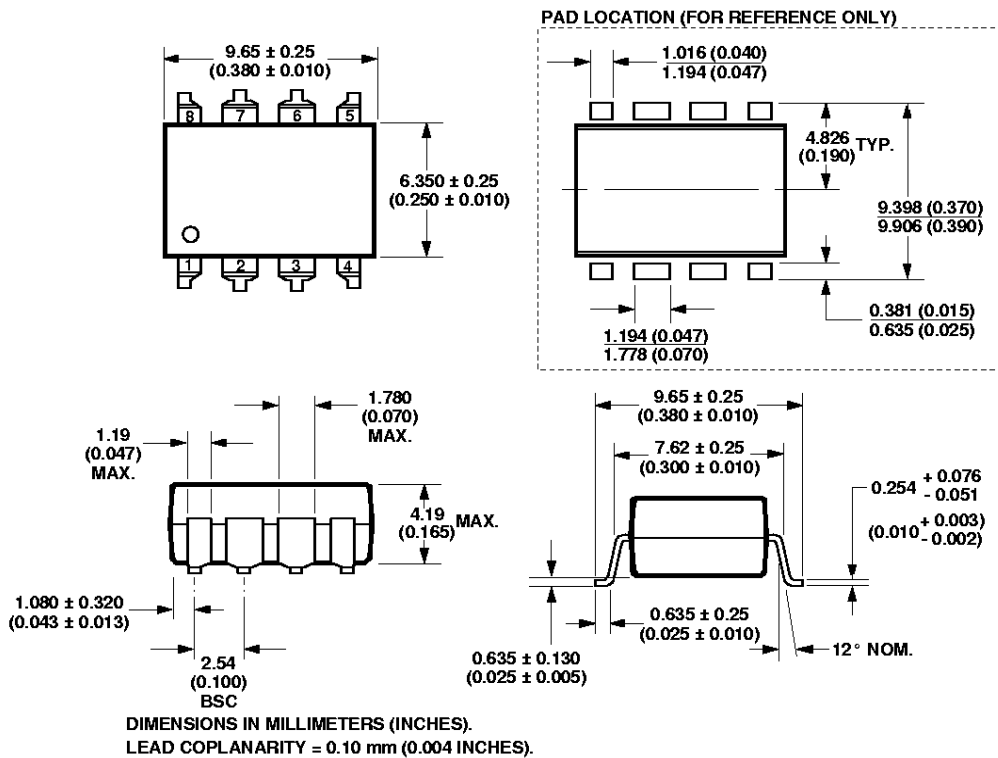


USE OF A 0.1  $\mu$ F BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 8)

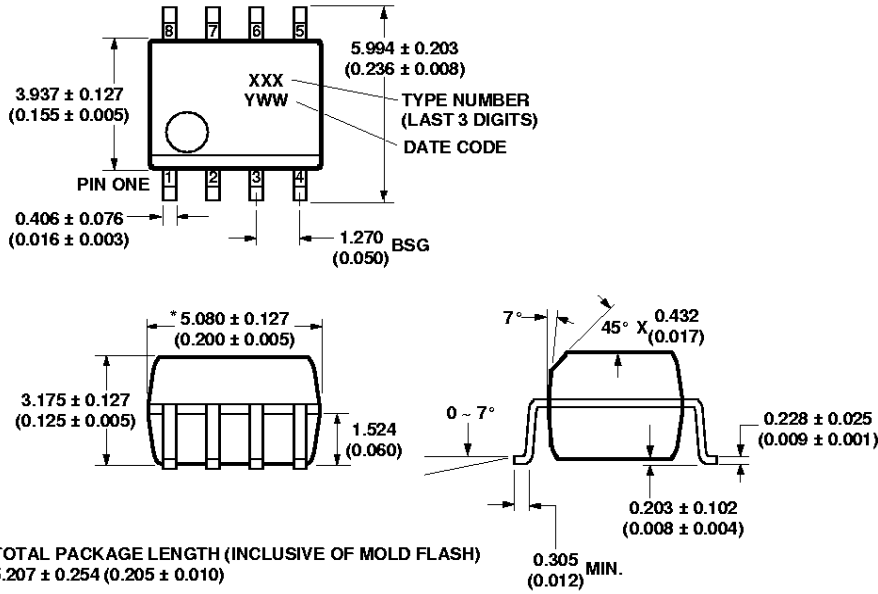
### Package Outline Drawings 8-Pin DIP Package (HCPL-4701, HCPL-4731)



### 8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4701, HCPL-4731)

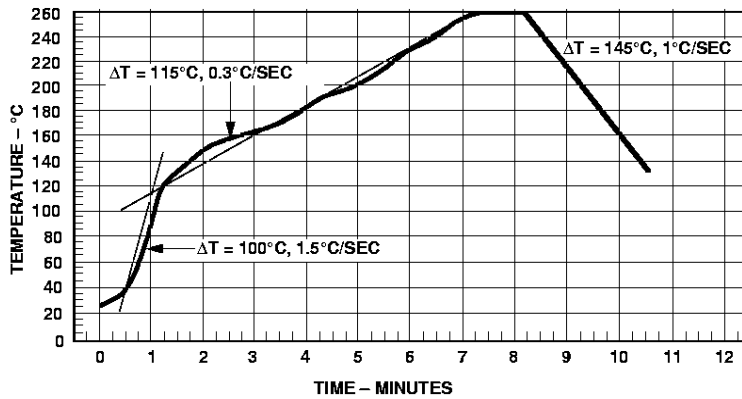


**Small-Outline SO-8 Package (HCPL-070A, HCPL-073A)**



DIMENSIONS IN MILLIMETERS (INCHES).  
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

**Solder Reflow Temperature Profile**



Note: Use of nonchlorine activated fluxes is highly recommended.

Figure 1. Solder Reflow Thermal Profile (HCPL-070A, HCPL-073A, and Gull Wing Surface Mount Option 300 Parts).

**Regulatory Information**

The HCPL-4701/4731 and HCPL-070A/073A have been approved by the following organizations:

**CSA**

Approved under CSA Component Acceptance Notice #5, File CA 88324.

**UL**

Recognized under UL 1577, Component Recognition Program, File E55361.

**VDE**

Approved according to VDE 0884/06.92 (Option 060 only).

**Insulation Related Specifications**

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/ VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

**VDE 0884 Insulation Related Characteristics (HCPL-4701 OPTION 060 ONLY)**

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 300$ V rms for rated mains voltage $\leq 450$ V rms		I-IV I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	630	V <sub>peak</sub>
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.87 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	1181	V <sub>peak</sub>
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.5 = V_{PR}$ , Type and sample test, $t_m = 60$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	945	V <sub>peak</sub>
Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini} = 10$ sec)	$V_{IOTM}$	6000	V <sub>peak</sub>
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.) Case Temperature Input Current Output Power	$T_S$ $I_{S,INPUT}$ $P_{S,OUTPUT}$	175 230 600	$^{\circ}C$ mA mW
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

\*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

## Absolute Maximum Ratings

(No Derating Required up to 70°C)

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	$T_S$	-55	125	°C
Operating Temperature	$T_A$	-40	85	°C
Average Forward Input Current (HCPL-4701/4731)	$I_{F(AVG)}$		10	mA
Average Forward Input Current (HCPL-070A/073A)	$I_{F(AVG)}$		5	mA
Peak Transient Input Current (HCPL-4701/4731) (50% Duty Cycle, 1 ms Pulse Width)	$I_{FPK}$		20	mA
Peak Transient Input Current (HCPL-070A/073A) (50% Duty Cycle, 1 ms Pulse Width)	$I_{FPK}$		10	mA
Reverse Input Voltage	$V_R$		2.5	V
Input Power Dissipation (Each Channel)	$P_I$		15	mW
Output Current (Each Channel)	$I_O$		60	mA
Emitter Base Reverse Voltage (HCPL-4701/070A)	$V_{EB}$		0.5	V
Output Transistor Base Current (HCPL-4701/070A)	$I_B$		5	mA
Supply Voltage	$V_{CC}$	-0.5	18	V
Output Voltage	$V_O$	-0.5	18	V
Output Power Dissipation (Each Channel)	$P_O$		100	mW
Total Power Dissipation (Each Channel)	$P_T$		115	mW
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane			
Reflow Temperature Profile (for SOIC-8 and Option #300)	See <b>Package Outline Drawings</b> section			

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$V_{CC}^*$	1.6	18	V
Forward Input Current (ON)	$I_{F(ON)}$	40	5000	μA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	$T_A$	0	70	°C

\*See Note 1.

### Electrical Specifications

$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $4.5\text{ V} \leq V_{CC} \leq 20\text{ V}$ ,  $1.6\text{ mA} \leq I_{F(\text{ON})} \leq 5\text{ mA}$ ,  $0\text{ V} \leq V_{F(\text{OFF})} \leq 0.8\text{ V}$ , unless otherwise specified. All Typical at  $T_A = 25^{\circ}\text{C}$ . See note 8.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR		800	3500	25k	%	$I_F = 40\ \mu\text{A}$ , $V_O = 0.4\text{ V}$ $V_{CC} = 4.5\text{ V}$	4, 5	2
			600	3000	8k		$I_F = 0.5\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		
			700	3200	25k		$I_F = 40\ \mu\text{A}$		
			500	2700	8k		$I_F = 0.5\text{ mA}$		
Logic Low Output Voltage	$V_{OL}$			0.06	0.4	V	$I_F = 40\ \mu\text{A}$ , $I_O = 280\ \mu\text{A}$	2, 3	
				0.04	0.4		$I_F = 0.5\text{ mA}$ , $I_O = 2.5\text{ mA}$		
Logic High Output Current	$I_{OH}$			0.01	5	$\mu\text{A}$	$V_O = V_{CC} = 3\text{ to }7\text{ V}$ , $I_F = 0\text{ mA}$		
				0.02	80		$V_O = V_{CC} = 18\text{ V}$ , $I_F = 0\text{ mA}$		
Logic Low Supply Current	$I_{CCL}$	4701/070A		0.02	0.2	mA	$I_F = 40\ \mu\text{A}$	$V_O = \text{Open}$	
				0.1	1		$I_F = 0.5\text{ mA}$		
		4731/073A		0.04	0.4		$I_F = 40\ \mu\text{A}$		
				0.2	2.0		$I_F = 0.5\text{ mA}$		
Logic High Supply Current	$I_{CCH}$	4701/070A		<0.01	10	$\mu\text{A}$	$I_F = 0\text{ mA}$	$V_O = \text{Open}$	
Supply Current		4731/073A		<0.01	20				
Input Forward Voltage	$V_F$		1.1	1.25	1.4	V	$I_F = 40\text{ to }500\ \mu\text{A}$ , $T_A = 25^{\circ}\text{C}$	6	
			0.95		1.5				
Input Reverse Breakdown Voltage	$BV_R$		3.0	5.0		V	$I_R = 100\ \mu\text{A}$ , $T_A = 25^{\circ}\text{C}$		
			2.5		$I_R = 100\ \mu\text{A}$				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$			-2.0		mV/ $^{\circ}\text{C}$	$I_F = 40\ \mu\text{A}$		
				-1.6	$I_F = 0.5\text{ mA}$				
Input Capacitance	$C_{IN}$			18		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		

\*All typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 5\text{ V}$ , unless otherwise noted.

## Switching Specifications (AC)

Over Recommended Operating Conditions  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $18\text{ V}$ , unless otherwise specified.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note		
Propagation Delay Time to Logic Low at Output	$t_{PHL}$			65	500	$\mu\text{s}$	$I_F = 40\ \mu\text{A}$ , $R_L = 11$ to $16\ \text{k}\Omega$ , $V_{CC} = 3.3$ to $5\ \text{V}$	7, 9	9, 10		
				3	25					$T_A = 25^\circ\text{C}$	$I_F = 0.5\ \text{mA}$ , $R_L = 4.7\ \text{k}\Omega$
					30						
Propagation Delay Time to Logic High Output	$t_{PLH}$			70	500	$\mu\text{s}$	$I_F = 40\ \mu\text{A}$ , $R_L = 11$ to $16\ \text{k}\Omega$ , $V_{CC} = 3.3$ to $5\ \text{V}$	7, 9	9, 10		
				34	60					$T_A = 25^\circ\text{C}$	$I_F = 0.5\ \text{mA}$ , $R_L = 4.7\ \text{k}\Omega$
					4701/4731						
				070A/073A	130						
Common Mode Transient Immunity at Logic High Output	$ CM_H $		1,000	10,000		$\text{V}/\mu\text{s}$	$I_F = 0\ \text{mA}$ , $R_L = 4.7$ to $11\ \text{k}\Omega$ , $V_{CM} = 10\ \text{V}_{p-p}$ , $T_A = 25^\circ\text{C}$ ,	8	6, 7		
Common Mode Transient Immunity at Logic Low Output	$ CM_L $		1,000	10,000		$\text{V}/\mu\text{s}$	$I_F = 0.5\ \text{mA}$ , $R_L = 4.7$ to $11\ \text{k}\Omega$ , $ V_{CM}  = 10\ \text{V}_{p-p}$ , $T_A = 25^\circ\text{C}$	8	6, 7		
				2,000						$I_F = 40\ \mu\text{A}$ , $R_L = 11$ to $16\ \text{k}\Omega$ , $ V_{CM}  = 10\ \text{V}_{p-p}$ , $V_{CC} = 3.3$ to $5\ \text{V}$ , $T_A = 25^\circ\text{C}$	

\*All typical values at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\ \text{V}$ , unless otherwise noted.

## Package Characteristics

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	$V_{ISO}$		2500			$\text{V rms}$	$RH \leq 50\%$ , $t = 1\ \text{min.}$ , $T_A = 25^\circ\text{C}$		3, 4
				4701 4731	5000				
Resistance (Input-Output)	$R_{I-O}$			$10^{12}$		$\Omega$	$V_{I-O} = 500\ \text{VDC}$ $RH \leq 45\%$		3
Capacitance (Input-Output)	$C_{I-O}$			0.6		$\text{pF}$	$f = 1\ \text{MHz}$		3
Insulation Leakage Current (Input-Input)	$I_{I-I}$	4731 073A		0.005		$\mu\text{A}$	$RH \leq 45\%$ , $t = 5\ \text{s}$ , $V_{I-I} = 500\ \text{VDC}$		5
Resistance (Input-Input)	$R_{I-I}$			$10^{11}$		$\Omega$			
Capacitance (Input-Input)	$C_{I-I}$	4731		0.03		$\text{pF}$	$f = 1\ \text{MHz}$		5
		073A		0.25					

\*All typical values at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\ \text{V}$ .

\*\*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

**Notes:**

1. Specification information is available from the factory for 1.6 V operation. Call your local field sales office for further information.
2. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 3000 V_{RMS}$  for 1 second (leakage detection current limit,  $I_{L,O} \leq 5 \mu A$ ).
- 4a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000 V_{RMS}$  for 1 second (leakage

- detection current limit,  $I_{L,O} \leq 5 \mu A$ . This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
  6. Common transient immunity in a Logic High level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a Logic High state (i.e.,  $V_O > 2.0 V$ ). Common transient immunity in a Logic Low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a Logic Low state (i.e.,  $V_O < 0.8 V$ ).

7. In applications where  $dV/dt$  may exceed  $50,000 V/\mu s$  (such as static discharge) a series resistor,  $R_{CC}$ , should be included to protect the detector IC from destructively high surge currents. The recommended value is  $R_{CC} = 220 \Omega$ .
8. Use of a  $0.1 \mu F$  bypass capacitor connected between pins 8 and 5 adjacent to the device is recommended.
9. Pin 7 open for single channel product.
10. Use of resistor between pins 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below  $47 k\Omega$  for single channel product.
11. The Applications Information section of this data sheet references the HCPL-47XX part family, but applies equally to the HCPL-070A and HCPL-073A parts.

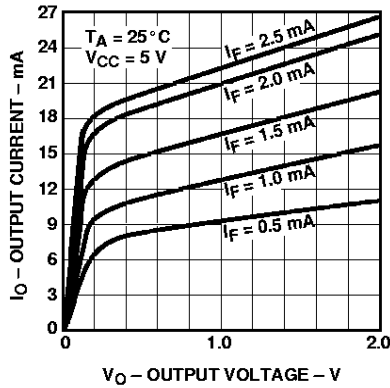


Figure 2. DC Transfer Characteristics ( $I_F = 0.5 \text{ mA}$  to  $2.5 \text{ mA}$ ).

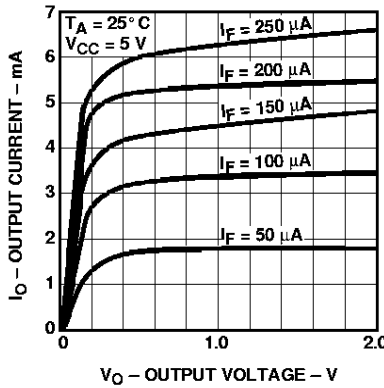


Figure 3. DC Transfer Characteristics ( $I_F = 50 \mu A$  to  $250 \mu A$ ).

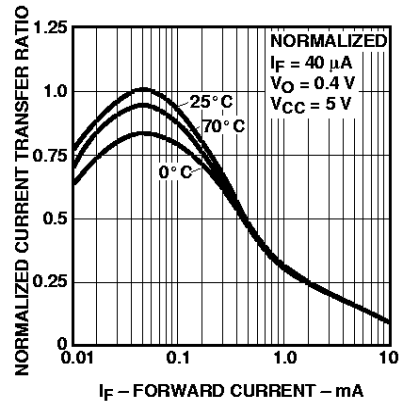


Figure 4. Current Transfer Ratio vs. Forward Current.

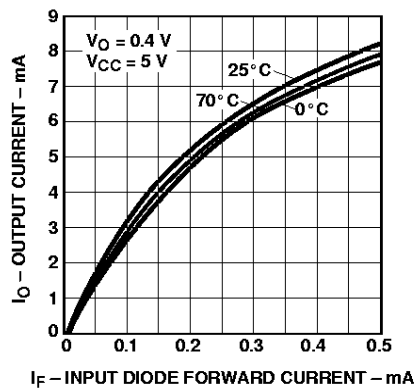


Figure 5. Output Current vs. Input Diode Forward Current.

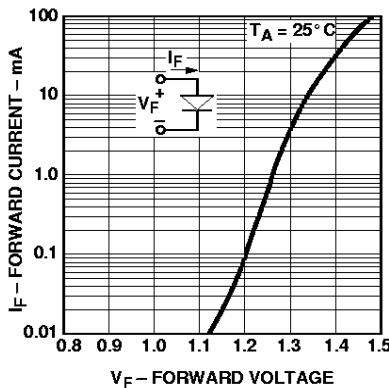


Figure 6. Input Diode Forward Current vs. Forward Voltage.

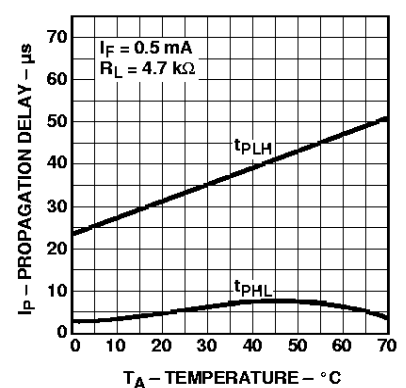


Figure 7. Propagation Delay vs. Temperature.



**Table 1. Typical HCPL-4701 Power Dissipation for 3 V and 5 V Applications**

Power Dissipation ( $\mu\text{W}$ )	$V_{\text{CC}} = 3.3 \text{ Vdc}$		$V_{\text{CC}} = 5 \text{ Vdc}$	
	$I_{\text{F}} = 40 \mu\text{A}$	$I_{\text{F}} = 500 \mu\text{A}$	$I_{\text{F}} = 40 \mu\text{A}$	$I_{\text{F}} = 500 \mu\text{A}$
$P_{\text{LED}}$	50	625	50	625
$P_{\text{VCC}}$	65	330	100	500
$P_{\text{O-C}}^{[1]}$	20	10	25	20
$P_{\text{TOTAL}}^{[2]}$	135 $\mu\text{W}$	965 $\mu\text{W}$	175 $\mu\text{W}$	1,145 $\mu\text{W}$

**Notes:**

- $R_{\text{L}}$  of 11 k $\Omega$  open-collector (o-c) pull-up resistor was used for both 3.3 Vdc and 5 Vdc calculations.
- For typical total interface circuit power consumption in 3.3 Vdc application, add to  $P_{\text{TOTAL}}$  approximately 80  $\mu\text{W}$  for 40  $\mu\text{A}$  (1,025  $\mu\text{W}$  for 500  $\mu\text{A}$ ) LED current-limiting resistor, and 960  $\mu\text{W}$  for the 11 k $\Omega$  pull-up resistor power dissipations. Similarly, for 5 Vdc applications, add to  $P_{\text{TOTAL}}$  approximately 150  $\mu\text{W}$  for 40  $\mu\text{A}$  (1,875  $\mu\text{W}$  for 500  $\mu\text{A}$ ) LED current-limiting resistor and 2,230  $\mu\text{W}$  for the 11 k $\Omega$  pull-up resistor power dissipations.

**Propagation Delay**

When the HCPL-47XX optocoupler is operated under very low input and output current conditions, the propagation delay times will lengthen. When lower input drive current level is used to switch the high-efficiency AlGaAs LED, the slower the charge and discharge time will be for the LED. Correspondingly, the propagation delay times will become longer as a result. In addition, the split-Darlington (open-collector) output amplifier needs a larger, pull-up load resistance to ensure the output current is within a controllable range. Applications that are not sensitive to longer propagation delay times and that are easily served by this HCPL-47XX optocoupler, typically 65  $\mu\text{s}$  or greater, are those of status monitoring of a telephone line, power line, battery condition of a portable unit, etc. For faster HCPL-47XX propagation delay times, approximately 30  $\mu\text{s}$ , this optocoupler needs to operate at higher  $I_{\text{F}}$  ( $\geq 500 \mu\text{A}$ ) and  $I_{\text{O}}$  ( $\geq 1 \text{ mA}$ ) levels.

**Applications****Battery-Operated Equipment**

Common applications for the HCPL-47XX optocoupler are within battery-operated, portable equipment, such as test or medical instruments, computer peripherals and accessories where energy conservation is required to maximize battery life. In these applications, the optocoupler would monitor the battery voltage and provide an isolated output to another electrical system to indicate battery status or the need to switch to a backup supply or begin a safe shutdown of the equipment via a communication port. In addition, the HCPL-47XX optocouplers are specified to operate with 3 Vdc CMOS logic family of devices to provide logic-signal isolation between similar or different logic circuit families.

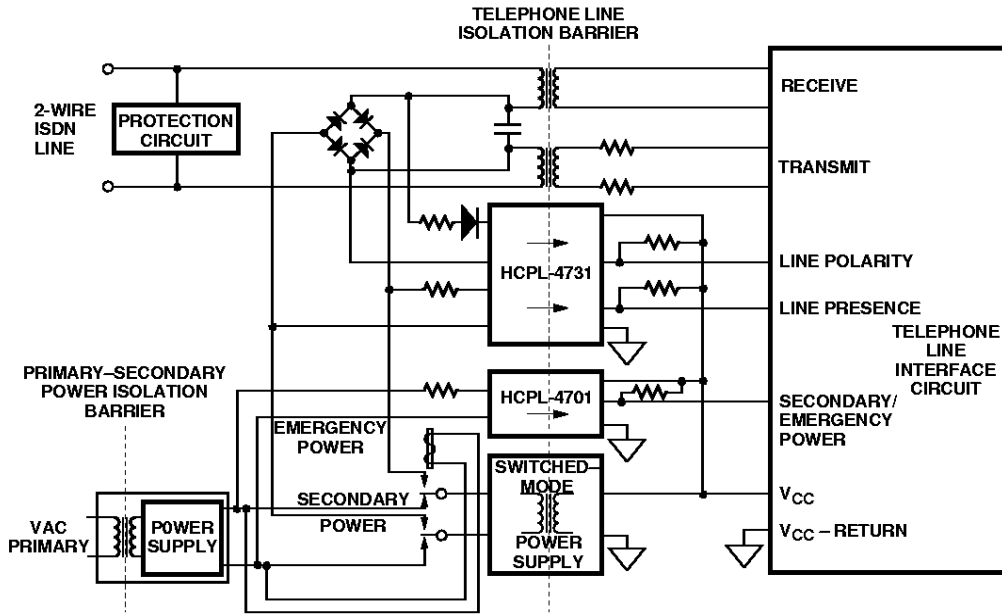
**Telephone Line Interfaces**

Applications where the HCPL-47XX optocoupler would be best used are in telephone line interface circuitry for functions of ring detection, on-off hook detection, line polarity, line presence and

supplied-power sensing. In particular, Integrated Services Digital Network (ISDN) applications, as illustrated in Figure 10, can severely restrict the input power that an optocoupler interface circuit can use (approximately 3 mW). Figure 10 shows three isolated signals that can be served by the small input LED current of the HCPL-47XX dual- and single-channel optocouplers. Very low, total power dissipation occurs with these series of devices.

**Switched-Mode Power Supplies**

Within Switched-Mode Power Supplies (SMPS) the less power consumed the better. Isolation for monitoring line power, regulation status, for use within a feedback path between primary and secondary circuits or to external circuits are common applications for optocouplers. Low-power HCPL-47XX optocoupler can help keep higher energy conversion efficiency for the SMPS. The block diagram of Figure 11 shows where low-power isolation can be used.



NOTE: THE CIRCUITS SHOWN IN THIS FIGURE REPRESENT POSSIBLE, FUNCTIONAL APPLICATION OF THE HCPL-47XX OPTOCOUPLER TO AN ISDN LINE INTERFACE. THIS CIRCUIT ARRANGEMENT DOES NOT GUARANTEE COMPLIANCE, CONFORMITY, OR ACCEPTANCE TO AN ISDN, OR OTHER TELECOMMUNICATION STANDARD, OR TO FCC OR TO OTHER GOVERNMENTAL REGULATORY AGENCY REQUIREMENTS. THESE CIRCUITS ARE RECOMMENDATIONS THAT MAY MEET THE NEEDS OF THESE APPLICATIONS. HEWLETT-PACKARD DOES NOT IMPLY, REPRESENT, NOR GUARANTEE THAT THESE CIRCUIT ARRANGEMENTS ARE FREE FROM PATENT INFRINGEMENT.

Figure 10. HCPL-47XX Isolated Monitoring Circuits for 2-Wire ISDN Telephone Line.

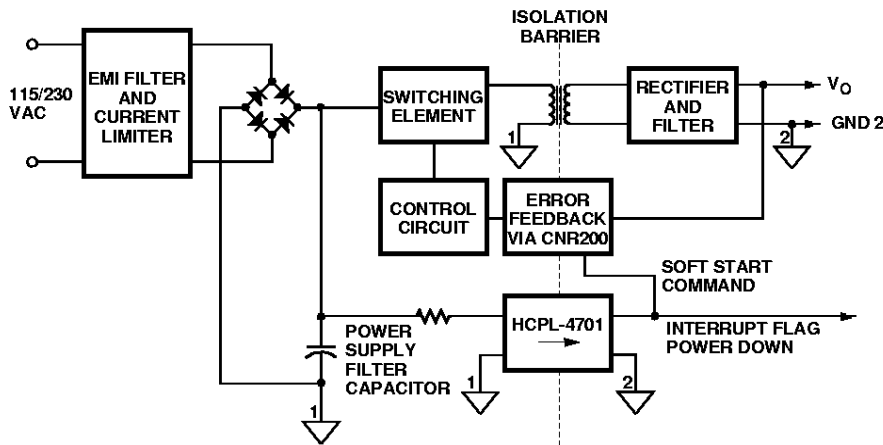


Figure 11. Typical Optical Isolation Used for Power-Loss Indication and Regulation Signal Feedback.

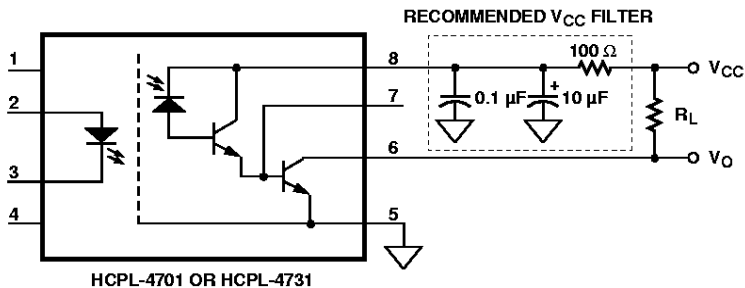


Figure 12. Recommended Power Supply Filter for HCPL-47XX Optocouplers.

### Data Communication and Input/Output Interfaces

In data communication, the HCPL-47XX can be used as a line receiver on a RS-232-C line or this optocoupler can be part of a proprietary data link with low input current, multi-drop stations along the data path. Also, this low-power optocoupler can be used within equipment that monitors the presence of high-voltage. For example, a benefit of the low input LED current (40  $\mu\text{A}$ ) helps the input sections of a Programmable Logic Controller (PLC) monitor proximity and limit switches. The PLC I/O sections can benefit from low input current optocouplers because the total input power dissipation when monitoring the high voltage (120 Vac - 220 Vac) inputs is minimized at the I/O connections. This is especially important when many input channels are stacked together.

### Circuit Design Issues

#### Power Supply Filtering

Since the HCPL-47XX is a high-gain, split-Darlington amplifier, any conducted electrical noise on the  $V_{CC}$  power supply to this optocoupler should be minimized. A recommended  $V_{CC}$  filter circuit is shown in Figure 12 to improve the power supply rejection (psr) of the optocoupler. The filter should be located near the combination of pin 8 and pin 5 to provide best filtering action. This filter will drastically limit any sudden rate of change of  $V_{CC}$  with time to a slower rate that cannot interfere with the optocoupler.

#### Common-Mode Rejection & LED Driver Circuits

With the combination of a high-efficiency AlGaAs LED and a high-gain amplifier in the HCPL-47XX optocoupler, a few circuit techniques can enhance the common-mode rejection (CMR) of

this optocoupler. First, use good high-frequency circuit layout practices to minimize coupling of common-mode signals between input and output circuits. Keep input traces away from output traces to minimize capacitive coupling of interference between input and output sections. If possible, parallel, or shunt switch the LED current as shown in Figure 13, rather than series switch the LED current as illustrated in Figure 15. Not only will CMR be enhanced with these circuits (Figures 13 and 14), but the switching speed of the optocoupler will be improved as well. This is because in the parallel switched case the LED current is current-steered into or away from the LED, rather than being fully turned off as in the series switched case. Figure 13 illustrates this type of circuit. The Schottky diode helps quickly to discharge and pre-bias the LED in the off state. If a common-mode voltage across the optocoupler suddenly attempts to inject a current into the off LED anode, the Schottky diode would divert the interfering current to ground. The combination of the Schottky diode forward voltage and the  $V_{OL}$  saturation voltage of the driver output stage (on-condition) will keep the LED voltage at or below 0.8 V. This will prevent the LED (off-condition) from conducting any significant forward current that might cause the HCPL-47XX to turn on. Also, if the driver stage is an active totem-pole output, the Schottky diode allows the active output pull-up section to disconnect from the LED and pull high.

As shown in Figure 14, most active output driver integrated circuits can source directly the forward current needed to operate the LED of the HCPL-47XX optocoupler. The advantage of using the silicon diode in this circuit is to conduct charge out of

the LED quickly when the LED is turned off. Upon turn-on of the LED, the silicon diode capacitance will provide a rapid charging path (peaking current) for the LED. In addition, this silicon diode prevents common-mode current from entering the LED anode when the driver IC is on and no operating LED current exists.

In general, series switching the low input current of the HCPL-47XX LED is not recommended. This is particularly valid when in a high common-mode interference environment. However, if series switching of the LED current must be done, use an additional pull-up resistor from the cathode of the LED to the input  $V_{CC}$  as shown in Figure 15. This helps minimize any differential-mode current from conducting in the LED while the LED is off, due to a common-mode signal occurring on the input  $V_{CC}$  (anode) of the LED. The common-mode signal coupling to the anode and cathode could be slightly different. This could potentially create a LED current to flow that would rival the normal, low input current needed to operate the optocoupler. This additional parallel resistor can help shunt any leakage current around the LED should the drive circuit, in the off state, have any significant leakage current on the order of 40  $\mu\text{A}$ . With the use of this parallel resistor, the total drive current conducted when the LED is on is the sum of the parallel resistor and LED currents. In the series circuit of Figure 15 with the LED off, if a common-mode voltage were to couple to the LED cathode, there can be enough imbalance of common-mode voltage across the LED to cause a LED current to flow and, inadvertently, turn on the optocoupler. This series, switching circuit has no protection against a negative-transition, input common-mode signal.

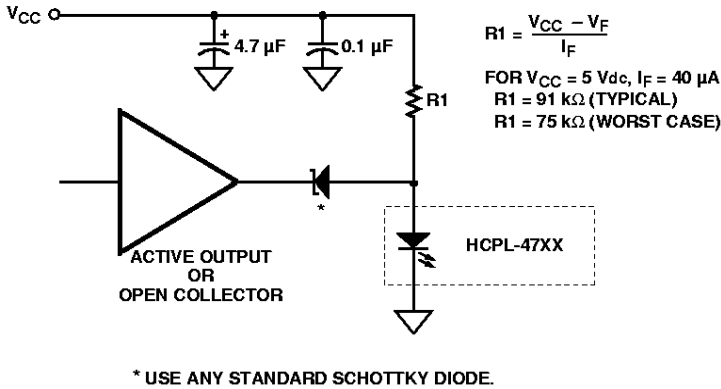


Figure 13. Recommended Parallel LED Driver Circuit for HCPL-4701/-4731.

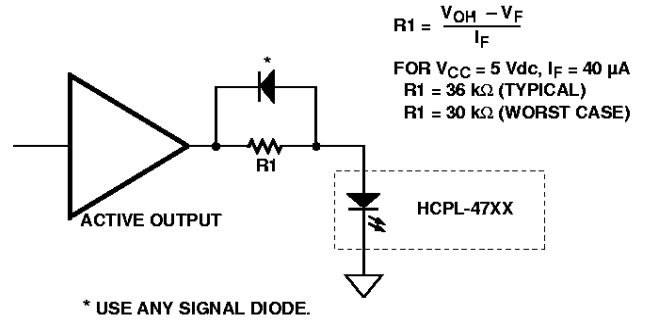


Figure 14. Recommended Alternative LED Driver Circuit for HCPL-4701/-4731 .

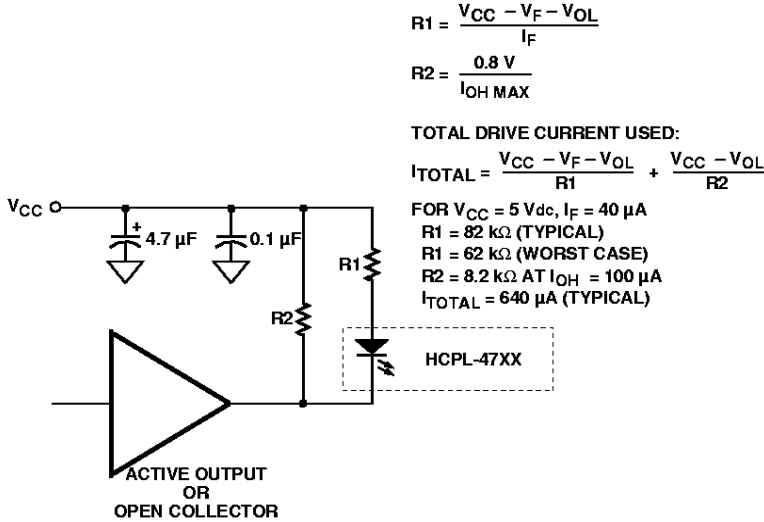


Figure 15. Series LED Driver Circuit for HCPL-4701/-4731.

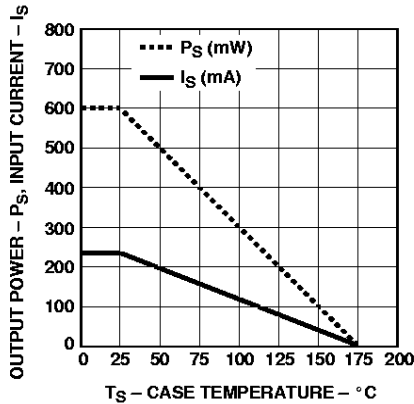


Figure 16. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

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