IS42G32256

256K x 32 x 2 (16-Mbit) SYNCHRONOUS GRAPHICS RAM

ADVANCE INFORMATION
APRIL 1998

FEATURES

- Operating frequency: 125 MHz
- 256,144 words x 32 bits x 2-bank organization
- Dual internal bank control
- Single 3.3V ± 3V power supply
- Synchronous interface
  - Pulsed interface
  - Auto and controlled precharge command
  - Pin-pong memory bank operation
- Random column address
- Programmable mode register
  - Burst length (1, 2, 4, 8, and full page)
  - CAS latency (1, 2, and 3)
  - Wrap type: Sequential and Interleave
- Programmable special register
  - Graphic cycles
- Eight column Block Write (BW) function
- Byte Control: read and write cycles
- Write-Per-Bit (WPB) function
- Burst stop command: Full page
- Precharge burst termination
- Power down and clock suspend operations
- Refresh capability
  - Auto, self-refresh
- 2,048 refresh cycles/32 ms
- LVTTL compatible inputs and outputs
- 100-pin plastic TQFP (14mm x 20mm)

KEY TIMING PARAMETERS

Symbol	Parameter	-8	-10	Units
t_{DS}	Input Data Setup Time	2.5	3	ns
t_{DH}	Input Data Hold Time	1	1	ns
t_{RAS}	Command Period (ACT to PRE)	48	50	ns
t_{CK}	Clock Cycle Time	8	10	ns
—	Operating Frequency	125	100	MHz

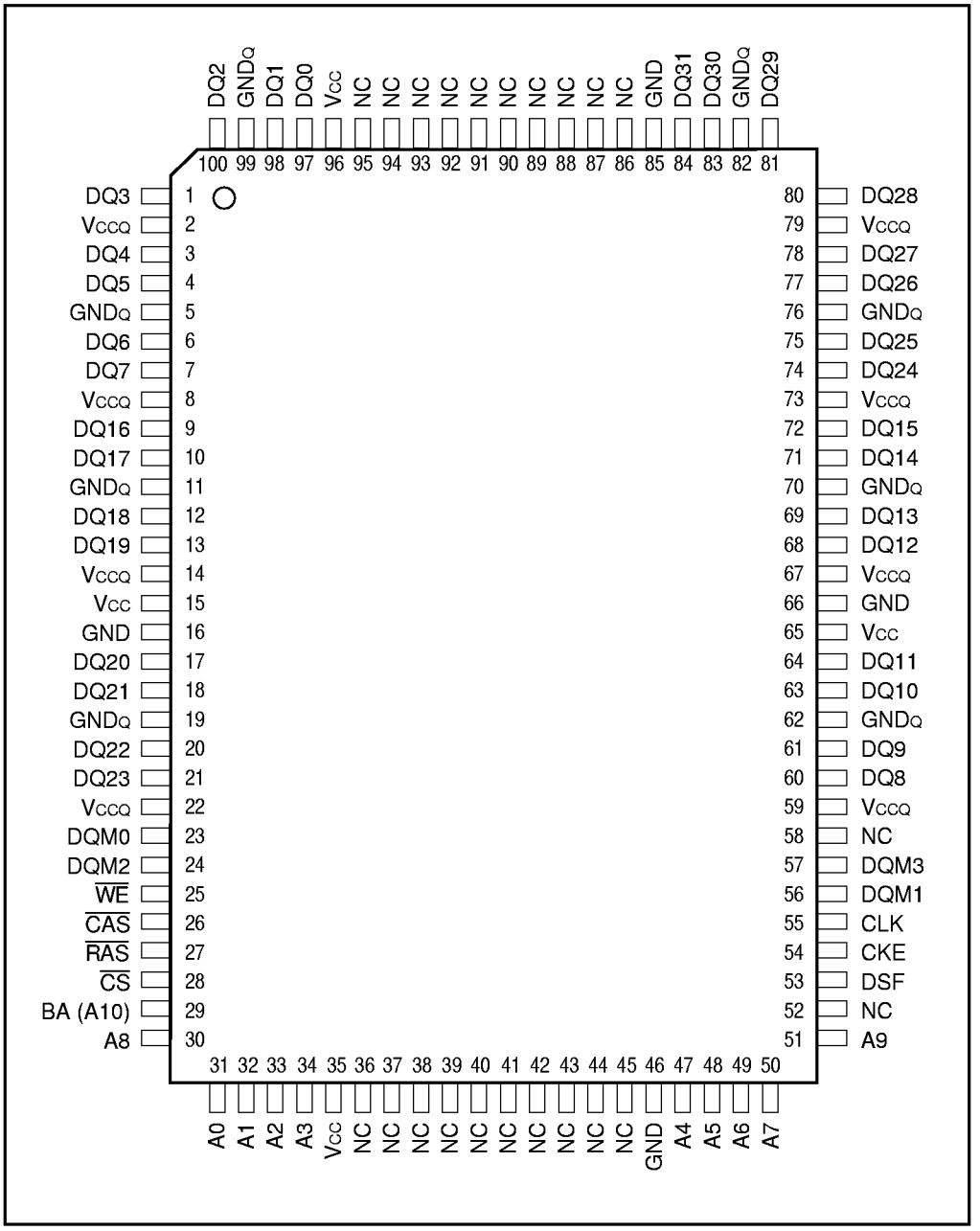
DESCRIPTION

The ISSI IS42G32256 is a high-speed 16-Mbit CMOS Synchronous Graphics RAM organized as 256K words x 32 bits x 2 banks. With SGRAM, all input and output signals are synchronized with the rising edge of the system clock. Programmable Mode Register and Special Registers provide a choice of Read or Write burst lengths of 1, 2, 4 or 8 locations or a Full Page with burst termination options. The SGRAM performance is enhanced with the Write-per-bit (WPB) and eight columns of Block Write functions.

The IS42G32256 is ideal for high-performance, high-bandwidth applications including workstation graphics, set top box, games, and PC-2D/3D graphic applications.

PIN CONFIGURATION

100-Pin PQFP



PIN DESCRIPTIONS

Symbol	Pin Number	I/O	Name and Function
A0-A9	30-34, 47-51	I	**Address:** Row/Column addresses are multiplexed on the same pins. Row address: RA0-RA9 Column address: CA0-CA7
A10	29	I	**Bank Select Address:** Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{CAS}$	26	I	**Column Address Strobe:** Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
CKE	54	I	**Clock Enable:** Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + t_{CKS} prior to new command. Disable input buffers for power down in standby.
CLK	55	I	**System Clock:** Active on the positive going edge to sample all inputs.
$\overline{CS}$	28	I	**Chip Select:** Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQMx.
DQ0-DQ31	1, 3-4, 6-7, 9-10, 12-13, 17-18, 20-21, 60-61, 63-64, 68-69, 71-72, 74-75, 77-78, 81-81, 83-84, 97-98, 100	I/O	**Data Input/Output:** Data Inputs/Outputs are multiplexed on the same pins.
DQM0-DQM3	23-24, 56-57	I/O	**Data Input/Output Mask:** Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DSF	53		**Define Special Function:** Enables write per bit, block write and special mode register set.
$\overline{RAS}$	27	I	**Row Address Strobe:** Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access and precharge.
$\overline{WE}$	25	I	**Write Enable:** Enables write operation and row precharge.
V_{CCQ}	2, 8, 14, 22, 59, 67, 73, 76, 79		Supplies voltage for data output
Vcc	15, 35, 65, 96		Power Supply Voltage
GND_Q	5, 11, 19, 62, 70, 82, 99		Ground for D_Q
GND	16, 46, 66, 85		Ground
NC	36-45, 52, 58, 86-95		No connect

TRUTH TABLE

Function	CKEn-1	CKEn	CS	RAS	CAS	WE	DSF	DQM	A10	A9	A8-A0
Mode Register Set[2,3]	H	X	L	L	L	L	L	X	OP CODE		
Special Mode Register Set[2,3,8]	H	X	L	L	L	L	H	X	OP CODE		
Auto Refresh[4]	H	H	L	L	L	H	L	X	X	X	X
Self Refresh, Entry[4]	H	L	L	L	L	H	L	X	X	X	X
Self Refresh, Exit[4]	L	H	L	H	H	H	X	X	X	X	X
	L	H	H	X	X	X	X	X	X	X	X
Bank Active/Row Address Write Per Bit Disable[5,6]	H	X	L	L	H	H	L	X	V		Row Address
Bank Active/Row Address Write Per Bit Enable[5,6,10]	H	X	L	L	H	H	H	X	V		Row Address
Read and Column Address Auto Precharge Disable[5]	H	X	L	H	L	H	L	X	V	L	Column Address
Read and Column Address Auto Precharge Enable[5,6]	H	X	L	H	L	H	L	X	V	H	Column Address
Write and Column Address Auto Precharge Disable[5,6]	H	X	L	H	L	H	L	X	V	L	Column Address
Write and Column Address Auto Precharge Enable[5,6,7,10]	H	X	L	H	L	H	L	X	V	H	Column Address
Block Write and Column Address Auto Precharge Disable[5,6]	H	X	L	H	L	H	L	X	V	L	Column Address
Block Write and Column Address Auto Precharge Enable[5,6,7,10]	H	X	L	H	L	H	L	X	V	H	Column Address
Burst Stop[8]	H	X	L	H	H	L	L	X	X	X	X
Precharge Bank Selection	H	X	L	L	H	L	L	X	V	L	X
Precharge Both Banks	H	X	L	L	H	L	L	X	X	H	X
Clock Suspend or	H	L	L	H	H	H	X	X	X	X	X
Active Power Down Entry	H	L	H	X	X	X	X	X	X	X	X
Clock Suspend or Active Power Down Exit	L	H	X	X	X	X	X	X	X	X	X
Precharge Pover Down Mode Entry	H	L	L	H	H	H	X	X	X	X	X
	H	L	H	X	X	X	X	X	X	X	X
Precharge Pover Down Mode Exit	L	H	L	V	V	V	V	X	X	X	X
	L	H	H	X	X	X	X	X	X	X	X
DQM[9]	H	X	X	X	X	X	X	V	X	X	X
No Operation Command	H	X	L	H	H	H	X	X	X	X	X
	H	X	H	X	X	X	X	X	X	X	X

Notes:

1. V=Valid, X=Don't Care, H=Logic High, L=Logic Low
2. OP Code : Operand Code; A0 ~ A10 : Program keys. (@MRS); A5, A6 : LMR or LCR select. (@SMRS) Color register exists only one per DQi which both banks share. So does Mask Register. Color or mask is loaded into chip through DQ pin.
3. MRS can be issued only at both banks precharge state. SMRS can be issued only if DQ's are idle. A new command can be issued at the next clock of MRS/SMRS.
4. Auto refresh functions as same as CBR refresh of DRAM. The automatical precharge without Row precharge command is meant by "Auto". Auto/Self refresh can be issued only at both precharge state.
5. A10 : Bank select address. If "Low" at read, (block) write, Row active and precharge, bank A is selected. If "High" at read, (block) write, Row active and precharge, Bank B is selected. If A9 is "High" at Row precharge, A10 is ignored and both banks are precharged.
6. It is determined at Row active cycle whether Normal/Block write operates in write per bit mode or not. For A bank write, at A bank Row active, for B bank write, at B bank Row active. Terminology : Write per bit = I/O mask. (Block) Write with write per bit mode = Masked (Block) Write.
7. During burst read or write with auto precharge, new read/(blodk) write command cannot be issued. Another bank read/(block) write command can be issued at t_{RP} after the end of burst.
8. Burst stop command is valid only at full page burst length.
9. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0) but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)
10. Graphic features added to SDRAM's original features. If SDF is tied to low, graphic functions are disabled and chip operates as a 16M SDRAM with 32 DQ's.

SGRAM vs SDRAM

SDRAM Function	MRS		Bank Active		Write	
DSF	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active with Write per bit Disable	Bank Active with Write per bit Enable	Normal Write	Block Write

Notes:
1. If DSF is low, SGRAM functionality is identical to SDRAM functionality.
2. SGRAM can be used as a unified memory by the appropriate DSF control; SGRAM = Graphic Memory + Main Memory.

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A10	A9	A8, A7	A6, A5, A4	A3	A2, A1, A0
Function	RFU(1)	W.B.L.(2)	TM	CAS Latency	BT	Burst Length

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor	0	0	1	1	1	Interleave	0	0	1	2	Reserved
1	0	Use	0	1	0	2			0	1	0	4	4
1	1	Only	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	256(Full)(3)	Reserved

Special mode Register Programmed with SMRS

Address	A10, A9, A8, A7	A6	A5	A4, A3, A2, A1, A0
Function	X	LC(4)	LM(4)	X

Load Color		Load Mask	
A6	Function	A5	Function
0	Disable	0	Disable
1	Enable	1	Enable

Notes:
1. RFU (Reserved for Future Use) should stay "0" during MRS cycle.
2. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
3. The full column burst (256-bit) is available only at Sequential mode of burst type.
4. If LC and LM both high (1), data of mask and color register will be unknown.

POWER UP SEQUENCE

1. Apply power and start clock, attempt to maintain DKE = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200 µs.
3. Issue precharge commands for all banks of the devices.
4. Issue two or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Sequence of 4 and 5 may be changed.

   The device is now ready for normal operation.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
$V_{CC\ MAX}$	Maximum Supply Voltage	–1.0 to +4.6	V
$V_{CCQ\ MAX}$	Maximum Supply Voltage for Output Buffer	–1.0 to +4.6	V
V_{IN}	Input Voltage	–1.0 to +4.6	V
V_{OUT}	Output Voltage	–1.0 to +4.6	V
$P_{D\ MAX}$	Allowable Power Dissipation	1	W
I_{CS}	Output Shorted Current	50	mA
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +150	°C

DC RECOMMENDED OPERATING CONDITIONS

At T_A = 0 to +70°C(2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}, V_{CCQ}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	—	Vcc + 0.3	V
V_{IL}	Input Low Voltage	–0.3	—	+0.8	V

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to GND.
3. V_{IH} (max) = 5.5V for pulse width ≤ 5 ns.
4. V_{IL} (min) = –1.0V for pulse width ≤ 5 ns.

CAPACITANCE CHARACTERISTICS

At T_A = 0 to +25°C, Vcc = V_{CCQ} = 3.3 ± 0.3V, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Input Capacitance: A0-A10	—	4	pF
C_{IN2}	Input Capacitance: (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM0-3)	—	4	pF
CI/O	Data Input/Output Capacitance: I/O0 ~ I/O31	—	5	pF

DC ELECTRICAL CHARACTERISTICS

(Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition		Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}, with pins other than the tested pin at 0V			–10	10	µA
I_{OL}	Output Leakage Current	Output is disabled 0V ≤ V_{OUT} ≤ V_{CC}			–10	10	µA
V_{OH}	Output High Voltage Level	I_{OUT} = –2 mA			2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OUT} = +2 mA			—	0.4	V
I_{CC1}	Operating Current[1,2]	One Bank Operation, Burst Length=1		-8	—	180	mA
		tRC ≥ tRC (min.), I_{OUT} = 0mA		-10	—	170	mA
I_{CC2P}	Precharge Standby Current	CKE ≤ V_{IL} (MAX)	t_{CK} = t_{CK} (MIN)	—	—	3	mA
I_{CC2PS}	(In Power-Down Mode)		t_{CK} = ∞	—	—	2	mA
I_{CC2N}	Precharge Standby Current	CKE ≥ V_{IH} (MIN)	t_{CK} = t_{CK} (MIN)	—	—	30	mA
I_{CC2NS}	(In Non Power-Down Mode)		t_{CK} = ∞	—	—	15	mA
I_{CC3P}	Active Standby Current	CKE ≤ V_{IL} (MAX)	t_{CK} = t_{CK} (MIN)	—	—	3	mA
I_{CC3PS}	(In Power-Down Mode)		t_{CK} = ∞	—	—	2	mA
I_{CC3N}	Active Standby Current	CKE ≥ V_{IH} (MIN)	t_{CK} = t_{CK} (MIN)	—	—	50	mA
I_{CC3NS}	(In Non Power-Down Mode)		t_{CK} = ∞	—	—	30	mA
I_{CC4}	Operating Current	t_{CK} = t_{CK} (MIN)	$\overline{CAS}$ latency = 3	-8	—	250	mA
	(In Burst Mode)[1]	I_{OUT} = 0mA		-10	—	210	mA
			$\overline{CAS}$ latency = 2	-8	—	150	mA
				-10	—	140	mA
			$\overline{CAS}$ latency = 1	-8	—	75	mA
				-10	—	70	mA
I_{CC5}	Auto-Refresh Current	t_{RC} = t_{RC} (MIN)		-8	—	150	mA
				-10	—	140	mA
I_{CC6}	Self-Refresh Current	CKE ≤ 0.2V		—	—	2	mA
I_{CC7}	Operating Current	t_{RC} ≥ t_{RC} (MIN)	I_{OL} = 0 mA, t_{BWC} (MIN)	-8	—	180	mA
	(one Bank Block Write)			-10	—	170	mA

Notes:

1. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between Vcc and GND for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.
2. Icc1 and Icc4 depend on the output load. The maximum values for Icc1 and Icc4 are obtained with the output open state.

AC CHARACTERISTICS[1,2,3]

Symbol	Parameter		-8 Min.	-8 Max.	-10 Min.	-10 Max.	Units
$t_{CK}3$	Clock Cycle Time	$\overline{CAS}$ Latency = 3	8	—	10	—	ns
$t_{CK}2$		$\overline{CAS}$ Latency = 2	12	—	15	—	ns
$t_{CK}1$		$\overline{CAS}$ Latency = 1	24	—	30	—	ns
$t_{AC}3$	Access Time From CLK[4]	$\overline{CAS}$ Latency = 3	—	6.5	—	8	ns
$t_{AC}2$		$\overline{CAS}$ Latency = 2	—	8	—	13	ns
$t_{AC}1$		$\overline{CAS}$ Latency = 1	—	22	—	28	ns
t_{CHI}	CLK HIGH Level Width		3	—	3.5	—	ns
t_{CL}	CLK LOW Level Width		3	—	3.5	—	ns
$t_{OH}3$	Output Data Hold Time	$\overline{CAS}$ Latency = 3	3	—	3	—	ns
$t_{OH}2$		$\overline{CAS}$ Latency = 2	3	—	3	—	ns
$t_{OH}1$		$\overline{CAS}$ Latency = 1	3	—	3	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	ns
$t_{HZ}3$	Output HIGH Impedance Time[5]	$\overline{CAS}$ Latency = 3	4	8	4	10	ns
$t_{HZ}2$		$\overline{CAS}$ Latency = 2	4	12	4	14	ns
$t_{HZ}1$		$\overline{CAS}$ Latency = 1	4	27	4	27	ns
t_{DS}	Input Data Setup Time		2.5	—	3	—	ns
t_{DH}	Input Data Hold Time		1	—	1	—	ns
t_{AS}	Address Setup Time		2.5	—	3	—	ns
t_{AH}	Address Hold Time		1	—	1	—	ns
t_{CKS}	CKE Setup Time		2.5	—	3	—	ns
t_{CKH}	CKE Hold Time		1	—	1	—	ns
t_{CKA}	CKE to CLK Recovery Delay Time		1CLK+3	—	1CLK+3	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, DSF)		2.5	—	3	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, DSF)		1	—	1	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		72	—	90	—	ns
t_{RAS}	Command Period (ACT to PRE)		48	12,000	50	12,000	ns
t_{RP}	Command Period (PRE to ACT)		24	—	30	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		24	—	30	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		16	—	20	—	ns
$t_{DPL}3$	Last Data In To Precharge	$\overline{CAS}$ Latency = 3	1CLK+16	—	1CLK+20	—	ns
		Command Delay time					
$t_{DPL}2$		$\overline{CAS}$ Latency = 2	16	—	20	—	ns
$t_{DPL}1$		$\overline{CAS}$ Latency = 1	16	—	20	—	ns
$t_{DAL}3$	Last Data In To Active / Refresh	$\overline{CAS}$ Latency = 3	40	—	50	—	ns
	Command Delay time (Auto-Precharge, same bank)						
$t_{DAL}2$		$\overline{CAS}$ Latency = 2	40	—	50	—	ns
$t_{DAL}1$		$\overline{CAS}$ Latency = 1	40	—	50	—	ns
t_{BDPL}	Block Write to Precharge Command Delay Time		24	—	30	—	ns
t_{BWC}	Block Write Cycle Time		16	—	20	—	ns
t_{MCD}	Mode Register Set to Command Delay Time		8	—	10	—	ns
t_{SMCD}	Special Moderegister Set to Command Delay Time		8	—	10	—	ns
t_T	Transition Time		1	30	1	30	ns
t_{REF}	Refresh Cycle Time		—	32	—	32	ns

Notes:

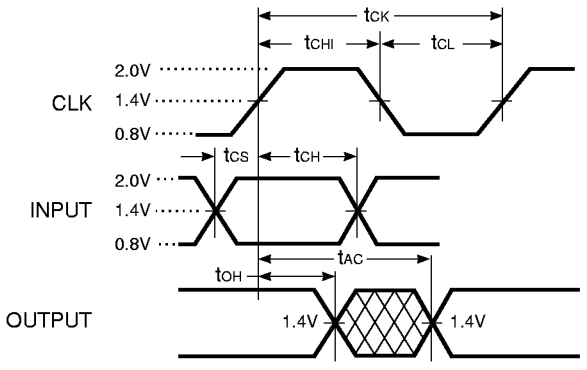
1. When power is first applied, memory operation should be started 100 µs after Vcc and VccQ reach their stipulated voltages. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns.
3. The reference level is 1.4 V when measuring input signal timing. Rise and fall times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Access time is measured at 1.4V with the load shown in the figure below.
5. The time t_{HZ} (max.) is defined as the time required for the output voltage to transition by ± 200 mV from V_{OH} (min.) or V_{OL} (max.) when the output is in the high impedance state.

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

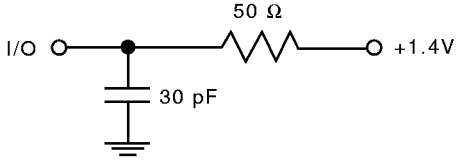
Symbol	Parameter	-8			-10			Units
CL		3	2	1	3	2	1	
t_{CK}	Clock Cycle Time	8	12	24	10	15	30	ns
—	Operating Frequency	125	83	41	100	66	33	MHz
t_{CAC}	$\overline{CAS}$ Latency	3	2	1	3	2	1	cycle
t_{RCD}	Active Command to Read/Write Command Delay Time	3	2	1	3	2	1	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC})	6	4	2	6	4	2	cycle
t_{RC}	Command Period (REF to REF/ACT to ACT)	9	6	3	9	6	3	cycle
t_{RAS}	Command Period (ACT to PRE)	6	4	2	6	4	2	cycle
t_{RP}	Command Period (PRE to ACT)	3	2	1	3	2	1	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])	2	2	1	2	2	1	cycle
t_{CCD}	Column Command Delay Time (READ, READA, WRIT, WRITA)	1	1	1	1	1	1	cycle
t_{DPL}	Last Data In to Precharge Command Delay Time	2	2	1	2	2	1	cycle
t_{DAL}	Last Data In to Active/Refresh Command Delay Time (Auto-Precharge, Same Bank)	5	4	2	5	4	2	cycle
t_{RBD}	Burst Stop Command to Output in HIGH-Z Delay Time (Read)	3	2	1	3	2	1	cycle
t_{WBD}	Burst Stop Command to Input in Invalid Delay Time (Write)	0	0	0	0	0	0	cycle
t_{RQL}	Precharge Command to Output in HIGH-Z Delay Time (Read)	3	2	1	3	2	1	cycle
t_{WDL}	Precharge Command to Input in Invalid Delay Time (Write)	0	0	0	0	0	0	cycle
t_{BDAL}	Block Write to Active Command (Auto Precharge, Same Bank)	6	5	3	6	5	3	cycle
t_{EP}	Last Data Out to Precharge Command	–2	–1	0	–2	–1	0	cycle
t_{SMCD}	Special Mode Register Set to Command	1	1	1	1	1	1	cycle
t_{RR}	Register Set Command to Register Set Command	2	2	2	2	2	2	cycle
t_{PQL}	Last Output to Auto-Precharge Start Time (Read)	–2	–1	0	–2	–1	0	cycle
t_{QMD}	DQM to Output Delay Time (Read)	2	2	2	2	2	2	cycle
t_{DMD}	DQM to Input Delay Time (Write)	0	0	0	0	0	0	cycle
t_{MCD}	Mode Register Set to Command Delay Time	1	1	1	1	1	1	cycle

AC TEST CONDITIONS (Input/Output Reference Level: 1.4V)

Input



Output Load



ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Frequency	Speed (ns) Cycle Time	Order Part No.	Package
125 MHz	- 8	IS42G32256-8TQ	TQFP
100 MHz	-10	IS42G32256-10TQ	TQFP

Integrated Silicon Solution, Inc.
2231 Lawson Lane
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Toll Free: 1-800-379-4774
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