

National Semiconductor is now part of
Texas Instruments.

Search <http://www.ti.com/> for the latest technical
information and details on our current products and services.

LMC6484 CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

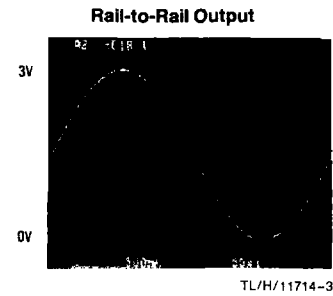
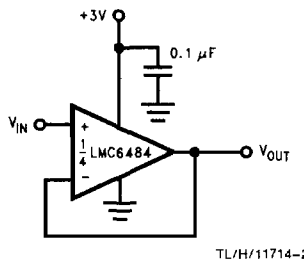
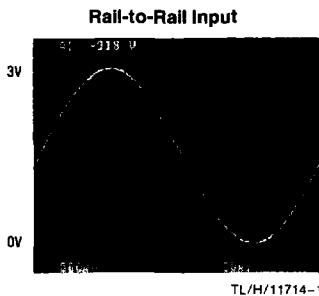
Features (Typical unless otherwise noted)

- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR 82 dB
- Ultra Low Input Current 20 fA
- High Voltage Gain ($R_L = 500\text{ k}\Omega$) 130 dB
- Specified for 2 kΩ and 600Ω loads

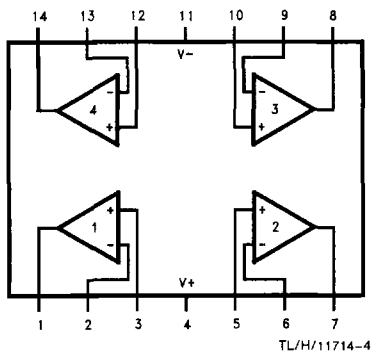
Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

3V Single Supply Buffer Circuit



Connection Diagram



Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military -55°C to +125°C	Industrial -40°C to +85°C		
14-pin Molded DIP	LMC6484MN	LMC6484AIN LMC6484IN	N14A	Rail
		LMC6484AIM LMC6484IM	M14A	Rail Tape and Reel
14-pin Ceramic DIP	LMC6484AMJ/883		J14A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.0 kV
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V ⁺) + 0.3V, (V ⁻) - 0.3V
Supply Voltage (V ⁺ - V ⁻)	16V
Current at Input Pin (Note 12)	± 5 mA
Current at Output Pin (Notes 3, 8)	± 30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C

Storage Temperature Range	-65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	3.0V ≤ V ⁺ ≤ 15.5V
Junction Temperature Range	
LMC6484AM	-55°C ≤ T _J ≤ +125°C
LMC6484AI, LMC6484I	-40°C ≤ T _J ≤ +85°C
Thermal Resistance (θ _{JA})	
N Package, 14-Pin Molded DIP	70°C/W
M Package, 14-Pin Surface Mount	110°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V⁺ = 5V, V⁻ = 0V, V_{CM} = V_O = V⁺/2 and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units	
V _{OS}	Input Offset Voltage		0.110	0.750 1.35	3.0 3.7	3.0 3.8	mV max	
TCV _{OS}	Input Offset Voltage Average Drift		1.0				μV/°C	
I _B	Input Current	(Note 13)	0.02	4.0	4.0	100	pA max	
I _{OS}	Input Offset Current	(Note 13)	0.01	2.0	2.0	50	pA max	
C _{IN}	Common-Mode Input Capacitance		3				pF	
R _{IN}	Input Resistance		> 10				Tera Ω	
CMRR	Common Mode Rejection Ratio	0V ≤ V _{CM} ≤ 15.0V, V ⁺ = 15V	82	70 67	65 62	65 60	dB min	
		0V ≤ V _{CM} ≤ 5.0V, V ⁺ = 5V	82	70 67	65 62	65 60		
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V ⁺ ≤ 15V, V ⁻ = 0V, V _O = 2.5V	82	70 67	65 62	65 60	dB min	
-PSRR	Negative Power Supply Rejection Ratio	-5V ≤ V ⁻ ≤ -15V, V ⁺ = 0V, V _O = -2.5V	82	70 67	65 62	65 60	dB min	
V _{CM}	Input Common-Mode Voltage Range	V ⁺ = 5V and 15V For CMRR ≥ 50 dB	V ⁻ - 0.3	-0.25 0	-0.25 0	-0.25 0	V max	
			V ⁺ + 0.3	V ⁺ + 0.25 V⁺	V ⁺ + 0.25 V⁺	V ⁺ + 0.25 V⁺	V min	
A _V	Large Signal Voltage Gain	R _L = 2kΩ (Notes 7, 13)	Sourcing	666	140 84	120 72	120 60	V/mV min
			Sinking	75	35 20	35 20	35 18	V/mV min
		R _L = 600Ω (Notes 7, 13)	Sourcing	300	80 48	50 30	50 25	V/mV min
			Sinking	35	20 13	15 10	15 8	V/mV min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+ / 2$ and $R_L > 1\text{M}$.

Boldface limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_O	Output Swing	$V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+ / 2$	4.9	4.8 4.7	4.8 4.7	4.8 4.7	V min
			0.1	0.18 0.24	0.18 0.24	0.18 0.24	V max
		$V^+ = 5\text{V}$ $R_L = 600\Omega$ to $V^+ / 2$	4.7	4.5 4.24	4.5 4.24	4.5 4.24	V min
			0.3	0.5 0.65	0.5 0.65	0.5 0.65	V max
		$V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+ / 2$	14.7	14.4 14.2	14.4 14.2	14.4 14.2	V min
			0.16	0.32 0.45	0.32 0.45	0.32 0.45	V max
	$V^+ = 15\text{V}$ $R_L = 600\Omega$ to $V^+ / 2$	14.1	13.4 13.0	13.4 13.0	13.4 13.0	V min	
		0.5	1.0 1.3	1.0 1.3	1.0 1.3	V max	
I_{SC}	Output Short Circuit Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	20	16 12	16 12	16 10	mA min
		Sinking, $V_O = 5\text{V}$	15	11 9.5	11 9.5	11 8.0	mA min
I_{SC}	Output Short Circuit Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	30	28 22	28 22	28 20	mA min
		Sinking, $V_O = 12\text{V}$ (Note 8)	30	30 24	30 24	30 22	mA min
I_S	Supply Current	All Four Amplifiers $V^+ = +5\text{V}$, $V_O = V^+ / 2$	2.0	2.8 3.6	2.8 3.6	2.8 3.8	mA max
		All Four Amplifiers $V^+ = +15\text{V}$, $V_O = V^+ / 2$	2.6	3.0 3.8	3.0 3.8	3.0 4.0	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+ / 2$ and $R_L > 1\text{M}$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484A Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 0.7	0.9 0.63	0.9 0.54	V/ μs min
GBW	Gain-Bandwidth Product	$V^+ = 15\text{V}$	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	$f = 1\text{ kHz}$ $V_{\text{CM}} = 1\text{V}$	37				nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.03				pA/ $\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	$f = 1\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 4.1\text{ V}_{\text{PP}}$	0.01				%
		$f = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 8.5\text{ V}_{\text{PP}}$ $V^+ = 10\text{V}$	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+ / 2$ and $R_L > 1\text{M}$

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 2.7	3.0 3.7	3.0 3.8	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 3\text{V}$	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	$3\text{V} \leq V^+ \leq 15\text{V}$, $V^- = 0\text{V}$	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	$V^- - 0.25$	0	0	0	V max
			$V^+ + 0.25$	V^+	V^+	V^+	V min
V_O	Output Swing	$R_L = 2\text{ k}\Omega$ to $V^+ / 2$	2.8				V
			0.2				V
		$R_L = 600\Omega$ to $V^+ / 2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	All Four Amplifiers	1.65	2.5 3.0	2.5 3.0	2.5 3.2	mA max

AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+ / 2$ and $R_L > 1\text{M}$

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/ μs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	$f = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 2\text{ V}_{\text{PP}}$	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{\text{J(max)}}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{\text{J(max)}} - T_A) / \theta_{\text{JA}}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{\text{CM}} = 7.5\text{V}$ and R_L connected to 7.5V. For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $3.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: Do not short circuit output to V^- , when V^- is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{\text{PP}}$.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

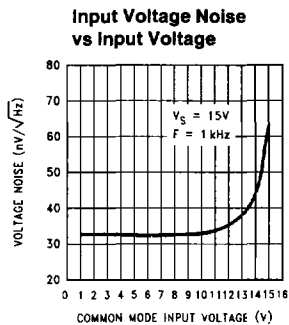
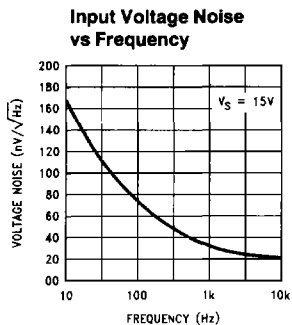
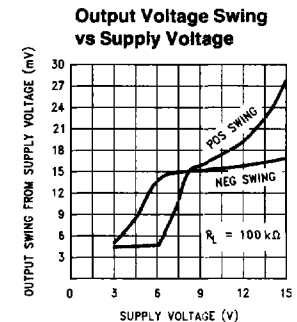
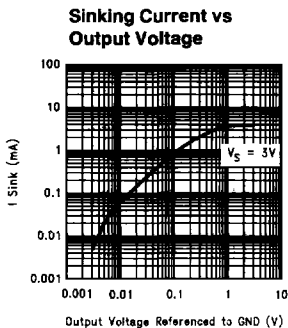
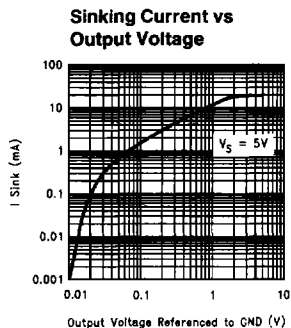
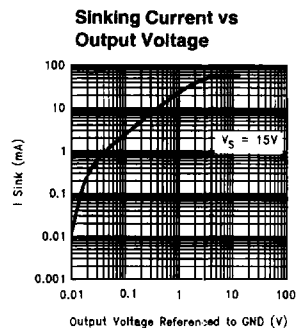
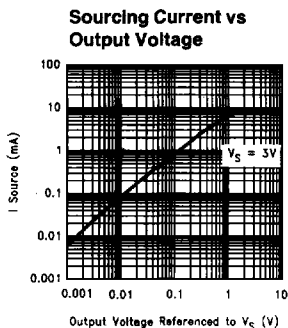
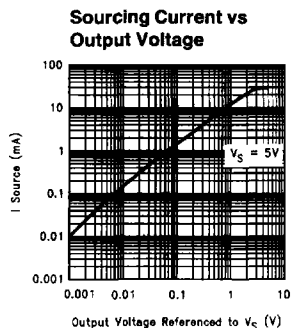
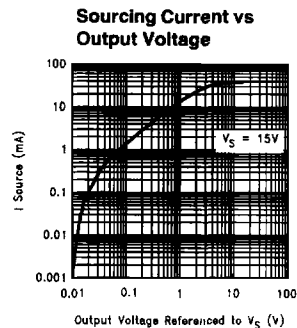
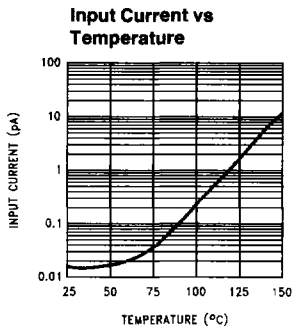
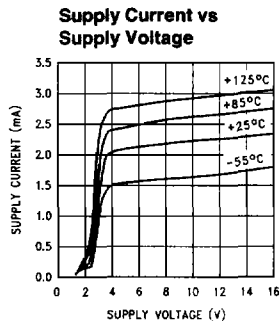
Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6484X.

Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

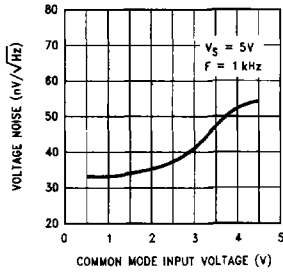


TL/H/11714-5

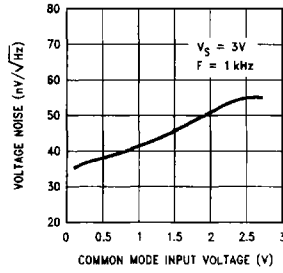
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

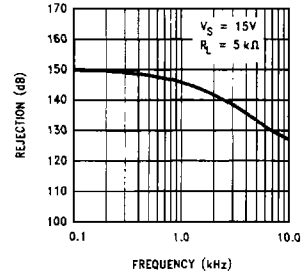
Input Voltage Noise vs Input Voltage



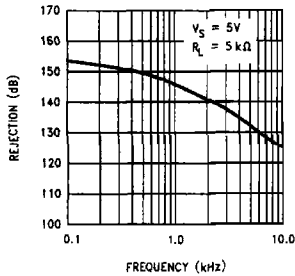
Input Voltage Noise vs Input Voltage



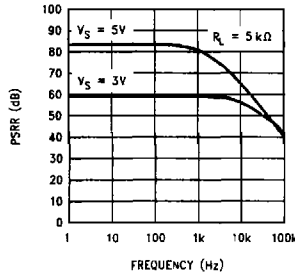
Crosstalk Rejection vs Frequency



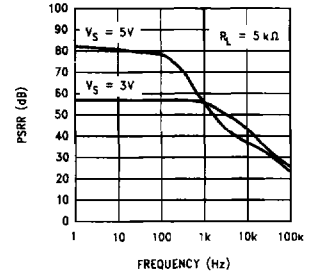
Crosstalk Rejection vs Frequency



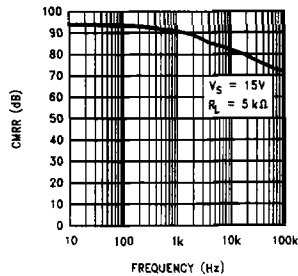
Positive PSRR vs Frequency



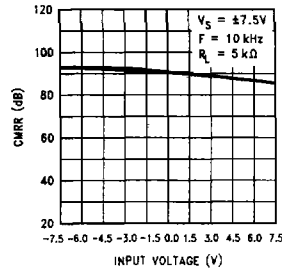
Negative PSRR vs Frequency



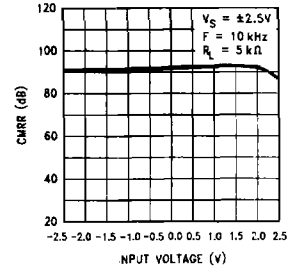
CMRR vs Frequency



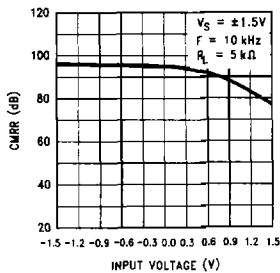
CMRR vs Input Voltage



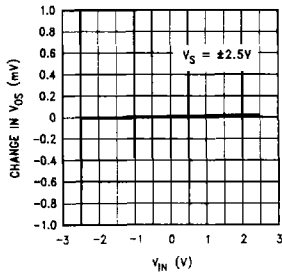
CMRR vs Input Voltage



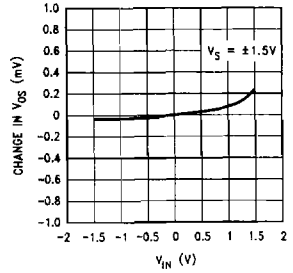
CMRR vs Input Voltage



ΔVOS vs CMR



ΔVOS vs CMR

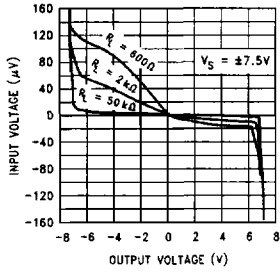


TL/H/11714-6

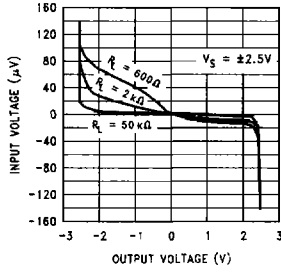
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

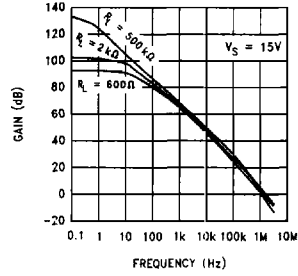
Input Voltage vs Output Voltage



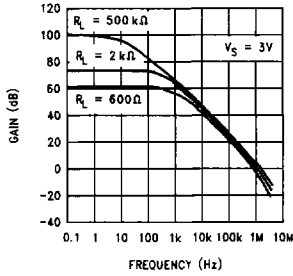
Input Voltage vs Output Voltage



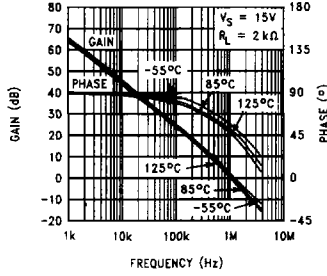
Open Loop Frequency Response



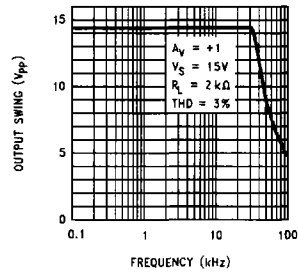
Open Loop Frequency Response



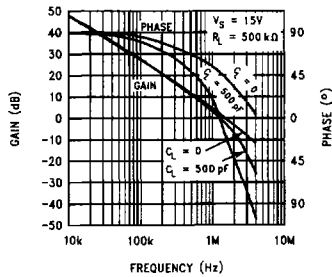
Open Loop Frequency Response vs Temperature



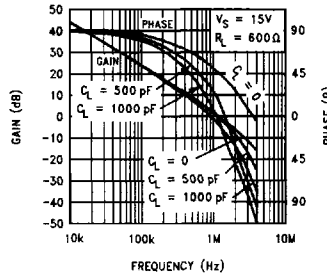
Maximum Output Swing vs Frequency



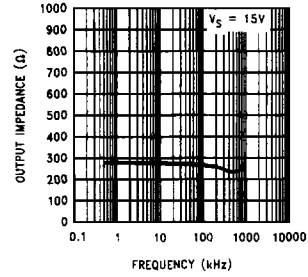
Gain and Phase vs Capacitive Load



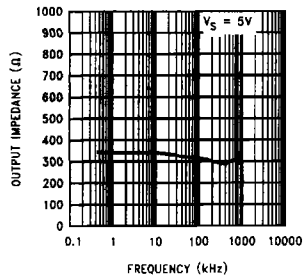
Gain and Phase vs Capacitive Load



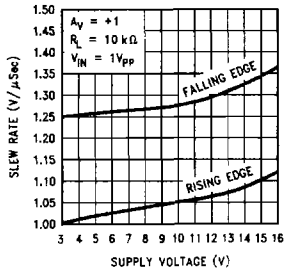
Open Loop Output Impedance vs Frequency



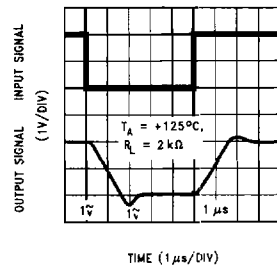
Open Loop Output Impedance vs Frequency



Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response

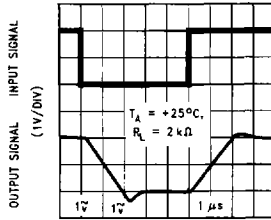


TL/H/11714-7

Typical Performance Characteristics

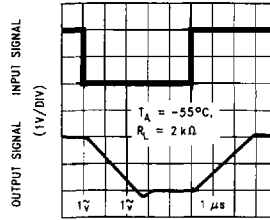
$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Non-Inverting Large Signal Pulse Response



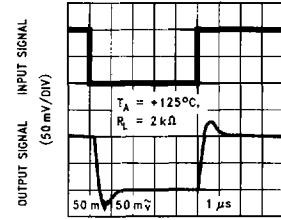
TIME (1 μs /DIV)

Non-Inverting Large Signal Pulse Response



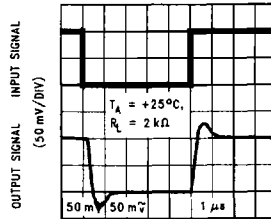
TIME (1 μs /DIV)

Non-Inverting Small Signal Pulse Response



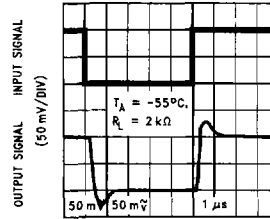
TIME (1 μs /DIV)

Non-Inverting Small Signal Pulse Response



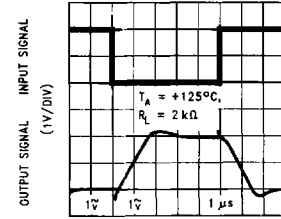
TIME (1 μs /DIV)

Non-Inverting Small Signal Pulse Response



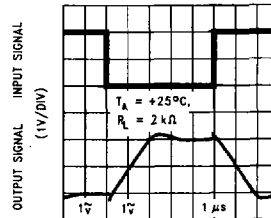
TIME (1 μs /DIV)

Inverting Large Signal Pulse Response



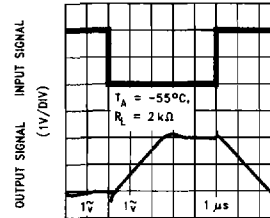
TIME (1 μs /DIV)

Inverting Large Signal Pulse Response



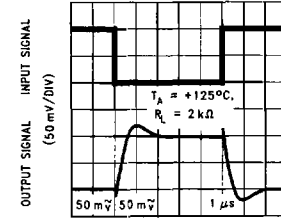
TIME (1 μs /DIV)

Inverting Large Signal Pulse Response



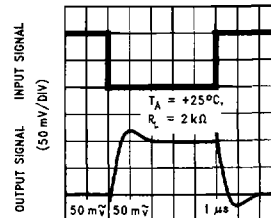
TIME (1 μs /DIV)

Inverting Small Signal Pulse Response



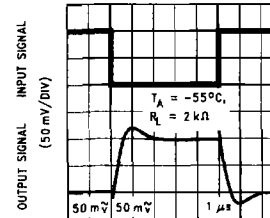
TIME (1 μs /DIV)

Inverting Small Signal Pulse Response



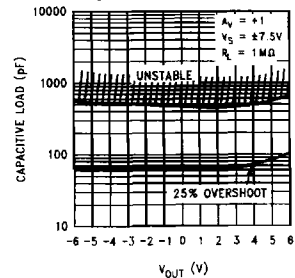
TIME (1 μs /DIV)

Inverting Small Signal Pulse Response



TIME (1 μs /DIV)

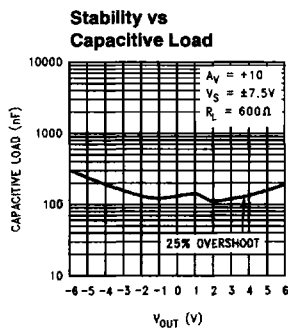
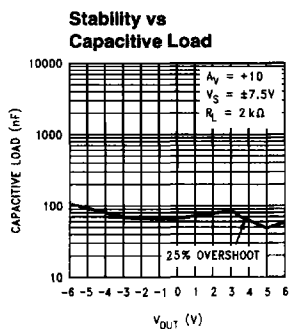
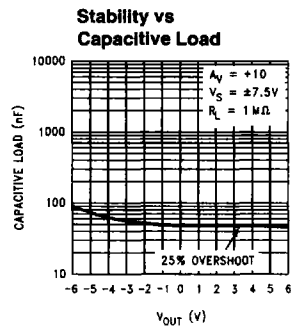
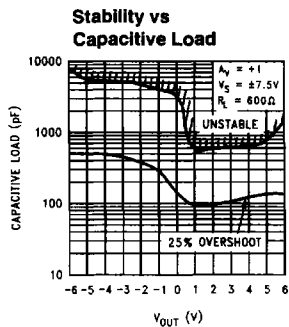
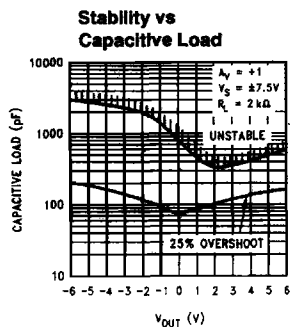
Stability vs Capacitive Load



TL/A/11714-8

Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)



TL/H/11714-9

Application Information (Continued)

1.0 Amplifier Topology

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6484's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

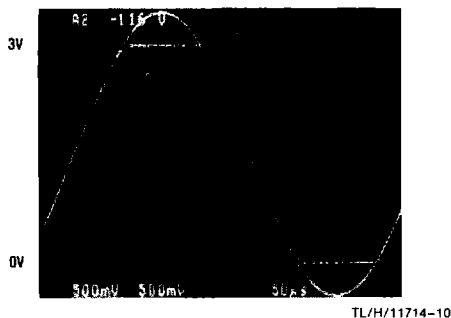


FIGURE 1. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

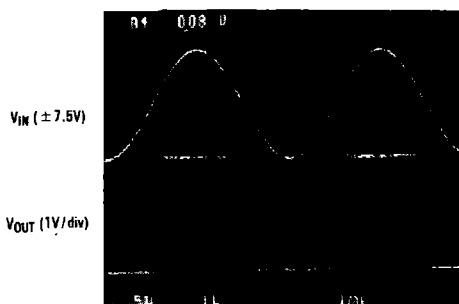


FIGURE 2. A $\pm 7.5V$ Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor as shown in *Figure 3*.

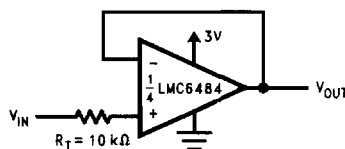


FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6484 is 180Ω sourcing and 130Ω sinking at $V_S = 3V$ and 110Ω sourcing and 83Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6484 can typically directly drive a 100 pF load with $V_S = 15V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

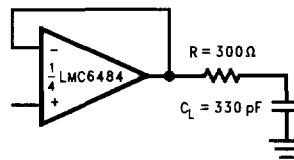
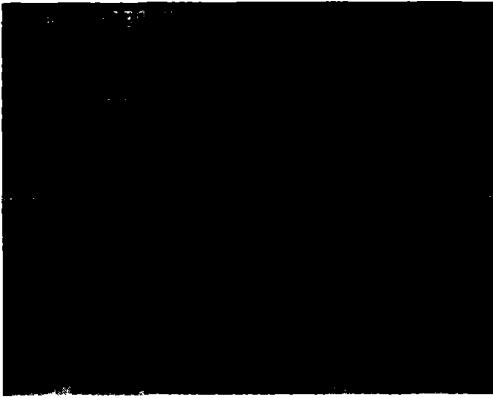


FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

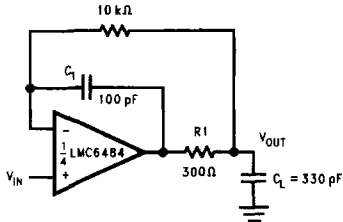
Application Information (Continued)



TL/H/11714-18

FIGURE 5. Pulse Response of the LMC6484 Circuit in Figure 4

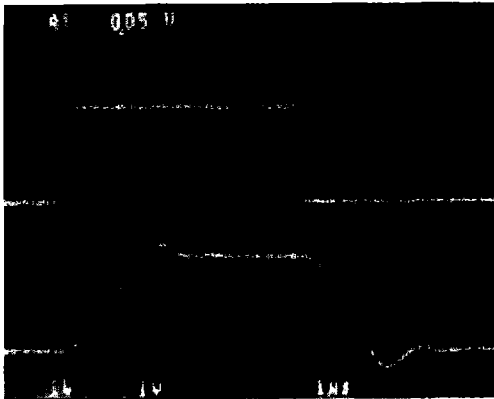
Improved frequency response is achieved by indirectly driving capacitive loads as shown in Figure 6.



TL/H/11714-15

FIGURE 6. LMC6484 Non-Inverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 7.

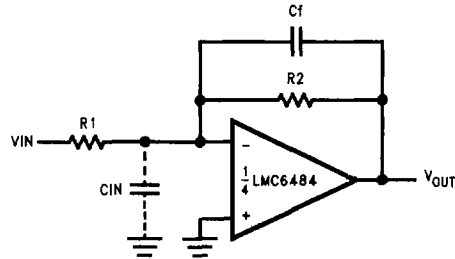


TL/H/11714-16

FIGURE 7. Pulse Response of LMC6484 Circuit in Figure 6

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.



TL/H/11714-19

FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 8), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

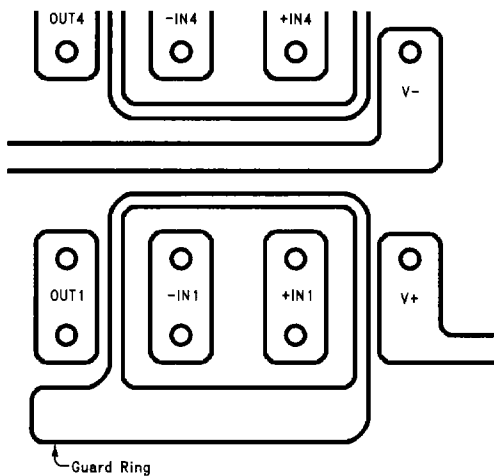
Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

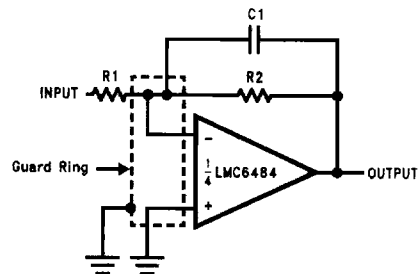
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board, when one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 9*. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6484's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 10a*, *10b* and *10c* for typical connections of guard rings for standard op-amp configurations.



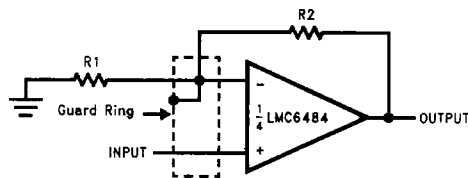
TL/H/11714-20

FIGURE 9. Example of Guard Ring in P.C. Board Layout



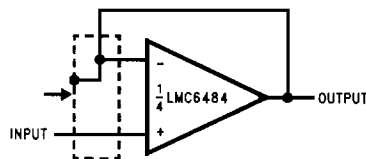
TL/H/11714-21

(a) Inverting Amplifier



TL/H/11714-22

(b) Non-Inverting Amplifier

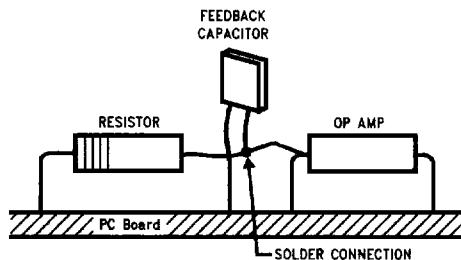


TL/H/11714-23

(c) Follower

FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 11*.



TL/H/11714-24

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

Application Information (Continued)

11.0 Spice Macromodel

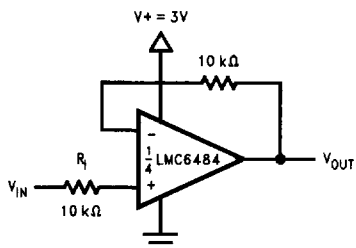
A spice macromodel is available for the LMC6484. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

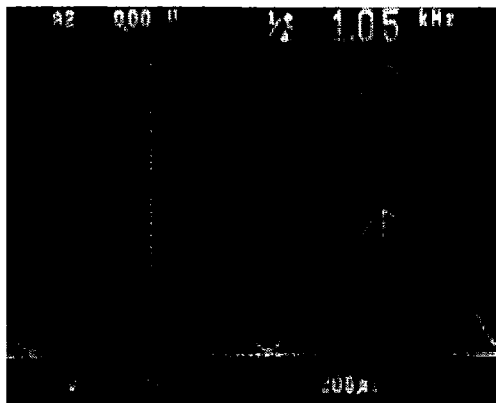
Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications



TL/H/11714-31

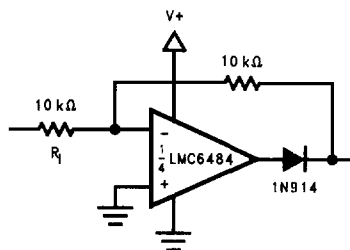
FIGURE 17. Half-Wave Rectifier with Input Current Protection (R_I)



TL/H/11714-32

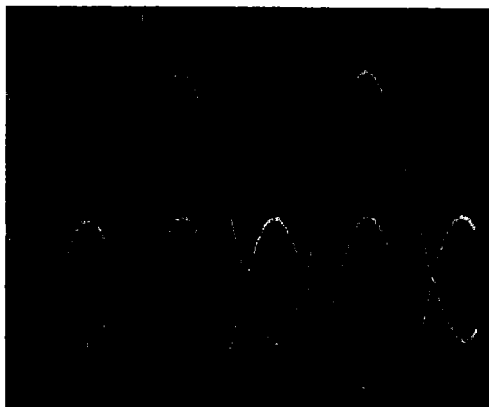
FIGURE 17a. Half-Wave Rectifier Waveform

The circuit in *Figure 17* uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in *Figure 18*.



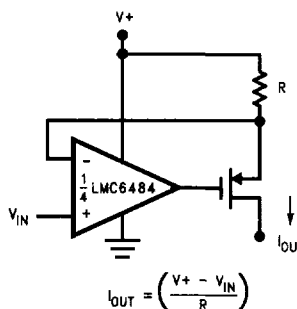
TL/H/11714-33

FIGURE 18. Full Wave Rectifier with Input Current Protection (R_I)



TL/H/11714-34

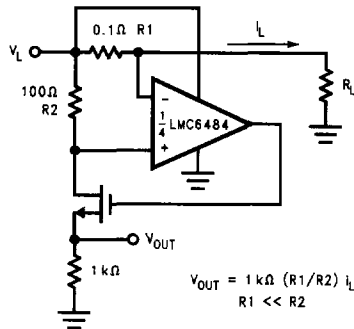
FIGURE 18a. Full Wave Rectifier Waveform



TL/H/11714-35

FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications (Continued)

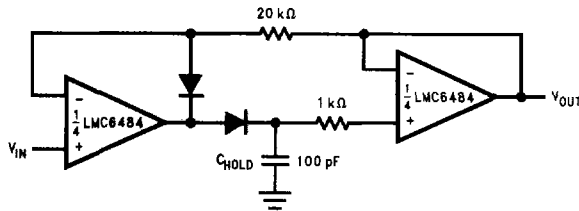


$$V_{OUT} = 1 \text{ k}\Omega \left(\frac{R1}{R2} \right) I_L$$

$$R1 \ll R2$$

TL/H/11714-36

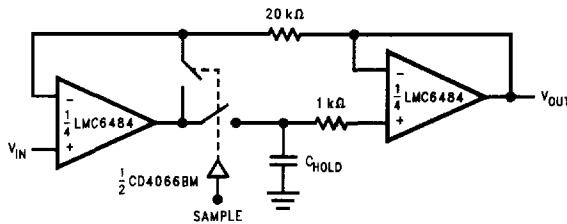
FIGURE 20. Positive Supply Current Sense



TL/H/11714-37

FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

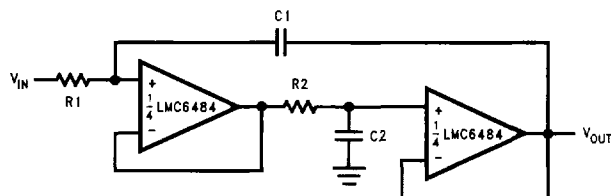
In *Figure 21* dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.



TL/H/11714-38

FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6484's high CMRR (85 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.



TL/H/11714-27

$$R1 = R2, C1 = C2; f = \frac{1}{2\pi R1 C1}; DF = \frac{1}{2} \frac{\sqrt{C2}}{\sqrt{C1}} \frac{\sqrt{R2}}{\sqrt{R1}}$$

FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in *Figure 23* can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.