

Electronic Volume

Description

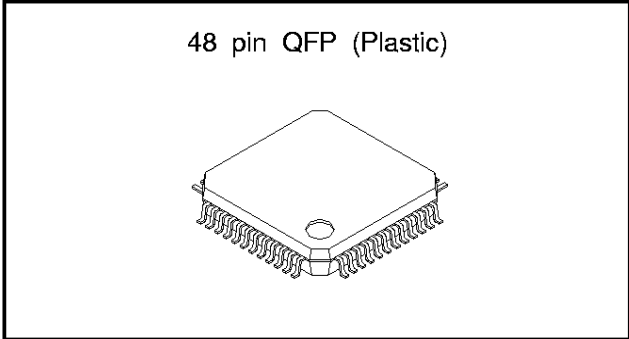
The CXA2506Q is a 2-channel electronic volume IC. A 34-bit serial data input controls the level and characteristics of the output signal. It may be used in car stereos and general audio systems.

Features

- Loudness (Full boost at -32 dB or less of VRC)
- Volume control
(from 0 dB to -87 dB, -∞ dB: Fine (1 dB-step)
 Coarse (8 dB-step)
- Balance
- Tone control
(3-band, 2 dB-step from -15 dB to +15 dB)
- Fader
(2 dB-step to -20 dB, -25 dB, -35 dB, -45 dB, -60 dB, -∞ dB)
- Input and gain selector (4 channels)
- Serial data control (DATA, CLK, CE)
- Single 8 V power supply
- Zero-cross detection circuit
- Timer
- Power-off mute

Structure

Bipolar IC



Absolute Maximum Ratings (Ta=25 °C)

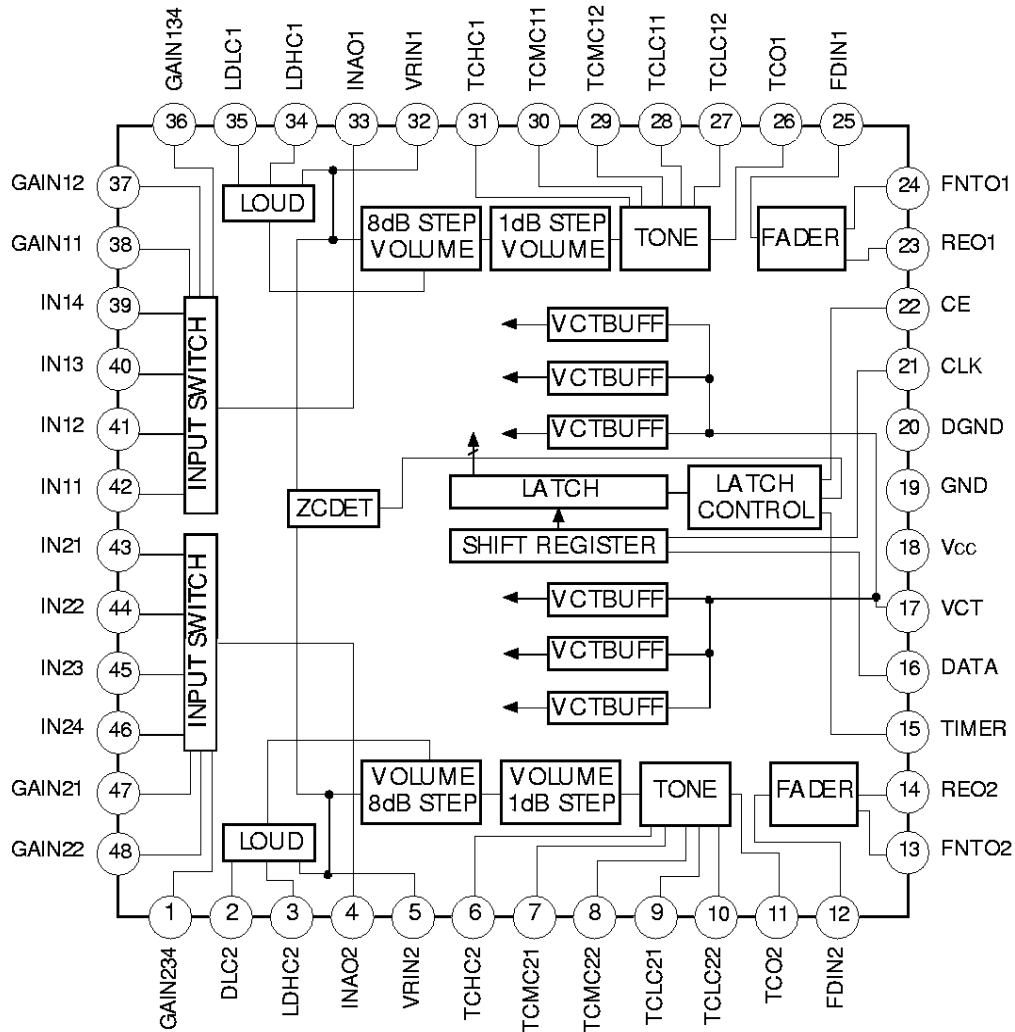
| | | | |
|-------------------------------|------|-------------|--------------|
| • Supply voltage | Vcc | 13 | V |
| • Operating temperature | Topr | -40 to +85 | °C |
| • Storage temperature | Tstg | -65 to +150 | °C |
| • Allowable power dissipation | Pd | 350 | mW |
| | | | (Ta = 85 °C) |

Recommended Operating Condition

| | | | |
|------------------|-----|---------|---|
| • Supply voltage | Vcc | 6 to 12 | V |
|------------------|-----|---------|---|

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Block Diagram and Pin Configuration



Pin Description and Equivalent Circuit

| Pin No. | Pin Name | I/O Resistance Pin voltage | Equivalent Circuit | Description |
|---------|----------------|-------------------------------|--------------------|--------------------------------------|
| 2 35 | LDLC2 LDLC1 | 6.18 k VCT | | Sets loudness low cut-off frequency. |
| 3 34 | LDHC2 LDHC1 | 8.92 k VCT | | Set loudness high cut-off frequency |
| 4 33 | INAO2 INAO1 | — VCT | | Input selector output |
| 5 32 | VRIN2 VRIN1 | 10 k VCT | | Volume input |
| 6 31 | TCHC2 TCHC1 | 5 k VCT | | Set tone Treble frequency |

| Pin No. | Pin Name | I/O Resistance Pin voltage | Equivalent Circuit | Description |
|----------|------------------|-------------------------------|--------------------|--------------------------|
| 7 30 | TCMC21 TCMC11 | 4 k VCT | | Sets tone Mid frequency |
| 8 29 | TCMC22 TCMC12 | 4 k VCT | | Sets tone Mid frequency |
| 9 28 | TCLC21 TCLC11 | 8 k VCT | | Sets tone Bass frequency |
| 10 27 | TCLC22 TCLC12 | 8 k VCT | | Sets tone Bass frequency |
| 11 26 | TCO2 TCO1 | — VCT | | Tone control output |

| Pin No. | Pin Name | I/O Resistance Pin voltage | Equivalent Circuit | Description |
|----------|----------------|-------------------------------|--------------------|---------------------|
| 12 25 | FDIN2 FDIN1 | 24 k VCT | | Fader input |
| 13 24 | REO2 REO1 | — VCT | | Rear output |
| 14 23 | FNT02 FNT01 | — VCT | | Front output |
| 15 | TIMER | ~ ∞ | | Sets timer constant |
| 16 | DATA | ~ ∞ | | Serial data input |

| Pin No. | Pin Name | I/O Resistance Pin voltage | Equivalent Circuit | Description |
|--|--|-------------------------------|--------------------|---|
| 17 | VCT | — VCT | | 1/2 Vcc |
| 18 | Vcc | — Vcc | | Power supply input |
| 19 | GND | — Gnd | | Ground |
| 20 | DGND | — — | | Digital ground |
| 21 | CLK | ≈ ∞ — | | Serial clock input |
| 22 | CE | ≈ ∞ — | | Latch enable input |
| 1 36 37 38 47 49 | GAIN234 GAIN134 GAIN12 GAIN11 GAIN21 GAIN22 | ≈ ∞ VCT | | External gain setting for input amplifier |
| 39 40 41 42 43 44 45 46 | IN14 IN13 IN12 IN11 IN21 IN22 IN23 IN24 | 50 k VCT | | Signal input |

Data Format

| | | |
|-----------|-----|--------------|
| First Bit | D1 | NOP |
| | D2 | NOP |
| | D3 | ISW |
| | D4 | |
| | D5 | LOUD |
| | D6 | VRC1 |
| | D7 | |
| | D8 | |
| | D9 | |
| | D10 | VRF1 |
| | D11 | |
| | D12 | |
| | D13 | VRC2 |
| | D14 | |
| | D15 | |
| | D16 | |
| | D17 | VRF2 |
| | D18 | |
| | D19 | |
| | D20 | TONE BASS |
| | D21 | |
| | D22 | |
| | D23 | |
| | D24 | TONE MID |
| | D25 | |
| | D26 | |
| | D27 | |
| | D28 | TONE TREBLE |
| | D29 | |
| | D30 | |
| | D31 | |
| | D32 | FADER |
| | D33 | |
| | D34 | |
| | D35 | |
| Last Bit | D36 | FADER SELECT |

ISW

| MODE | D3 | D4 |
|----------------------------|----|----|
| IN14/IN24, GAIN134/GAIN234 | 1 | 1 |
| IN13/IN23, GAIN134/GAIN234 | 1 | 0 |
| IN12/IN22, GAIN12/GAIN22 | 0 | 1 |
| IN11/IN21, GAIN11/GAIN21 | 0 | 0 |

LOUD

| MODE | D5 |
|------|----|
| ON | 1 |
| OFF | 0 |

VRC1/VRC2

| OUTPUT (dB) | D6/D13 | D7/D14 | D8/D15 | D9/D16 |
|-------------|--------|--------|--------|--------|
| 0 | 1 | 1 | 1 | 1 |
| -8 | 1 | 1 | 1 | 0 |
| -16 | 1 | 1 | 0 | 1 |
| -24 | 1 | 1 | 0 | 0 |
| -32 | 1 | 0 | 1 | 1 |
| -40 | 1 | 0 | 1 | 0 |
| -48 | 1 | 0 | 0 | 1 |
| -56 | 1 | 0 | 0 | 0 |
| -64 | 0 | 1 | 1 | 1 |
| -72 | 0 | 1 | 1 | 0 |
| -80 | 0 | 1 | 0 | 1 |
| -∞ | 0 | 1 | 0 | 0 |
| -∞ | 0 | 0 | 0 | 0 |

VRF1/VRF2

| OUTPUT (dB) | D10/D17 | D11/D18 | D12/D19 |
|-------------|---------|---------|---------|
| 0 | 1 | 1 | 1 |
| -1 | 1 | 1 | 0 |
| -2 | 1 | 0 | 1 |
| -3 | 1 | 0 | 0 |
| -4 | 0 | 1 | 1 |
| -5 | 0 | 1 | 0 |
| -6 | 0 | 0 | 1 |
| -7 | 0 | 0 | 0 |

BASS/MID/TREBLE

| OUTPUT (dB) | D20/D24/D28 | D21/D25/D29 | D22/D26/D30 |
|-------------|-------------|-------------|-------------|
| 15 | 1 | 1 | 1 |
| 12 | 1 | 1 | 0 |
| 10 | 1 | 0 | 1 |
| 8 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 |
| 2 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |

BOOST/CUT

| MODE | D23/D27/D31 |
|-------|-------------|
| BOOST | 1 |
| CUT | 0 |

FADER

| OUTPUT (dB) | D32 | D33 | D34 | D35 |
|-------------|-----|-----|-----|-----|
| -∞ | 1 | 1 | 1 | 1 |
| -60 | 1 | 1 | 1 | 0 |
| -45 | 1 | 1 | 0 | 1 |
| -35 | 1 | 1 | 0 | 0 |
| -25 | 1 | 0 | 1 | 1 |
| -20 | 1 | 0 | 1 | 0 |
| -18 | 1 | 0 | 0 | 1 |
| -16 | 1 | 0 | 0 | 0 |
| -14 | 0 | 1 | 1 | 1 |
| -12 | 0 | 1 | 1 | 0 |
| -10 | 0 | 1 | 0 | 1 |
| -8 | 0 | 1 | 0 | 0 |
| -6 | 0 | 0 | 1 | 1 |
| -4 | 0 | 0 | 1 | 0 |
| -2 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

FADER SELECT

| MODE | D36 |
|-------|-----|
| FRONT | 1 |
| REAR | 0 |

RESET

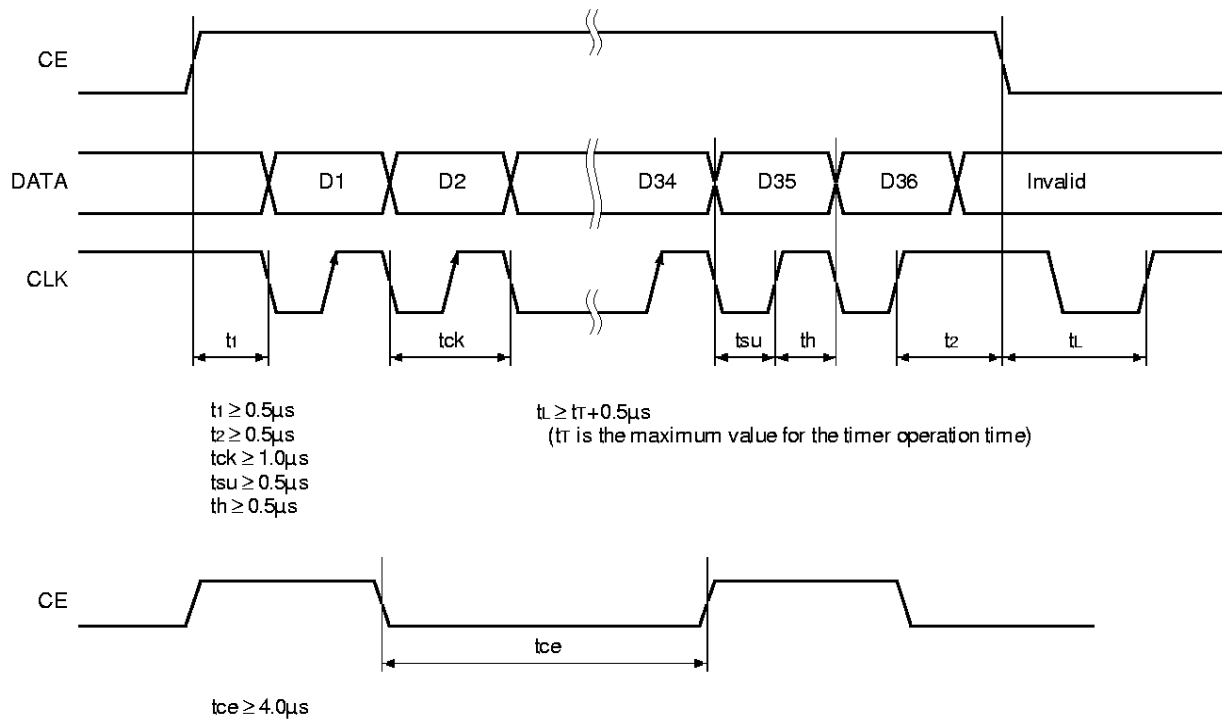
Reset is performed automatically when power is first supplied to the IC; there is no reset pin.

The following table shows the respective statuses of various settings after a reset has been performed.

However, from the time when power is first supplied until the first data transfer, keep CE high by pulling it up to Vcc, etc.

| MODE | SET VALUE |
|-------------|------------|
| INPUT | 1 |
| VRC1 | -∞ dB |
| VRF1 | -7 dB |
| VRC2 | -∞ dB |
| VRF2 | -7 dB |
| LOUD | OFF |
| TONE BASS | 0 dB |
| TONE MID | 0 dB |
| TONE TREBLE | 0 dB |
| FADER | 0 dB, REAR |

Timing Chart



Timer Waiting Period Setting Chart ($V_{cc} = 6$ to 12 V, operating temperature = -40 °C to 85 °C)

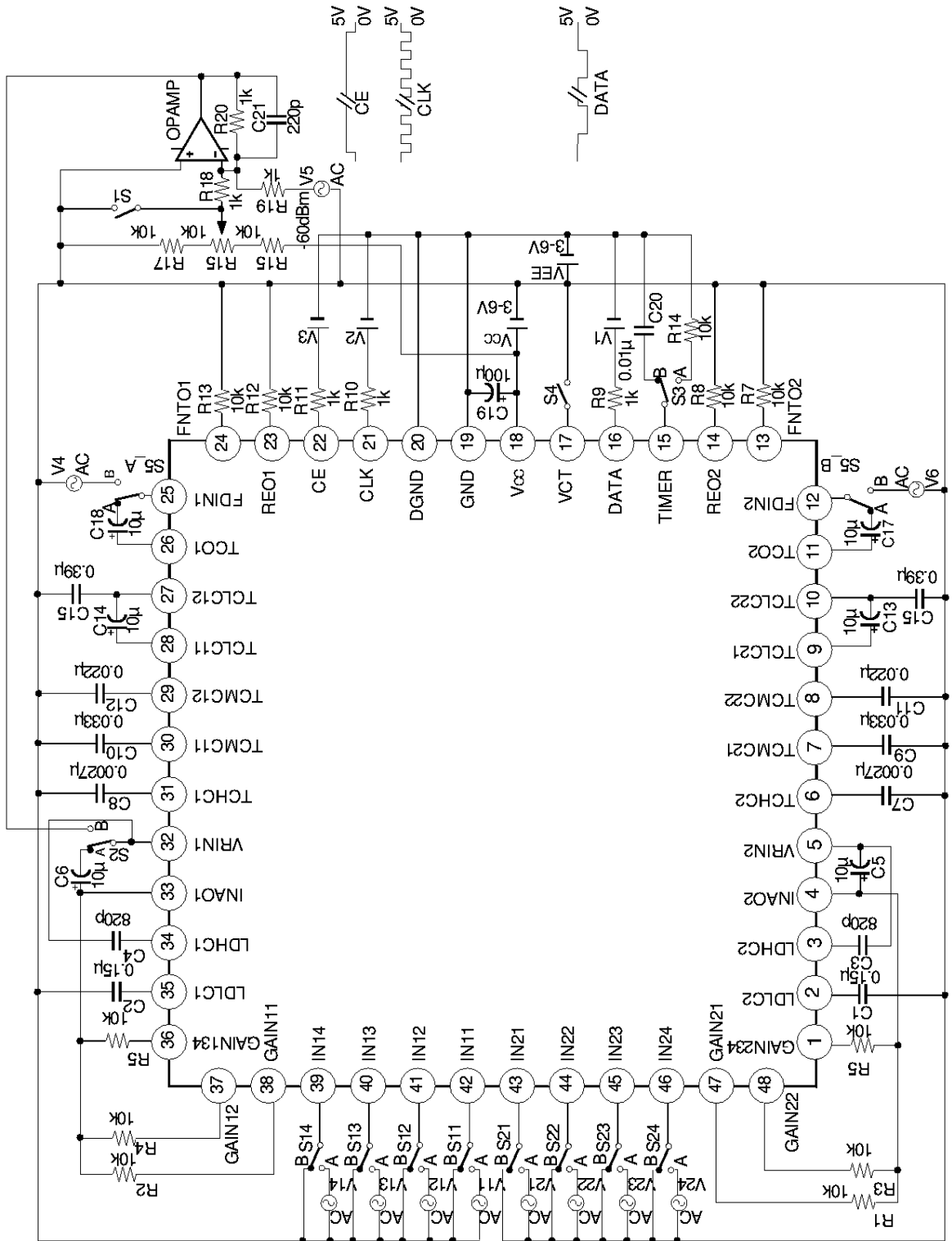
| TIMER pin capacitance C | Waiting period | | |
|-------------------------|----------------|-------------|-------------|
| | Min. | Typ. | Max. |
| C = 100 pF | 3 μs | 5 μs | 9 μs |
| C = 0.001 μF | 30 μs | 50 μs | 90 μs |
| C = 0.01 μF | 300 μs | 500 μs | 900 μs |
| C = 0.1 μF | 3 ms | 5 ms | 9 ms |
| C = 1 μF | 30 ms | 50 ms | 90 ms |
| C = 10 μF | 300 ms | 500 ms | 900 ms |

Electrical Characteristics

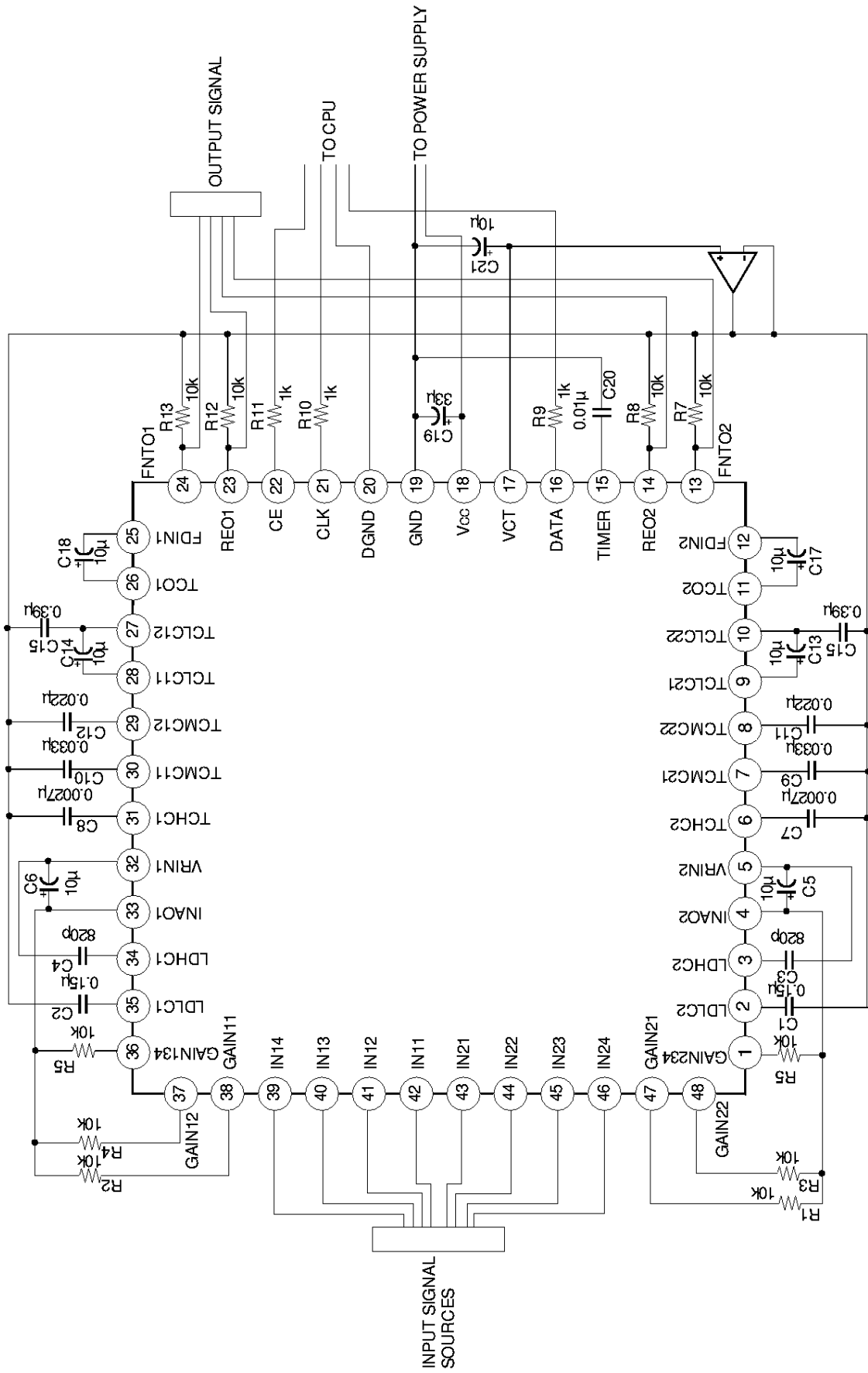
V_{cc}=8 V, T_a=25 °C, Input=0 dB unless otherwise specified

| Item | Symbol | Conditions | Min. | Typ. | Max | Unit | |
|---------------------------|------------------|--|------|-------|--------------------|-------------------|---|
| Current consumption | I _{cc} | No signal | — | 21 | 28 | mA | |
| Total Harmonic distortion | THD | 1 kHz, 5 dBm output | — | 0.003 | 0.01 | % | |
| Output noise voltage | V _n | Short-circuit at input, A weight | — | 8 | 10 | μV _{rms} | |
| Max output voltage | V _{om} | 1 kHz | 8 | — | — | dBm | |
| Separation | CS | 1 kHz | 72 | 90 | — | dB | |
| Max. attenuation factor | ATT _m | | 85 | 90 | — | | |
| Loudness LOW | G _{lb} | 100 Hz, VRC=-16 dB | 7 | 8 | 9 | | |
| Loudness HIGH | G _{lh} | 10 kHz, VRC=-16 dB | 5 | 6 | 7 | | |
| Bass max. boost gain | G _{bb} | | 13 | 15 | 17 | | |
| Bass max. cut gain | G _{bc} | | 13 | 15 | 17 | | |
| Mid max. boost gain | G _{mb} | | 13 | 15 | 17 | | |
| Mid max. cut gain | G _{mc} | | 13 | 15 | 17 | | |
| Treble max. boost gain | G _{tb} | | 13 | 15 | 17 | | |
| Treble max. cut gain | G _{tc} | | 13 | 15 | 17 | | |
| Input voltage HIGH | V _{sh} | DATA, CLK, CE | 3 | — | 6 | | V |
| Input voltage LOW | V _{sl} | DATA, CLK, CE | 0 | — | 1.5 | | |
| Input voltage range | V _{in} | IN11 to 14 IN21 to 24 VRIN1, 2 FDIN1, 2 | 1 | — | V _{cc} -1 | | |

Electrical Characteristic Test Circuit

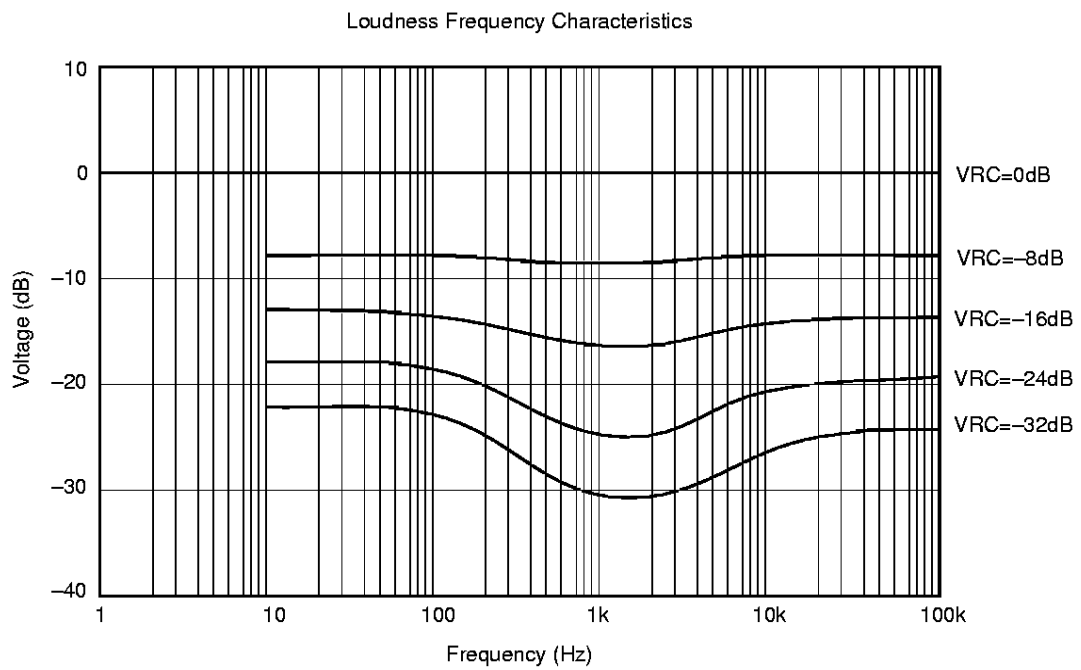
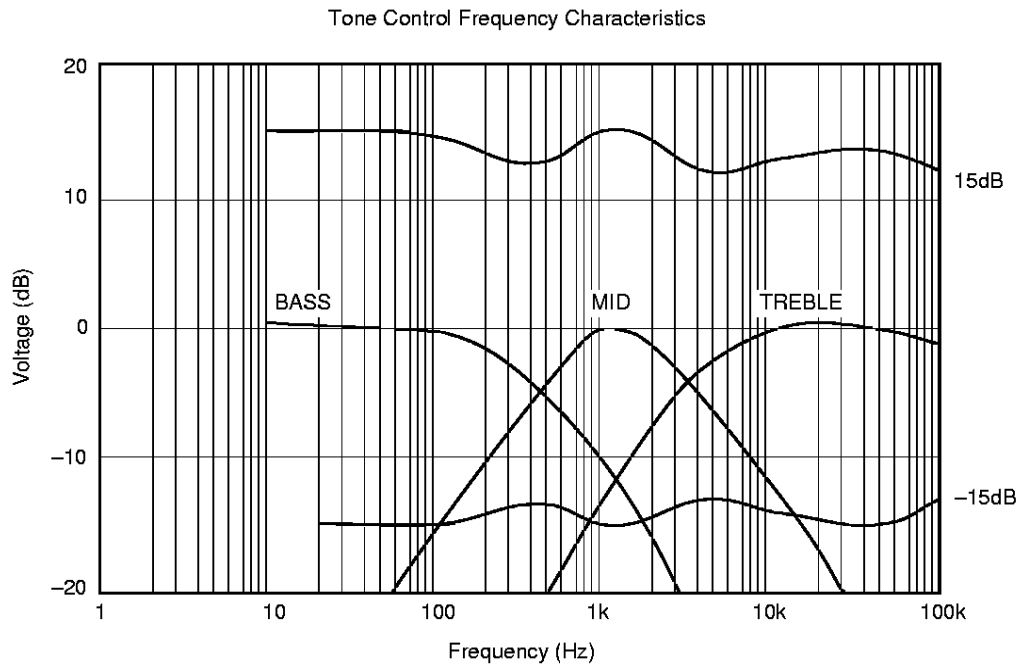


Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

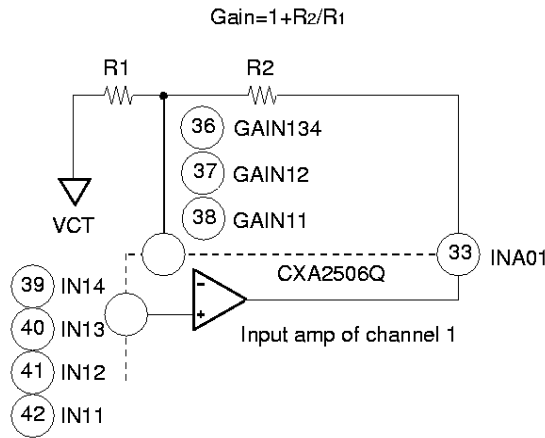
Example if Representative Characteristics



Description of Operation

(1) Gain of input amplifier

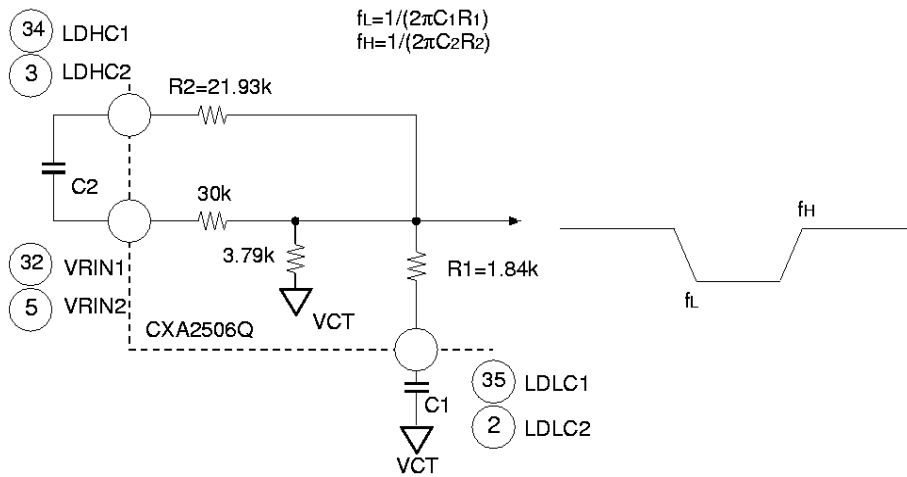
The input selector stage may be configured as a buffer or a non-inverting amplifier.



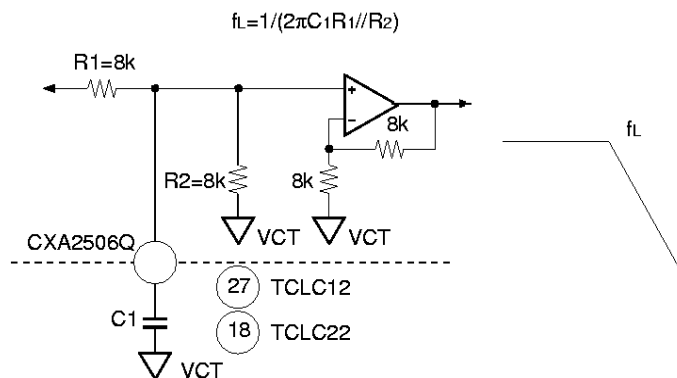
(2) Loud

The loudness function achieves the necessary frequency characteristics by using a filter as shown below.

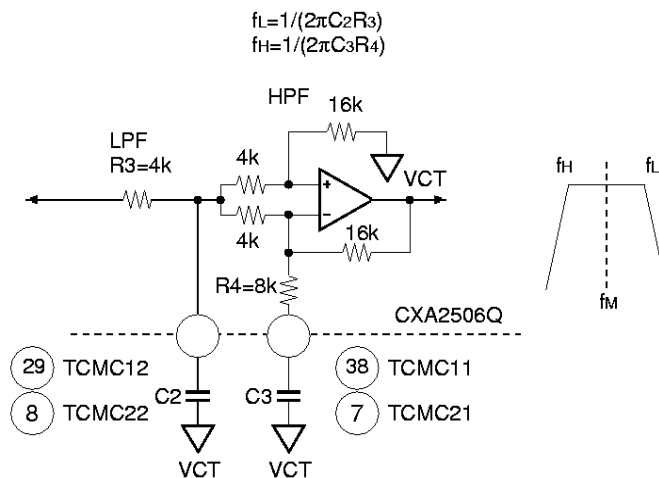
The resistors are built in so that f_L and f_H can be set by selecting C1 and C2.



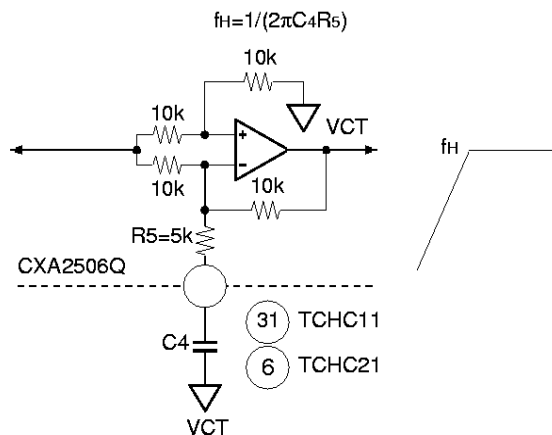
(3) Tone control
BASS: LPF



MID: BPF



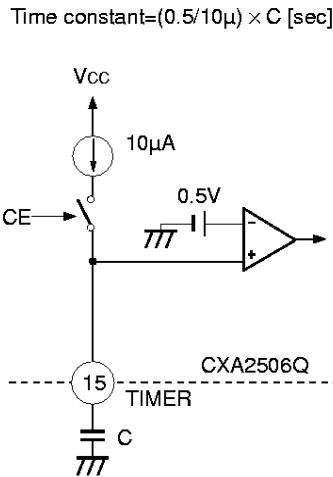
TREBLE: HPF



(4) Zero-cross detector and Timer

A built-in zero-cross detection circuit is used to detect the zero-cross points of the input signal. When data arrived at the IC, they are executed at the next zero-cross point or when there is no input signal. This is to minimize 'click' noise during the transition of levels.

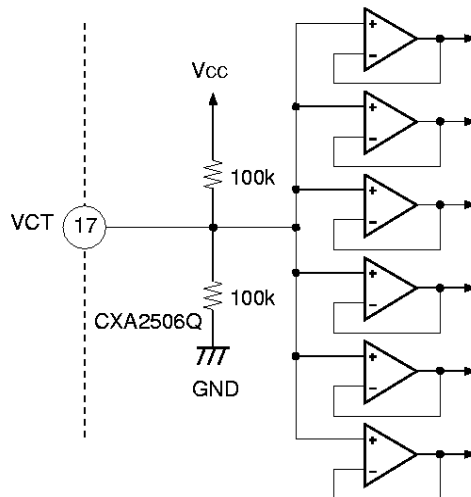
The timer circuit is added to ensure that the data is executed even when a zero-cross point is not detected after a pre-determined period of time from the falling edge of the CE pulse.



(5) VCT pin

The internal circuit of VCT pin has the following structure.

Insert a buffer when using it as a reference voltage for an external circuit.

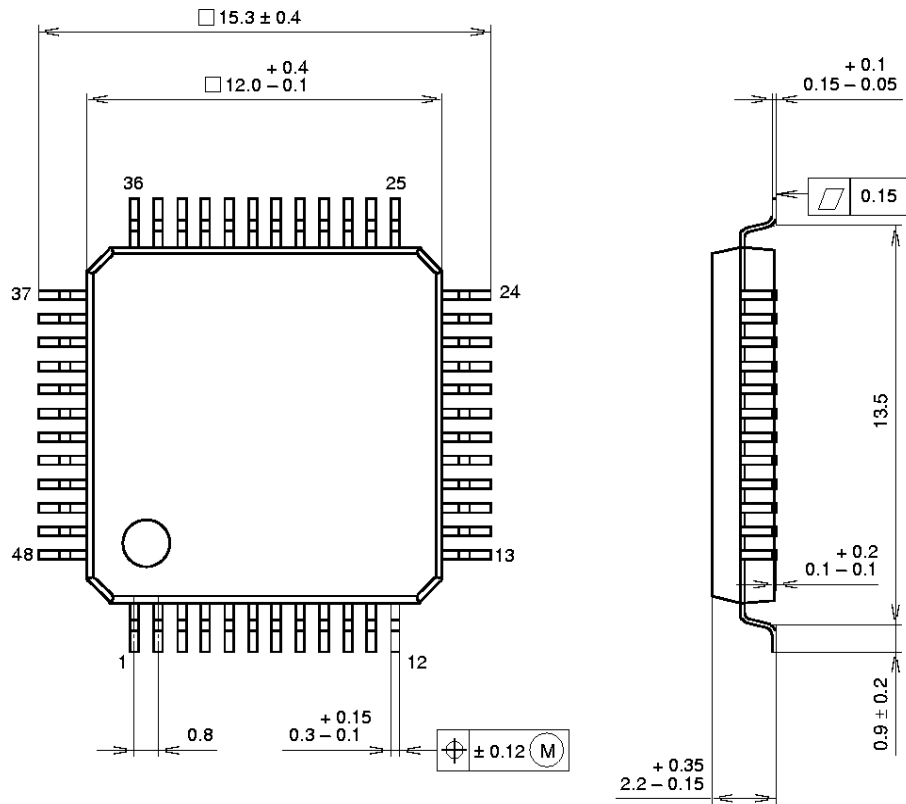


(6) Power-off Mute

This function mutes the output pins FNT01, FNT02, REO1 and REO2, when the Vcc goes below 5V, by turning off the bias of the output stage of the fader circuit. By so doing, the 'pop' noise caused by the drop in these pins potential from Vcc/2 during power-off can be avoided.

Package Outline Unit : mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

| | |
|------------|------------------|
| SONY CODE | QFP-48P-L04 |
| EIAJ CODE | *QFP048-P-1212-B |
| JEDEC CODE | _____ |

| | |
|------------------|----------------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER / PALLADIUM PLATING |
| LEAD MATERIAL | COPPER / 42 ALLOY |
| PACKAGE WEIGHT | 0.7g |

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).