Technical Data
Datasheet 6132, Rev. -

SiC FET Full Bridge with Integrated Gate Drive

FEATURES:

- 1200VDC max voltage
- 60A max current
- Compact package
- Temperature range -55°C to +125°C
- Efficient conduction cooled design
- Total weight: 1.10 oz.

DESCRIPTION:

This SiC FET Full Bridge power module can be used in various applications including, but not limited to, power converters and motor drives. The integrated gate drive simplifies the system design and optimizes the dynamic performance of the bridge.

The small size of this complete module makes it ideal for high reliability industrial, aerospace, and military applications.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Bus Supply Voltage			1200	V
PWM Switching Frequency	F_{SW}	-	500	kHz
Continuous Drain Current, each Leg of Full Bridge	I_D	-	60	A
Pulsed Drain Current, each Leg of Full Bridge Pulse Width limited by T_{jmax}	$I_{D(pulse)}$	-	120	A
Junction Temperature	T_{jmax}	-55	150	˚C
Storage Temperature	$T_{s\,max}$	-55	150	˚C
Operating Temperature on Cold Plate	$T_{c\,max}$	-55	125	˚C

Technical Data
Datasheet 6132, Rev. -

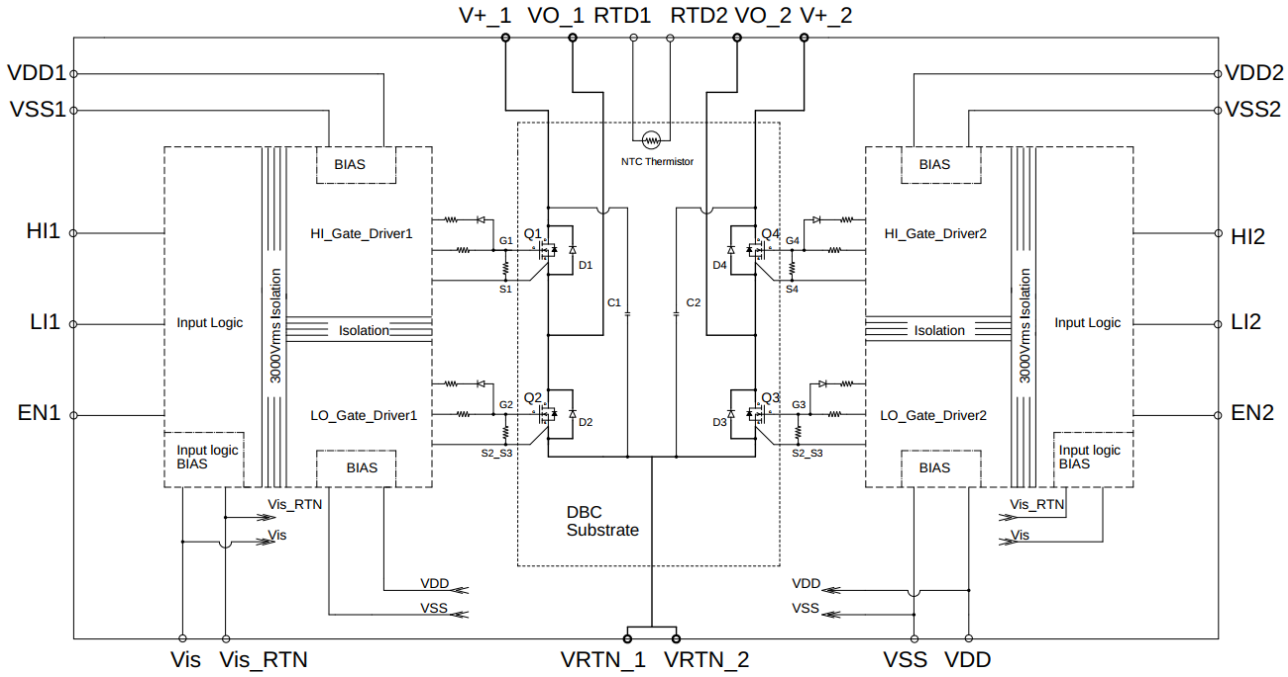

Figure 1 – Block Diagram

Connections for Full Bridge Application

V+_1, V+_2:	both pins must connect to DC Bus power supply's Positive, no internal connection between these two pins
VRTN_1,VRTN_2:	both pins must connect to DC Bus power supply's Return, VRTN_1 and VRTN_2 are internally tied together
VO_1, VO_2:	output connections
HI1, LI1, HI2, LI2:	gate control inputs; internally bypassed to V_{is_RTN} with 1.0kohm resistor and 22pF capacitor, external in-line resistors [33ohm, 59ohm] recommended
EN1, EN2:	enable driver outputs; internally bypassed to V_{is_RTN} with 1.0kohm resistor and 1nF capacitor, external in-line resistors [33ohm, 59ohm] recommended
|Vis|/V_{is}, V_{is_RTN}:	power supply input to logic circuitry
|VDD|/VDD, VSS:	power supply input to LO_Gate_Driver1 and LO_Gate_Driver2 circuitry
|VDD1|/VDD1, VSS1:	power supply input HI_Gate_Driver1 circuitry
|VDD2|/VDD2, VSS2:	power supply input for HI_Gate_Driver2 circuitry
RTD1, RTD2	connection to internal thermistor

- Requirements to DC Bus power supply, |V_{is}|, |VDD|, |VDD1| and |VDD2|:

  Minimum 2000VDC isolation between |VDD|, |VDD1| and |VDD2|

  Minimum 2000VDC isolation between |VDD1|/|VDD2| power supplies and DC Bus power supply.

  Power supply to |VDD| needs to be isolated to DC Bus power supply: VSS is internally clamped 3.6V below VRTN_1/VRTN_2, for negative gate drive

  3000VRMS isolation between power supply to |V_{is}| and DC Bus/|VDD1|/|VDD2| power supplies is recommended

Technical Data
Datasheet 6132, Rev. -

ELECTRICAL CHARACTERISTICS OF FULL BRIDGE, PER EACH LEG

T_J=25°C, UNLESS OTHERWISE SPECIFIED.
Production units are tested at room temperature. Low/High temperature operation is guaranteed by design.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V+_1, V+_2	DC Bus Supply Voltage, Absolute Max to V_RTN1, V_RTN_2 Recommended		- 400	1200 600	VDC
MOSFET (Q1, Q2, Q3, Q4) Characteristics					
BV_{DSS}	Drain to Source Breakdown Voltage I_D = 100 µA, V_{GS} = 0V	1200			VDC
I_D	Continuous Drain Current T_J = 25°C T_J = 125°C			60 30	A
$I_{D(pulse)}$	Pulsed Drain Current			120	A
V_{GS}	Gate to Source Voltage		-4/+15 Static	-8/+19 Dynamic	VDC
I_{GSS}	Gate-Source Leakage Current V_{GS} = +15V, V_{DS} = 0V		10	250	nA
$V_{GS(th)}$	Gate Threshold Voltage T_J = 25°C I_D = 17.7mA, V_{DS} = V_{GS} T_J = 105°C	1.8 -	2.5 2.0	3.6 -	VDC
I_{DSS}	Zero Gate Voltage Drain Current V_{DS} = 1200 V, V_{GS} = 0V	-	1	25	µA
$R_{DS(on)}$	Drain-Source On-State Resistance T_J = 25°C I_D = 50A, V_{GS} = +15V T_J = 105°C	14 -	22 40	30 -	mΩ
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer capacitance V_{DS} = 200 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV	-	4820 300 18	-	pF
Q_{gs} Q_{gd} Q_g	Gate to Source Charge Gate to Drain Charge Total Gate Charge V_{DS} = 600 V, I_D = 50A, V_{GS} = -4V/+15V	-	49 50 162	-	nC
Anti-parallel Diode (D1, D2, D3, D4) Characteristics					
V_F	Diode Forward Voltage T_J = 25°C I_F = 20A T_J = 105°C	1.0 -	1.5 2.0	1.8 -	VDC
I_R	Reverse Current V_R = 1200V	-	35	200	µA
QC	Total Capacitive Charge IF = 20A, VR =400V, di/dt = 150 A/ µs	-	68	-	nC
Internal DC Link - Snubber Capacitance between V+_1/V+_2 and VRTN_1/VRTN_2					
C1, C2	1.2 kV, NP0, ±5%, -55˚C to 150˚C	-	12	-	nF
Stray inductance					
L_{stray}	between pin 1 and 3 or pin 7 and 6		7.0		nH

ELECTRICAL CHARACTERISTICS OF LOGIC AND DRIVER INPUT

T_J=25°C, UNLESS OTHERWISE SPECIFIED.
Production units are tested at room temperature. Low/High temperature operation is guaranteed by design.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Absolute Maximum Ratings					
V_{is}	Logic supply voltage, V_{is} to V_{is_RTN}	-0.5		20.0	VDC
HI1, LI1, HI2, LI2	Input logic signals to V_{is_RTN}, TTL/CMOS compatible input threshold	-0.5		V_{Vis}+0.5	VDC
VDD, VSS VDD1, VSS1 VDD2, VSS2	Driver side supply voltage	-0.5		22.0	VDC
Recommend Operating Conditions					
V_{is}	Logic supply voltage, V_{is} to V_{is_RTN}	3.0		15.0	VDC
VDD, VSS VDD1, VSS1 VDD2, VSS2	Driver side supply voltage	18.0		20.0	VDC
V_{is} to V_{is_GND} Undervoltage Thresholds					
V_{is_ON}	UVLO rising threshold	2.5	2.7	2.9	VDC
V_{is_OFF}	UVLO falling threshold	2.3	2.5	2.7	VDC
V_{is_HYS}	UVLO threshold hysteresis		0.2		VDC
VDD-VSS, VDD1-VSS1, VDD2-VSS2 Undervoltage Thresholds					
	UVLO rising threshold	12.5	13.5	14.5	VDC
	UVLO falling threshold	11.5	12.5	13.5	VDC
	UVLO threshold hysteresis		1.0		VDC
EN1, EN2 Thresholds					
V_{ENH}	Enable high voltage	2.0			VDC
V_{ENH}	Enable low voltage			0.8	VDC
HI1, LI1, HI2 and LI2 Thresholds					
	Input logic high threshold voltage	1.6	1.8	2.0	VDC
	Input logic low threshold voltage	0.8	1.0	1.2	VDC
	Input logic threshold hysteresis		0.8		VDC
Switching Characteristics (Vis = 5V, VDD/VDD1/VDD2 = 15V)					
t_{RISE}	Output rise time, 20% to 80%, 1.8nF capacitor at gate drive output		6	16	ns

Technical Data
Datasheet 6132, Rev. -

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T_J=25°C, UNLESS OTHERWISE SPECIFIED.
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SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{FALL}	Output fall time, 90% to 10%, 1.8nF capacitor at gate drive output		7	12	ns
t_{PDHL}	Propagation delay from logic input to gate drive signal falling edges	14	19	30	ns
t_{PDLH}	Propagation delay from logic input to gate drive signal rising edges	14	19	30	ns
t_{PWD}	Pulse width distortion $\lvert t_{PDLH} - t_{PDHL} \rvert$			5	ns
t_{DM}	Propagation delays matching between V_{G1} and V_{G2}, V_{G3} and V_{G4}			5	ns
NTC Thermistor Characteristics (Heraeus Nexensos's M Sensor)					
R_0	Resistance @ T_C = 0 °C		1		K Ohm
R_{TOL}	Resistance Tolerance			±0.12	%
	Measuring Current	0.1		0.3	mA
TCR	$TCR = \frac{R_{100} - R_0}{R_0 * 100°C}$ R_{100} is resistance at 100ºC, R_0 is resistance at 0°C		3850		ppm/K
	Temperature Range	-70		500	°C
Resistance vs Temperature	t >= 0 º $R(t) = R_0 * (1 + A * t + B * t^2$ t < 0 ºC $R(t) = R_0 * (1 + A * t + B * t^2 + C * (t - 100°C) * t^3)$;	$A = 3.9083 * 10^{-3}$ ºC^{-1} $B = -5.775 * 10^{-7}$ °C^{-2} $C = -4.183 * 10^{-12}$ ºC^{-4}			
Internal Configurations					
VSS-VRTN_1 VSS-VRTN_2	VSS is internally clamped below VRTN_1/VRTN_2 for negative gate drive		-3.6		VDC
DT	Internal dead time setting		No		

Technical Data
Datasheet 6132, Rev. -

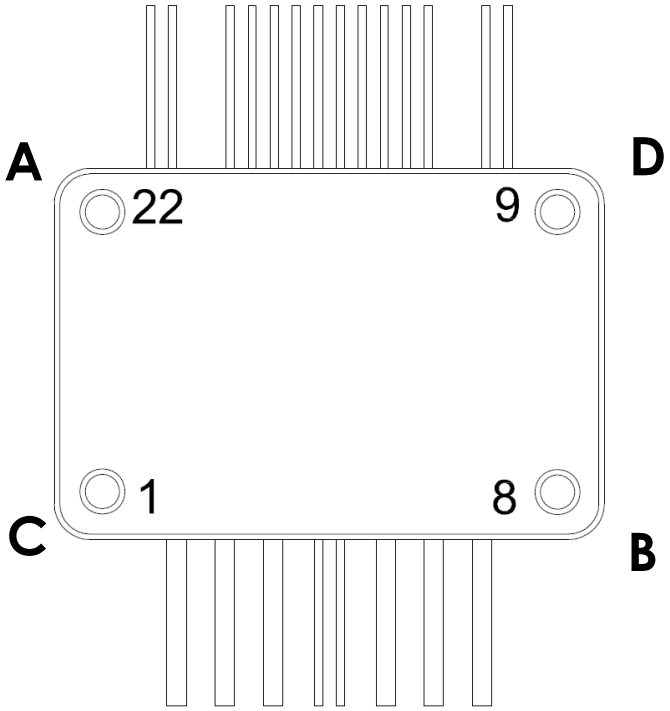
THERMAL AND MECHANICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JB\_M}$	MOSFET Junction-to- Base Plate Thermal Resistance Per Leg	-	.339	.390	$^oC/W$
$R_{\theta JB\_D}$	Diode Junction-to-Base Plate Thermal Resistance Per Leg	-	.884	1.017	$^oC/W$
Isolations	All pins to Base Plate/Screw mounting pads	-	-	2500	VDC
	Logic signals to driver signals $\lvert V_{is}\text{-VDD}\rvert$ $\lvert V_{is}\text{ -VDD1}\rvert$ $\lvert V_{is}\text{ -VDD2}\rvert$	-	-	2500	V_{RMS}
Mounting Torque	**see installation instructions** #4 Size Screw	3	-	4	in-lbs.
	Weight Module	-	32	40	g

INSTALLATION INSTRUCTIONS:

Recommended thermal interface material = Laird Tgon 805 (5 mil thick graphite pad)

1. Fasten screws to 1 to 2 in-lb. of torque in the following sequence: A, B, C, D.
2. Fasten screws to final torque in the same sequence: A, B, C, D



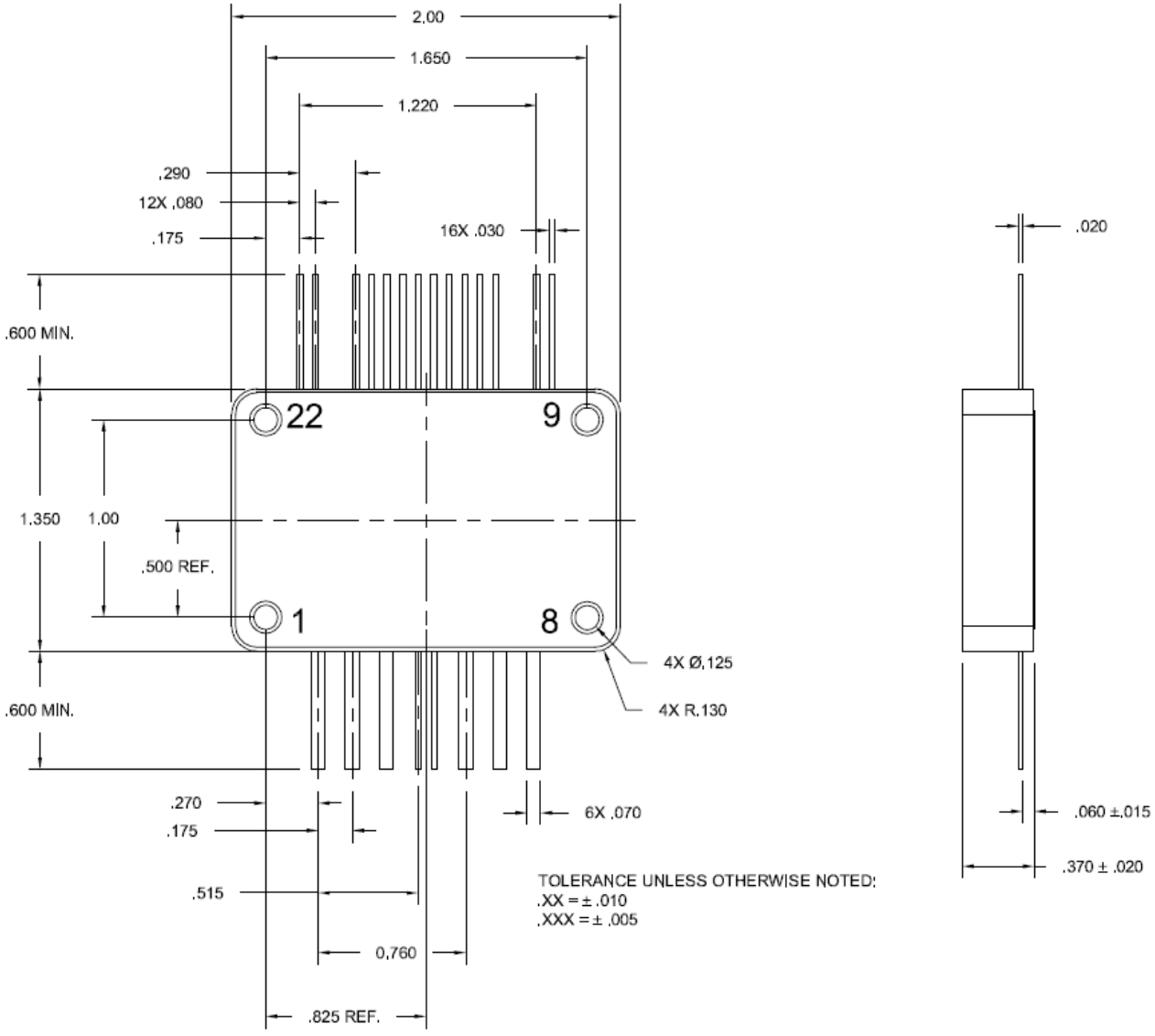
Technical Data
Datasheet 6132, Rev. -

PART NUMBER DESCRIPTION:

- "SPG060C120P2" – Straight Leads
- "SPG060C120P2A" – Surface Mount Lead Formation

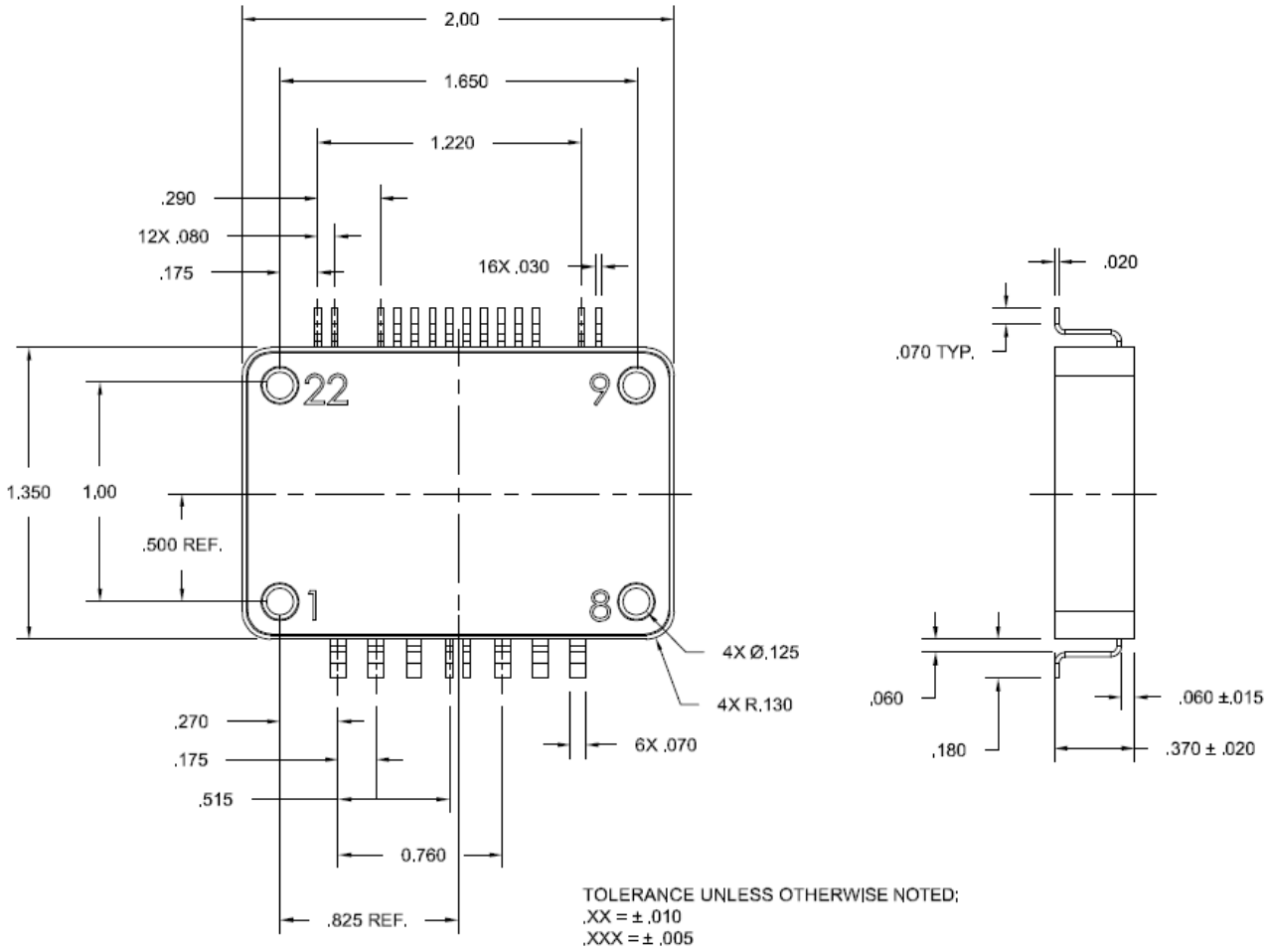
MECHANICAL OUTLINES (inches)

SPG060C120P2



Technical Data
Datasheet 6132, Rev. -

SPG060C120P2A



PINOUTS

Pin 1: V+_1
Pin 2: VO_1
Pin 3: VRTN_1
Pin 4: VDD
Pin 5: VSS
Pin 6: VRTN_2
Pin 7: VO_2
Pin 8: V+_2
Pin 9: VSS2
Pin 10: VDD2
Pin 11: HI2
Pin 12: LI2
Pin 13: EN2
Pin 14: Vis
Pin 15: RTD1
Pin 16: RTD2
Pin 17: Vis_RTN
Pin 18: LI1
Pin 19: HI1
Pin 20: EN1
Pin 21: VSS1
Pin 22: VDD1