HDAS-534,-538
12-Bit, 250 KHz
Data Acquisition Systems

FEATURES

- 12-bit resolution, 250 KHz
- 8 channels single-ended or 4 channels differential
- Miniature 40-pin DDIP
- Full scale gain range from 100 mV to 10V
- Three-state outputs
- No missing codes

GENERAL DESCRIPTION

The HDAS-534/538 are complete data acquisition systems containing an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in a miniature 40-pin double-dip package, the HDAS-534/538 provides 250 KHz throughput with a low power dissipation of 2.6 Watts.

The HDAS-534 provides 4 differential inputs and the HDAS-538 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1,2,4,8,10 and 100. The gain range is selectable through an external resistor.

TECHNICAL NOTES

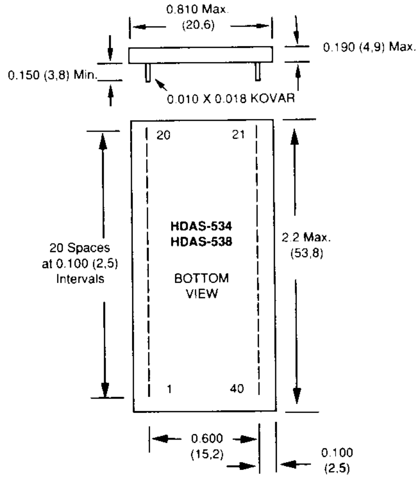
1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the analog, signal and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

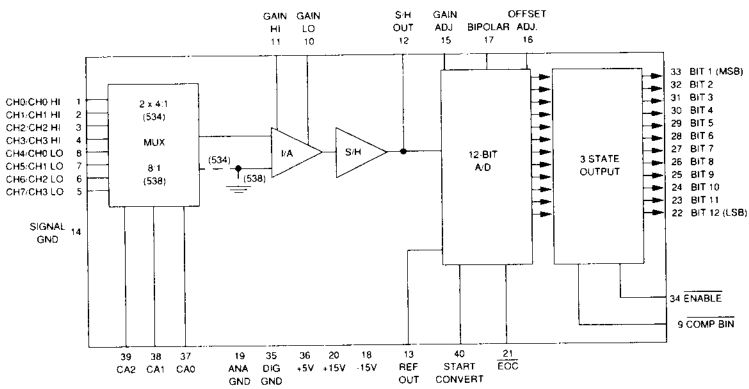
2. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-538 from 8 single-ended channels to 128 single-ended channels or the HDAS-534 from 4 differential channels to 32 single-ended channels.

3. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 9) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 9 to ground. Pin 9 signal is compatible to CMOS/TTL logic levels for logic control of this function.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "0" (low). To disable, connect pin 10 to a logic "1" (high).

MECHANICAL DIMENSIONS INCHES (mm)





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 0/CH 0 HI	40	START CNVRT
2	CH 1/CH 1 HI	39	CA2
3	CH 2/CH 2 HI	38	CA1
4	CH 3/CH 3 HI	37	CA0
5	CH 7/CH 3 LO	36	+5V
6	CH 6/CH 2 LO	35	DIGITAL GND
7	CH 5/CH 1 LO	34	$\overline{\text{ENABLE}}$
8	CH 4/CH 0 LO	33	BIT 1 (MSB)
9	COMP BIN	32	BIT 2
10	RGAIN LO	31	BIT 3
11	RGAIN HI	30	BIT 4
12	S/H OUT	29	BIT 5
13	+10V REF OUT	28	BIT 6
14	SIGNAL GND	27	BIT 7
15	GAIN ADJ	26	BIT 8
16	OFFSET ADJUST	25	BIT 9
17	BIPOLAR	24	BIT 10
18	-15V	23	BIT 11
19	ANALOG GND	22	BIT 12 (LSB)
20	+15V	21	$\overline{\text{EOC}}$

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 20)	0 to +18	V dc
-15V Supply (pin 18)	0 to -18	V dc
+5V Supply (pin 36)	-0.5 to +7.0	V dc
Digital Inputs (pins 34, 37-40)	-0.3 to +6.0	V dc
Analog Inputs (pins 1-8)	±25	V
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-534	4 differential inputs			
HDAS-538	8 single-ended inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V, ±10V			
Gain = 100	0 to 100 mV, ±100 mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Input Impedance				
CH ON, CH OFF	10^{11}	10^{12}	–	Ohms
Input Capacitance				
(534) CH ON, CH OFF	–	–	25	pF
(538) CH ON, CH OFF	–	–	12	pF
Input Bias Current	–	–	200	pA
Input Offset Current	–	–	50	pA
Input Offset Voltage	–	–	±10	mV
Common Mode Volt. Range	±11	–	–	V
CMMR, G=1 ,@ 10 Hz, Vcm=1V p-p	-75	-80	–	dB
Voltage Noise (RMS)				
Gain = 1	–	–	200	µV
Gain = 8	–	–	50	µV
MUX Crosstalk @ 125 KHz	-72	–	–	dB
MUX ON Resistance	–	450	500	Ohms
Bias Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Voltage Tempco	(±30 ppm/ °C x gain) ±20 ppm/ °C (max.)			
Input Gain Equation	Rg = 1/[(gain -1)/2K]			
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	5	µA
Logic 0	–	–	-200	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.9	+10.0	+10.1	V dc
Drift	–	±5	±35	ppm/ °C
External Current	–	–	1.5	mA
Output Coding	Straight binary/Offset binary Complementary binary Complementary offset binary			

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	12	–	–	Bits
Integral Nonlinearity,25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity, +25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1	LSB
F.S. Abs. Accuracy +25 °C	–	±0.13	±0.30	%FSR
0 to +70 °C	–	±0.15	±0.5	%FSR
-55 to +125 °C	–	±0.25	±0.78	%FSR
Unipolar Zero Error,+25 °C	–	±0.074	±0.15	%FSR
Unipolar Zero Tempco	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C	–	±0.074	±0.15	%FSR
Bipolar Zero Tempco	–	±5	±10	ppm/ °C
Bipolar Offset Error,+25 °C	–	±0.1	±0.25	%FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C	–	±0.1	±0.25	%FSR
Gain Tempco	–	±20	±40	ppm/ °C
Harmonic Distortion (- FS) (DC to 50 KHz, 10V pk-pk) [1]	-65	-73	–	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
Enable to Data Val. Delay	–	–	10	nS
MUX Address Set-up Time	400	–	–	nS
Start Convert Pulse Width	125	150	175	nS
Data Valid Before				
$\overline{EOC}$ Signal Goes Low	–	–	20	nS
Conversion Time, +25 °C	–	–	1000	nS
0 to +70 °C, -55 to +125 °C	–	–	1100	nS
Throughput Rates				
Gain= 1, [1]	250	–	–	KHz
Gain = 2, [1]	150	–	–	KHz
Gain = 4, [1]	125	–	–	KHz
Gain = 8, [1]	100	–	–	KHz
Gain = 10, [1]	90	–	–	KHz
Gain = 100, [1]	30	–	–	KHz
S/H PERFORMANCE				
Acquistion Time				
Full Scale Step to 0.01%	–	500	900	nS
Full Scale Step to 0.1%	–	400	750	nS
Aperture Delay	-50	-20	0	nS
Aperture Uncertainty	–	±100	±150	pS
Slew Rate	70	90	–	V/µS
Hold Mode Settling Time,				
10V to ±0.01%FS	–	100	200	nS
10V to ±0.1%FS	–	75	150	nS
Feedthrough Rejection	-80	-88	–	dB
Droop Rate, [1]	–	0.1	100	µV/µS
POWER SUPPLY				
Range, +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current, +15V	–	+78	+90	mA
-15V	–	-72	-82	mA
+5V	–	+75	+90	mA
Power Dissipation	–	2.6	3.0	Watts
Power Supply Rejection	–	–	0.01%	%FSR/ %V
ENVIRONMENTAL				
Oper. Temp. Range, -MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin DDIP			
Weight	0.32 oz./(9 grams) max.			
Pins	0.010 x 0.018 in. Kovar			

[1] Specifications valid at 25 °C and over the operating temperature ranges of 0 to +70 °C and -55 to +125 °C.

HDAS-534/538 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to SIGNAL GROUND, pin 14.

Channel selection is accomplished using the multiplexer address pins shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy.

The acquisition time can be measured by how long $\overline{EOC}$ is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the RGAIN resistor to increase the acquisition time. The gain is equal to 1 without an RGAIN resistor. Table 2 refers to the appropriate RGAIN resistors for various throughputs.

The HDAS devices enter the hold mode and are ready for conversion upon the start convert going high. The conversion is complete within a maximum of 1 µsec (+25°C). $\overline{EOC}$ returns low, the data is valid and sent to the three-state output buffers. The sample/hold is now ready to acquire new data.

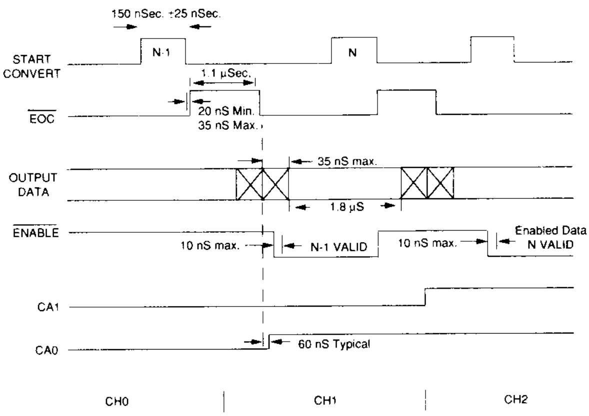


Figure 1. HDAS-534/538 Timing Diagram

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 39 CA2	38 CA1	37 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-534
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-538
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

Table 2. Input Range Parameters

INPUT RANGE	GAIN	RGAIN ( )	THROUGHPUT
0 to +10V	1	OPEN	250 KHz
0 to +5V	2	2K	150 KHz
0 to +2.5V	4	665 Ω	125 KHz
0 to +1.25V	8	287 Ω	100 KHz
0 to +1.0V	10	221 Ω	90 KHz
0 to +100mV	100	20 Ω	30 KHz
±10V	1	OPEN	250 KHz
±5V	2	2K	150 KHz
±2.5V	4	665 Ω	125 KHz
±1.25V	8	287 Ω	100 KHz
±1.0V	10	221 Ω	90 KHz
±100mV	100	20 Ω	30 KHz

$$\frac{1}{\left[\frac{(gain - 1)}{2K}\right]}$$

Notes

1. A START CONVERT pulse greater than 175 nanoseconds will slow the throughput.
2. Retriggering START CONVERT before EOC goes low will not start a new conversion.
3. Times shown apply over the full operating temperature range.

Table 3. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV	+9.9963V dc
±10V dc	+2.44 mV dc	+9.9927V dc

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 150 nSec (typical) to the START CONVERT input (pin 40) at a rate of 75 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments

Apply a precision voltage reference source between the analog input and signal ground (pin 14). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 9) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with pin 9 tied low (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 9 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 9 tied low (complementary offset binary).

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 9 tied high and 0000 0000 0001 and 0000 0000 0000 for pin 9 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

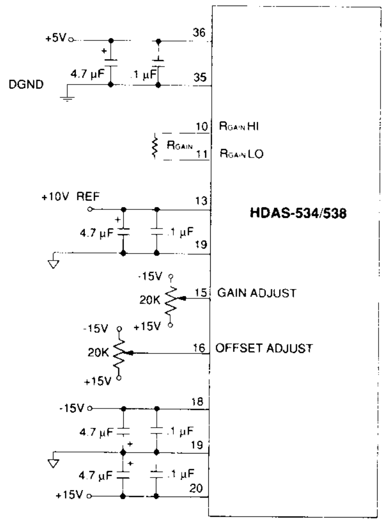


Figure 2. Typical Connection Diagram

NOTES:

1. For unipolar operation, connect pin 12 to pin 17.
2. For bipolar operation, connect pin 13 to pin 17.
3. Position RGAIN as close as possible to pins 10 and 11. Use RN55C, 1% resistors.
4. If gain and offset adjusts are not used connect pin 15 to ground and leave pin 16 open.

Table 4. Output Coding

UNIPOLAR SCALE	INPUT RANGES, V dc 0 to +10V	OUTPUT CODING MSB LSB (STRAIGHT BIN. / OFF. BINARY)	MSB LSB (COMP. BINARY / COMP. OFF. BIN.)	INPUT RANGE ±10V dc	BIPOLAR SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000	1011 1111 1111	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000	1101 1111 1111	-7.5000V	-3/4 FS
1 LSB	+0.0024V	0000 0000 0001	1111 1111 1110	-9.9951V	-FS +1 LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	-10.000V	-FS

ORDERING INFORMATION

MODEL NO.	INPUT	OPER. TEMP. RANGE	SEAL
HDAS-534MC	4 D Channels	0 to +70 °C	Hermetic
HDAS-534MM	4 D Channels	-55 to +125°C	Hermetic
HDAS-538MC	8 SE Channels	0 to +70° C	Hermetic
HDAS-538MM	8 SE Channels	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc.,Part # 3-331272-8 (Component Lead Socket), 40 required.

For availability of MIL-STD-883B versions, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356