PRELIMINARY INFORMATION

TC1321

# 10-Bit Digital-to-Analog Converter with Two-Wire Interface

## FEATURES

- 10-Bit Digital-Analog Converter
- 8-Pin SOIC and 8-Pin MSOP Packages
- 2.7–5.5V Single-Supply Operation
- Simple SMBUS/I²C Serial Interface
- Low Power - 0.35mA Operation, 5µA Shutdown
- Guaranteed Monotonicity

## TYPICAL APPLICATIONS

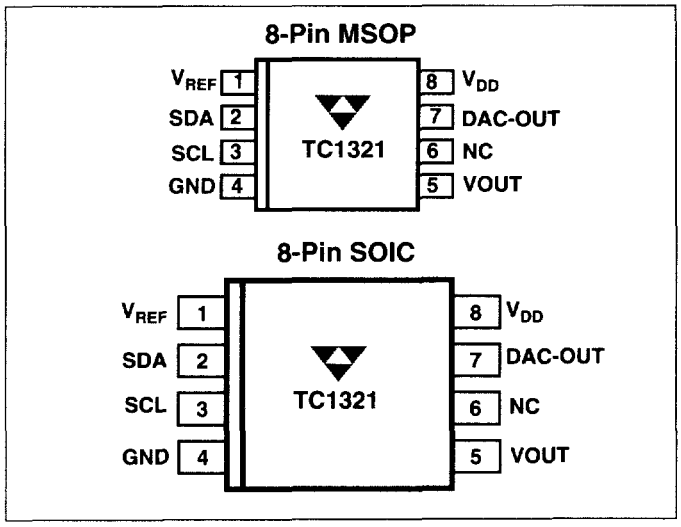
- Programmable Voltage Sources
- Digital-Controlled Amplifiers/Attenuators
- Process Monitoring and Control
- Microprocessor- controlled systems

## GENERAL DESCRIPTION

The TC1321 is a serially accessible 10-bit voltage output digital-to-analog converter (DAC). The DAC produces an output voltage that ranges from ground to an externally supplied reference voltage. It operates from a single power supply that can range from 2.7V to 5.5V, making it ideal for a wide range of applications. Built into the part is a power-on reset function that ensures that the device starts at a known condition.

Communication with the TC1321 is accomplished via a simple 2-wire SMBus/I²C compatible serial port with the TC1321 acting as a slave only device. The host can enable the SHDN bit in the CONFIG register to activate the low-power standby mode.

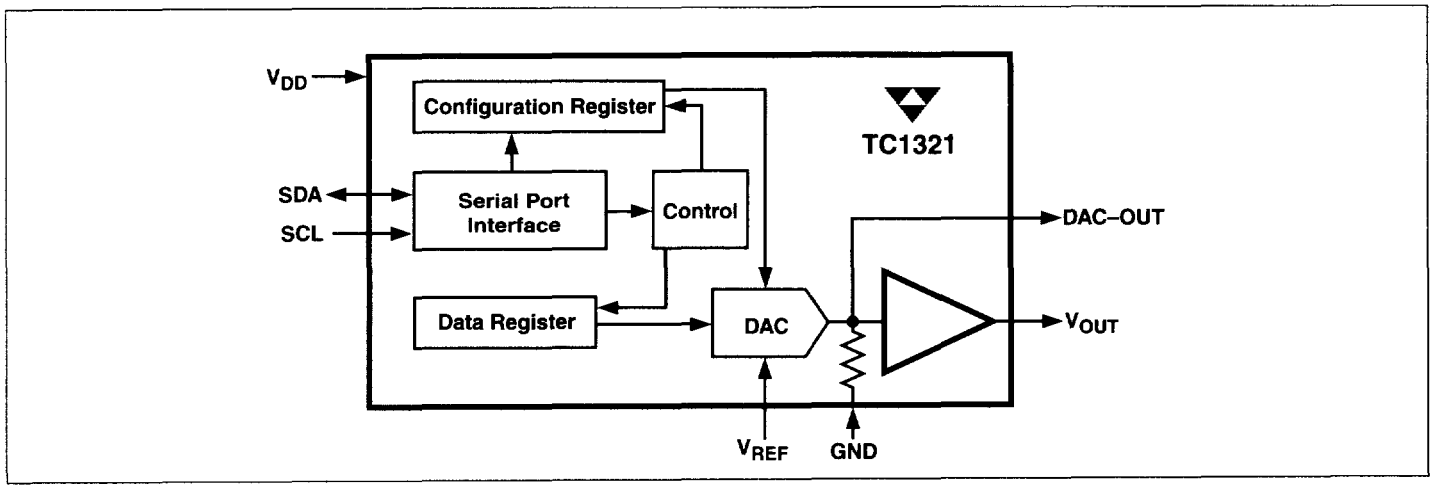
## PIN CONFIGURATION




## ORDERING INFORMATION

| Part No. | Package | Temp. Range |
|---|---|---|
| TC1321VOA | 8-Pin SOIC | –40°C to +85°C |
| TC1321VUA | 8-Pin MSOP | –40°C to +85°C |

## FUNCTIONAL BLOCK DIAGRAM



## TC1321

## PRELIMINARY INFORMATION

### ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ($V_{DD}$) ..... +6V
Voltage On Any Pin ..... (GND – 0.3V) to ($V_{DD}$ + 0.3V)
Operating Temperature ($T_A$) ..... See Below
Storage Temperature ($T_{STG}$) ..... – 65°C to +150°C
Current On Any Pin ..... ±50 mA
Package Thermal Resistance ($\theta_{JA}$) ..... 330°C/W

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS: $V_{DD}$ = 2.7V or 5.5V, – 40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{DD}$ | Supply Voltage | | 2.7 | — | 5.5 | V |
| $I_{DD}$ | Operating Current | $V_{DD}$ = 5.5V, $V_{REF}$ = 1.2V<br>Serial Port Inactive (Note 1) | — | 0.35 | 0.5 | mA |
| $I_{DD-STANDBY}$ | Standby Supply Current | $V_{DD}$ = 3.3V<br>Serial Port Inactive (Note 1) | — | 5 | 10 | µA |

### STATIC PERFORMANCE–ANALOG SECTION: ($V_{DD}$ = 2.7V to 5.5V, $V_{REF}$ = 1.2V, –40°C ≤ $T_A$ ≤ 85°C, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Resolution | | 8 | — | — | Bits |
| INL | Integral Non-Linearity at FS Error (Gain Error) | | — | — | ±2 | LSB |
| DNL | Differential Non-Linearity | All Codes (Note 2) | — | — | ±0.8 | LSB |
| $V_{OS}$ | Offset Error at $V_{OUT}$ | (Note 2) | | ±0.3 | ±8 | mV |
| $TCV_{OS}$ | Offset Error Tempco at $V_{OUT}$ | | | 6 | | ppm/°C |
| PSRR | Power Supply Rejection Ratio | $V_{DD}$ at DC | 70 | — | — | dB |
| $V_{REF}$ | Voltage Reference Range | | 0 | — | $V_{DD}$ – 1.2 | V |
| $I_{REF}$ | Reference Input Leakage Current | | | | 0.5 | µA |
| $V_{SW}$ | Voltage Swing | $V_{REF}$ ≤ ($V_{DD}$ – 1.2V) | 0 | | $V_{REF}$ | V |
| $R_{OUT}$ | Output Resistance @ $V_{OUT}$ | $R_{OUT}$ (ohmic) | — | — | 5.0 | |
| $I_{OUT}$ | Output Current (Source or Sink) | | 3 | — | — | mA |
| $I_{SC}$ | Output Short-Circuit Current | Source<br>Sink | —<br>— | —<br>— | 40<br>40 | mA<br>mA |

**NOTES:** 1. SDA and SCL must be connected to $V_{DD}$ or GND.
2. Measured at $V_{OUT}$ ≥ 50mV refered to GND to avoid output buffer clipping.

## PRELIMINARY INFORMATION — TC1321

### DYNAMIC PERFORMANCE: ($V_{DD}$ = 2.7V to 5.5V, –40°C ≤ $T_A$ ≤ 85°C, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SR | Voltage Output Slew Rate | | — | 0.8 | — | V/µs |
| $t_{SETTLE}$ | Output Voltage Full Scale Settling Time | | — | 10 | — | µsec |
| $t_{WU}$ | Wake-up Time | | — | 20 | — | µs |
| | Digital Feedthrough and Crosstalk | SDA = $V_{DD}$, SCL = 100kHz | — | 5 | — | nV-s |

### SERIAL PORT INTERFACE: ($V_{DD}$ = 2.7V to 5.5V, –40°C ≤ $T_A$ ≤ 85°C, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic Input High | | 2.4 | — | 5.5 | V |
| $V_{IL}$ | Logic Input Low | | — | — | 0.6 | V |
| $V_{OL}$ | SDA Output Low | $I_{OL}$ = 3 mA (Sinking Current)<br>$I_{OL}$ = 6 mA | —<br>— | —<br>— | 0.4<br>0.6 | V<br>V |
| $C_{IN}$ | Input Capacitance SDA, SCL | | — | 5 | — | pF |
| $I_{LEAK}$ | I/O Leakage | | — | — | ±5 | µA |

### SERIAL PORT AC TIMING: $V_{DD}$ = 2.7V or 5.5V, –40°C ≤ ($T_A$ = $T_J$) ≤ 85°C; $C_L$ = 80pF, unless otherwise noted.)

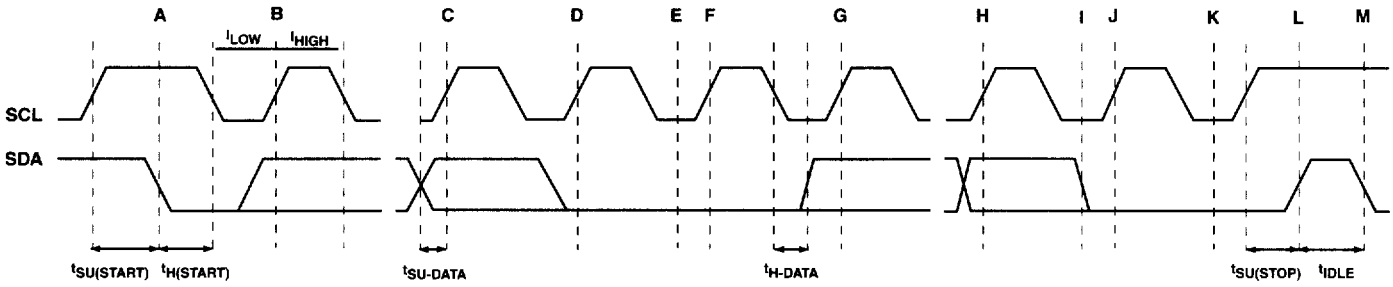
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SMB}$ | SMBus Clock Frequency | | 10 | — | 100 | kHz |
| $t_{IDLE}$ | Bus Free Time Prior to New Transition | | 4.7 | — | — | µsec |
| $t_{H(START)}$ | Start Condition Hold Time | | 4.0 | — | — | µsec |
| $t_{SU(START)}$ | Start Condition Setup Time | 90% SCL to 10% SDA (for repeated Start Condition) | 4.7 | — | — | µsec |
| $t_{SU(STOP)}$ | Stop Condition Setup Time | | 4.0 | — | — | µsec |
| $t_{H-DATA}$ | Data In Hold Time | | 100 | — | — | nsec |
| $t_{SU-DATA}$ | Data In Setup Time | | 100 | — | — | nsec |
| $t_{LOW}$ | Low Clock Period | 10% to 10% | 4.7 | — | — | µsec |
| $t_{HIGH}$ | High Clock Period | 90% to 90% | 4 | — | — | µsec |
| $t_F$ | SMBus Fall Time | 90% to 10% | — | — | 300 | nsec |
| $t_R$ | SMBus Rise Time | 10% to 90% | — | — | 1000 | nsec |
| $t_{POR}$ | Power-On Reset Delay | $V_{DD}$ ≥ $V_{POR}$ (Rising Edge) | — | 500 | — | µsec |

### PIN DESCRIPTION

| Pin No. | Symbol | Type | Description |
|---|---|---|---|
| 1 | $V_{REF}$ | Input | Voltage Reference Input |
| 2 | SDA | Bi-Directional | SMBUS Serial Data |
| 3 | SCL | Input | SMBUS Serial Clock |
| 4 | GND | Input | System Ground |
| 5 | VOUT | Output | Buffered DAC Output |
| 6 | NC | None | Not Connected |
| 7 | DAC_OUT | Output | Unbuffered DAC Output |
| 8 | $V_{DD}$ | Power | Positive Power Supply Input |

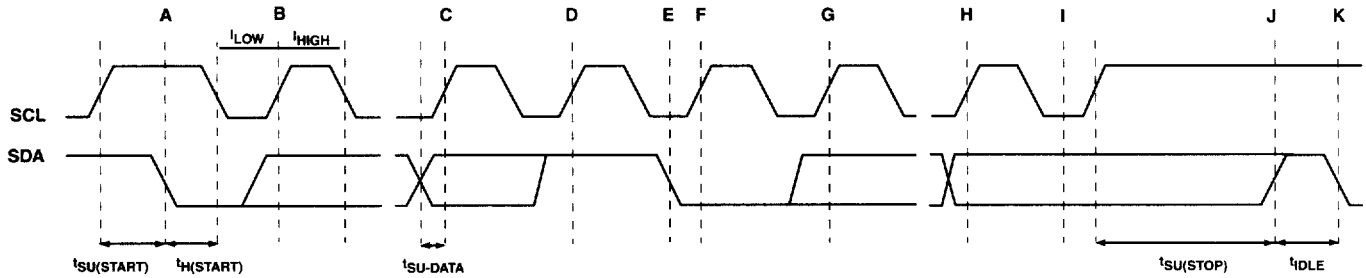
### TIMING DIAGRAMS

#### SMBUS Write Timing Diagram




A = Start Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/W Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Slave
H = LSB of Data Clocked into Slave
I = Slave Pulls SDA Line Low
J = Acknowledge Clocked into Master
K = Acknowledge Clock Pulse
L = Stop Condition, Data Executed by Slave
M = New Start Condition

#### SMBUS READ Timing Diagram

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E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Master
H = LSB of Data Clocked into Master
I = Acknowledge Clock Pulse
J = Stop Condition
K = New Start Condition