Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice. Please consult Brooktree regarding the most updated datasheet before design.

Bt467

230 MHz
Monolithic CMOS
256-Color Palette
RAMDAC™

Distinguishing Features

- 230, 170, 135 MHz Operation
- 8:1 Multiplexed TTL Pixel Ports
- Register Compatibility with Bt458
- 256-Word Dual-Port Color Palette
- 4-Word Dual-Port Overlay Palette
- RS-343A-Compatible Outputs
- Bit Plane Read and Blink Masks
- Programmable Offset
- Standard MPU Interface
- 145-pin PGA Package
- +5 V CMOS Monolithic Construction

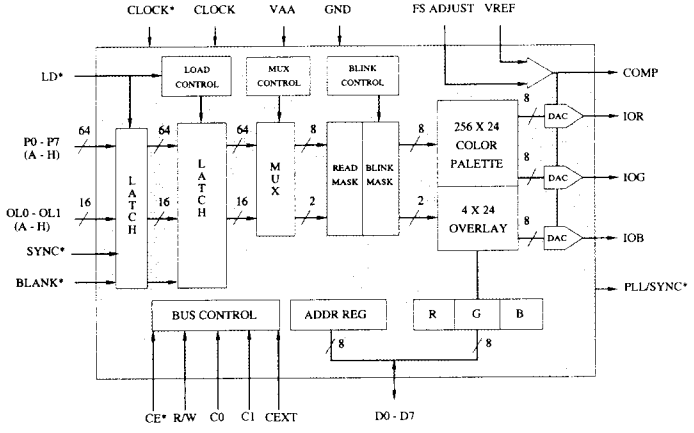
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439, Bt458

Functional Block Diagram



Product Description

The Bt467 is designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1600 x 1280 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information). This minimizes the requirements for costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The 8:1 multiple pixel ports and internal multiplexing enable TTL-compatible interface (up to 29 MHz) to the frame buffer, while maintaining the 230-MHz video data rates required for 76 Hz systems.

The Bt467 contains a 256 x 24 color lookup table with triple 8-bit video D/A converters. The Bt467 is also register-compatible with the Bt458, providing Bt458 software/device driver compatibility. In addition, extended registers are optional, providing such features as testability enhancements, sync output, and pedestal option. The Bt467 has 0 IRE setup with no composite sync on the green channel. An output is provided for either separate sync or PLL for synchronization.

On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt467 generates RS-343A-compatible red, green, and blue and can drive doubly-terminated 75 Ω coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt467 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay RAM allow color updating without contention with the display refresh process.

As shown in Table 1, the C0, C1, and CEXT control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay RAM will be accessed by the MPU. CEXT is used to specify Bt458 register compatibility or access to the extended register set.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Bt467 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay RAM to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay RAM to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay RAM. Following the blue read cycle, the address register increments to the next location, which the MPU may read by reading another sequence of red, green, and blue data.

ADDR0–7	CEXT	C1	C0	Addressed by MPU
$xx	X	0	0	address register
$00–$FF	X	0	1	color palette RAM
$00	X	1	1	overlay color 0
$01	X	1	1	overlay color 1
$02	X	1	1	overlay color 2
$03	X	1	1	overlay color 3
$00	X	1	0	ID Register ($80)
$01	X	1	0	Revision Register
$02	X	1	0	reserved ($00)
$03	X	1	0	reserved ($00)
$04	X	1	0	read mask register
$05	X	1	0	blink mask register
$06	X	1	0	command register
$07	X	1	0	test register
$08	1	1	0	command register 1
$09	1	1	0	command register 2
$0A	1	1	0	reserved ($00)
$0B	1	1	0	test register 1
$0C	1	1	0	red signature
$0D	1	1	0	green signature
$0E	1	1	0	blue signature
$0F	1	1	0	reserved ($00)

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay Register 3. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. In the Bt458 register-compatibility mode, the MPU does not have access to these bits. However, in the extended register mode, the modulus three is accessible as read-only register bits through Command Register 1. This provides the state of these 2 bits after the last color was loaded. These 2 bits provide the state of the read/write cycle after the last color is loaded.

Additional Information

Although the color palette RAM and overlay registers are dual ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU during the write cycle, 1 or more of the pixels on the display screen may be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers can also be accessed through the address register in conjunction with the C0, C1, and CEXT inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU. Figure 1 illustrates the MPU read/write timing of the Bt467.

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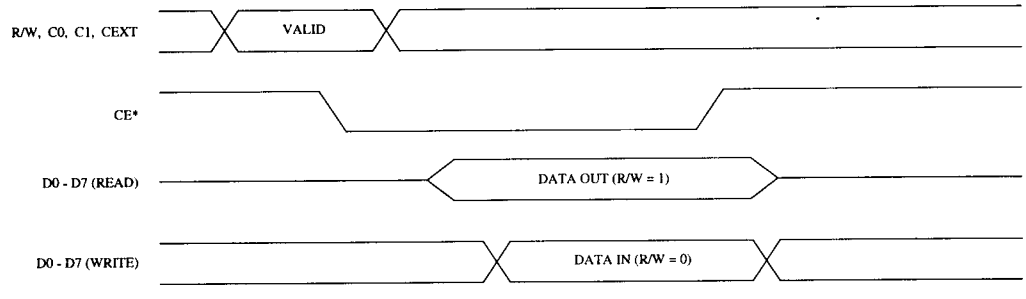

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable the transfer of pixel data from the frame buffer at TTL data rates, the Bt467 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color information (up to 8 bits per pixel), and overlay information (up to 2 bits per pixel), for 8 consecutive pixels, are latched into the device. With this configuration, the sync and blank timing will be recognized only with 8-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

At each clock cycle, the Bt467 outputs color information based on the {A} inputs, followed by the {B} inputs, followed by the {C} inputs, etc., until all 8 pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis. Or, they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK.

This enables the LD* signal to be derived by externally dividing CLOCK by eight, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than eight clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

Only one rising edge of LD* should occur every eight clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

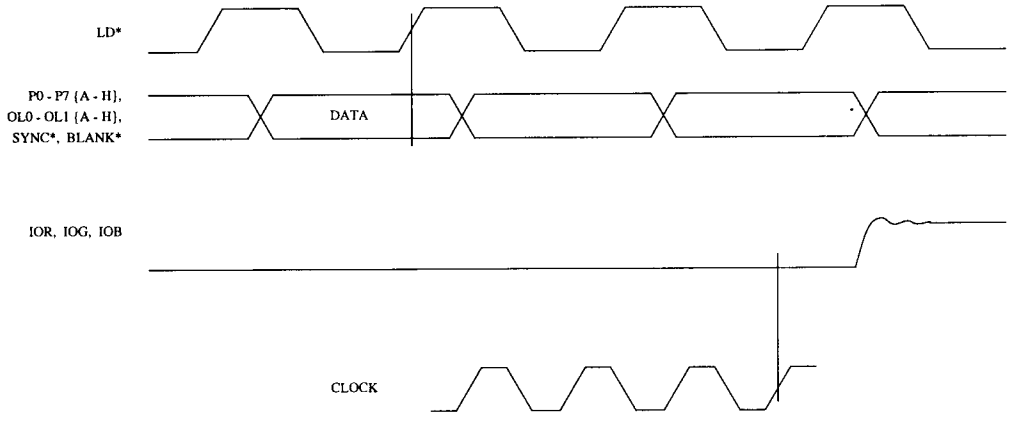

Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

At each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. These registers are not initialized. They must be initialized by the user after power up for proper operation. Through the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change caused by blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt467 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval occurs when BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAM. Table 2 is the truth table used for color selection.

Video Generation

At every clock cycle, the selected color information from the color palette RAMs or overlay registers is presented to the D/A converters.

The BLANK* input, pipelined to maintain synchronization with the pixel data, adds an appropriately-weighted current to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Tables 3–6 detail how the BLANK* input modifies the output levels.

The D/A converters on the Bt467 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

The Bt467 does not have a sync current source on the green channel (IOG) as does the Bt458. However, to generate a sync on green (IOG), the PLL/sync signal can be programmed to generate sync current. Sync on green can be generated by tying the IOG and PLL/Sync output signals together. This combination will supply the appropriate sync current (see Figures 5 and 6). This output signal combination should be properly terminated to ground through a 75 Ω resistor.

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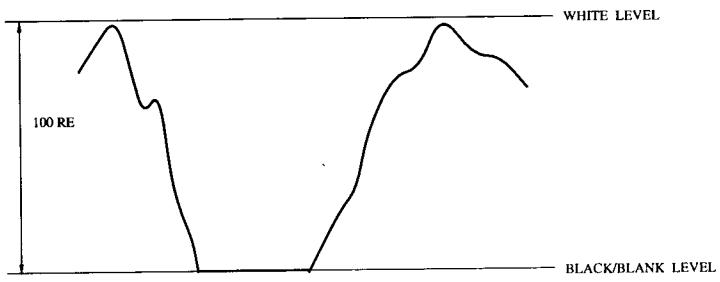
CR06	OL1	OL0	P0–P7	Addressed by frame
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

IOR, IOG, IOB	
MA	V
19.05	0.714
0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Figure 3. Composite Video Output Waveform (SETUP = 0 IRE).

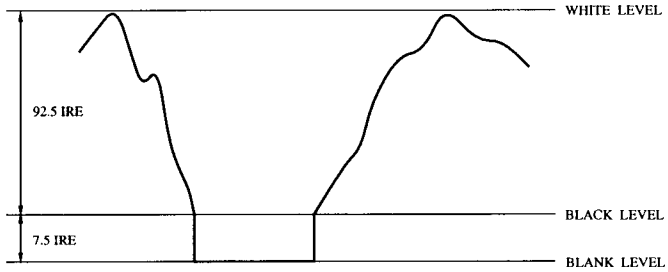
Description	IOR, IOG, IOB (mA)	BLANK*	DAC Input Data
WHITE	19.05	1	$FF
DATA	data	1	data
BLACK	0	1	$00
BLANK	0	0	$xx

Note: Typical with full-scale IOG = 19.05 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Table 3. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

IOR, IOG, IOB	
MA	V
19.05	0.714
1.44	0.054
0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Figure 4. Composite Video Output Waveform (SETUP = 7.5 IRE).

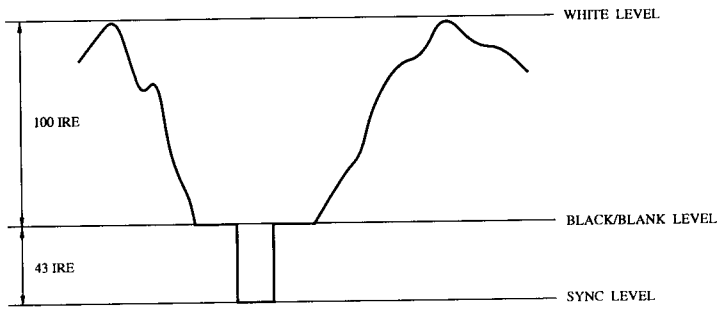
Description	IOR, IOG, IOB (mA)	BLANK*	DAC Input Data
WHITE	19.05	1	$FF
DATA	data + 1.44	1	data
BLACK	1.44	1	$00
BLANK	0	0	$xx

Note: Typical with full-scale IOG = 19.05 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. For full-scale voltage of 0.700 V, RSET = 495 Ω.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 5. Composite Video Output Waveform (SETUP = 0 IRE) PLL/SYNC Externally Tied To IOG.

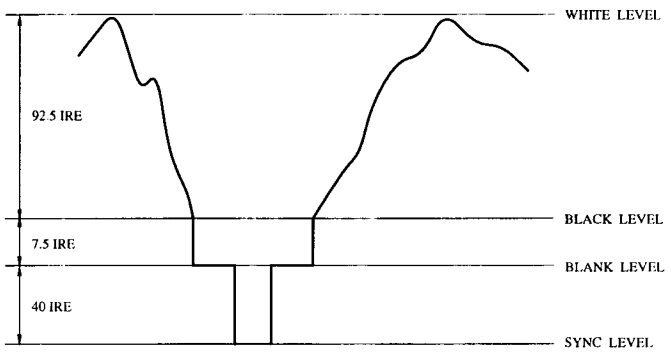
Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 487 Ω, and VREF = 1.235 V. RS-343A levels and tolerances are assumed on all levels.

Figure 6. Composite Video Output Waveform (SETUP = 7.5 IRE) PLL/SYNC Externally Tied To IOG.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 487 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. This register is not initialized. It must be initialized by the user after power up for proper operation. CR0 corresponds to data bus bit D0.

CR07 Multiplex select

(0) 8:1 multiplexing
(1) 8:1 multiplexing

It is only possible to set the pipeline delay of the Bt467 to a fixed 8-clock cycle.

CR06 RAM enable

(0) use overlay color 0
(1) use color palette RAM

When the overlay display bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.

CR05, CR04 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).

CR03 OL1 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL1 {A–H} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the values of the OL1 {A–H} inputs. In order for overlay 1 bit plane to blink, bit CR01 must be set to a logical one.

CR02 OL0 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL0 {A–H} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the values of the OL0 {A–H} inputs. In order for overlay 0 bit plane to blink, bit CR00 must be set to a logical one.

CR01 OL1 display enable

(0) disable
(1) enable

If a logical zero, this bit forces the OL1 {A–H} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the values of the OL1 {A–H} inputs.

CR00 OL0 display enable

(0) disable
(1) enable

If a logical zero, this bit forces the OL0 {A–H} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the values of the OL0 {A–H} inputs.

Internal Registers (continued)

Command Register 1

The command register may be written to or read by the MPU at any time and is not initialized. This register is not initialized. It must be initialized by the user after power up for proper operation. CR10 corresponds to data bus bit D0.

CR17, CR16	Address counters (0,0) red (0,1) green (1,0) blue (1,1) undefined	This is a read-only register bit that specifies the location of the modulus a,b addresses. This is useful to determine the last location written to during the load of the palette RAM. These bits are read only.
CR15	reserved (logical zero)	
CR14	reserved (logical zero)	
CR13	reserved (logical zero)	
CR12	reserved (logical zero)	
CR11	reserved (logical zero)	
CR10	reserved (logical zero)	

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Internal Registers (continued)

Command Register 2

The command register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power up for proper operation. CR20 corresponds to data bus bit D0.

CR27 — reserved (logical zero)

CR26 — Pedestal enable

(0) 0 IRE pedestal
(1) 7.5 IRE pedestal

This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.

CR25, CR24 — Load palette RAM select

(00) normal
(01) red RAMDAC
(10) green RAMDAC
(11) blue RAMDAC

If (00) is specified, color data is loaded into the Bt467 using three write cycles (red, green, and blue). Color data is output using three read cycles (red, green, and blue).

Modes (01), (10), and (11) enable the Bt467 to emulate a single-channel RAMDAC using only the green channel. The Bt467 expects color data to be input and output using (red, green, blue) cycles. The exact value indicates during which one of the three color cycles the Bt467 is to load or output color information. The value is loaded into or read from the green color palette RAM.

CR23 — PLL generate

(0) SYNC*
(1) BLANK*

This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.

CR22 — PLL/SYNC

(0) disable
(1) enable

If (0) is specified, the PLL/SYNC output is disabled. If (1) is specified, the PLL/SYNC output is enabled, and CR21 should be used to select PLL or SYNC.

CR21 — PLL/SYNC select

(0) PLL
(1) SYNC

If (0) is specified, PLL/SYNC outputs PLL current. CR23 should be used to select SYNC or BLANK to generate the PLL information. If (1) is specified, PLL/SYNC outputs SYNC current.

CR20 — Test mode select

(0) signature analysis test
(1) data strobe test

This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–H}), and D7 correspond to bit plane 7 (P7 {A–H}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power up for proper operation.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A–H}), and D7 corresponds to bit plane 7 (P7 {A–H}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power up for proper operation.

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt467, the value read by the MPU will be $80. Data written to this register is ignored. If this location is read from the Bt458, the value returned will be $00.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt467. If this location is read from the Bt458, the value returned will be $01. The 4 most significant bits signify the revision letter in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored. For the Bt467, the value read by the MPU will be $B2.

Reserved Register ($02 and $03)

These registers are not identically compatible with the Bt458. For the Bt467, if these registers are read, they will return a value of ($00) to the data bus. For the Bt458, if these same locations are read, the data present on the data bus will be returned.

Internal Registers (continued)

Bt467 Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	Color Information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting *only one* of the (red, green, blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the (red, green, blue, low, or high nibble) enable information previously written. Either the CLOCK must be slowed to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits and D0–D3 containing (red, green, blue, low, or high nibble) enable information, as listed below.

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Internal Registers (continued)

Signature Registers (Signature Mode)

In the active mode, the signature register operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs.

The SARs act as a 24-bit-wide linear feedback shift register on each succeeding pixel that is latched. *In 8:1 multiplexed mode, the SARs only latch 1 pixel per load group.* Thus, the SARs are operating only on every eighth pixel in the multiplexed mode. The user determines which pixel phase (A, B, C, D, E, F, G, or H) is latched to generate new signatures by setting bits D0–D2 in Test Register 1.

The Bt467 will generate signatures only while it is in "active-display" (BLANK* negated). The SARs are available for reading and writing by the MPU port when the Bt467 is in a blanking state (BLANK* asserted). It is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan-line or one frame buffer's worth of pixels, will be input to the chip. Then, at the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay data validity is also tested with the signature registers.

The Bt467 linear feedback configuration is shown in Figure 7.

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Signature Registers (Data-Strobe Mode)

Setting command bit CR20 to a logic one puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt467. The levels of most inputs do not matter *except* that CLOCK should be high and CLOCK* should be low. Then, the user can read the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

In general, the color read-out will correspond to a pixel latched on the previous load. However, because the data path is pipelined, the color may come from an earlier load cycle. To read successive pixels, LD* should be toggled, the CLOCK pins should be pulsed according to the mux state, and all pixel-related inputs should then be held and the three MPU reads should be performed as described. This process is best done on a sophisticated VLSI semiconductor tester.

Internal Registers (continued)

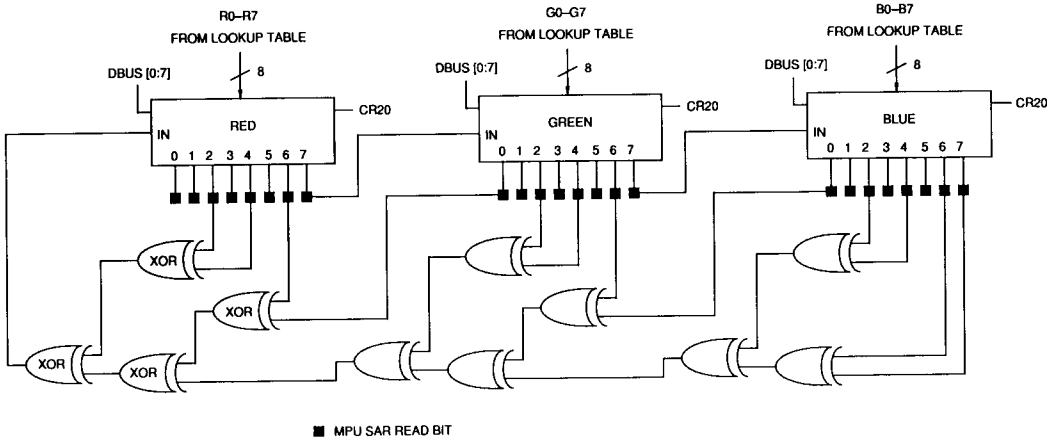


Figure 7. Signature Analysis Register Circuit.

Internal Registers (continued)

Test Register 1

This 8-bit register is used to test the Bt467. Signature analysis is performed on every eighth pixel. D0–D2 are used for 8:1 multiplexing to specify whether the A, B, C, D, E, F, G, or H pixel inputs are to be used, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	pixel F
110	pixel G
111	pixel H

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	–	–
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The output levels of the DACs should be constant for 5 µS to allow enough time for detection. The capture occurs over one LD* period set by a logical one at any of the pixel pins.

For normal operation, D3–D7 must be logical zeros.

Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>BLANK*</td><td>Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.</td></tr>
<tr><td>SYNC*</td><td>Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the PLL/SYNC output (see Figures 5 and 6). SYNC* does not override any other control or data input, as shown in Tables 5 and 6; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.</td></tr>
<tr><td>LD*</td><td>Load control input (TTL compatible). The P0–P7 {A–H}, OL0–OL1 {A–H}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD* may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.</td></tr>
<tr><td>P0–P7
{A–H}</td><td>Pixel select inputs (TTL compatible). These inputs are used to specify on a pixel basis which one of the 256 entries in the color palette RAM is to be used to provide color information. Eight consecutive pixels are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.

The {A} pixel is output first, followed by the {B} pixel, followed by the {C} pixel, etc., until all 8 pixels have been output, at which point the cycle repeats.</td></tr>
<tr><td>OL0–OL1
{A–H}</td><td>Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD* and, in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:
<table>
<tr><th>OL1</th><th>OL0</th><th>CR06 = 1</th><th>CR06 = 0</th></tr>
<tr><td>0</td><td>0</td><td>color palette RAM</td><td>overlay color 0</td></tr>
<tr><td>0</td><td>1</td><td>overlay color 1</td><td>overlay color 1</td></tr>
<tr><td>1</td><td>0</td><td>overlay color 2</td><td>overlay color 2</td></tr>
<tr><td>1</td><td>1</td><td>overlay color 3</td><td>overlay color 3</td></tr>
</table>
When accessing the overlay palette, the P0–P7 {A–H} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for 8 consecutive pixels are input through this port. Unused inputs should be connected to GND.</td></tr>
<tr><td>IOR, IOG, IOB</td><td>Red, green, and blue video current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figure 5).</td></tr>
<tr><td>PLL/SYNC*</td><td>Phase lock loop current output. This high-impedance current source is used to enable synchronization of multiple Bt467s with subpixel resolution when used with an external PLL. This function is accessible through the extended command registers. A logical one on the BLANK* input results in no current output onto this pin, while a logical zero results in the following current output:

PLL (mA) = 3,227 * VREF (V) / RSET (Ω)

If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor of up to 150 Ω). The Bt467 does not have a SYNC current source on the green channel (IOG) as does the Bt458. However, to generate a SYNC on green (IOG), the PLL/SYNC signal can be programmed to generate SYNC current. SYNC can be generated by tying the IOG and PLL/SYNC output signals together. This combination will supply the appropriate SYNC current (see Figures 5 and 6). This output signal combination should be properly terminated to ground through a 75 Ω resistor.</td></tr>
</table>

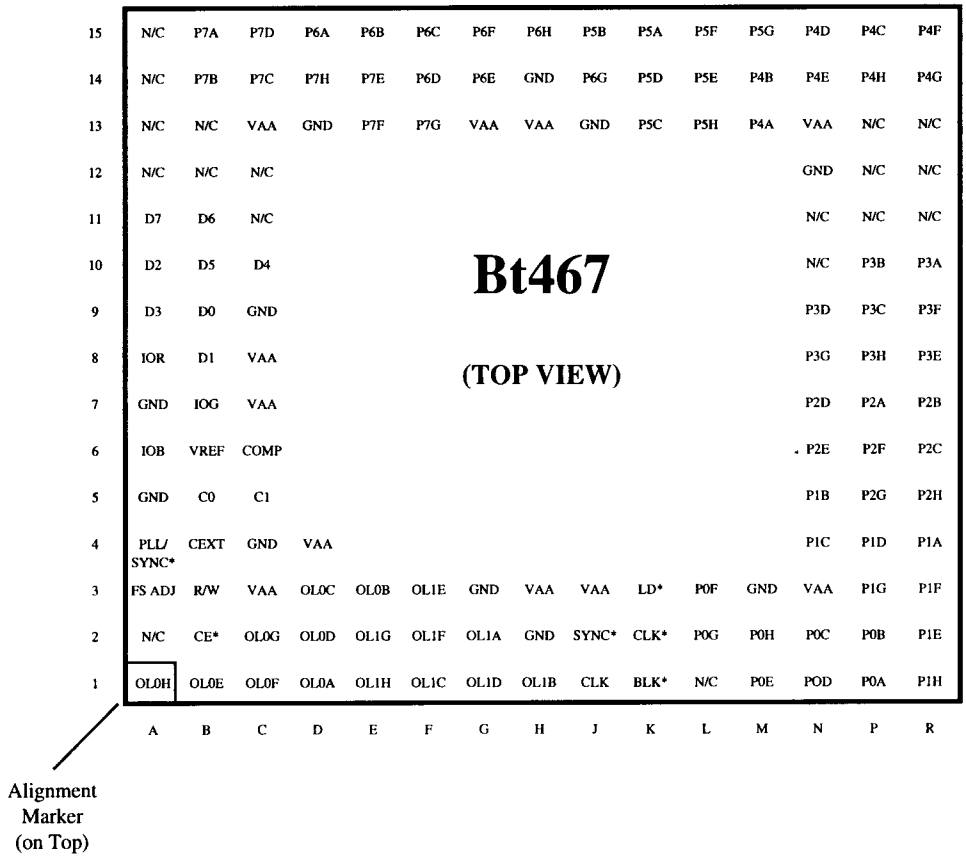
Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (see Figure 8 in the PC Board Layout Considerations section). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and to maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to PC board layout considerations for critical layout criteria.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (see Figure 8). The IRE relationships in Figures 3–6 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = 10,684* VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOG, IOB, (mA) = 7,457* VREF (V) / RSET (Ω)
VREF	Voltage reference input. An external voltage reference circuit must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum (see Figure 8.)
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1, CEXT	Command control inputs (TTL compatible). C0, C1, and CEXT specify the type of read or write operation being performed, as shown in Table 1. CEXT provides the control input for Bt458 register compatibility or access to the extended register set. These Inputs are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions (continued)

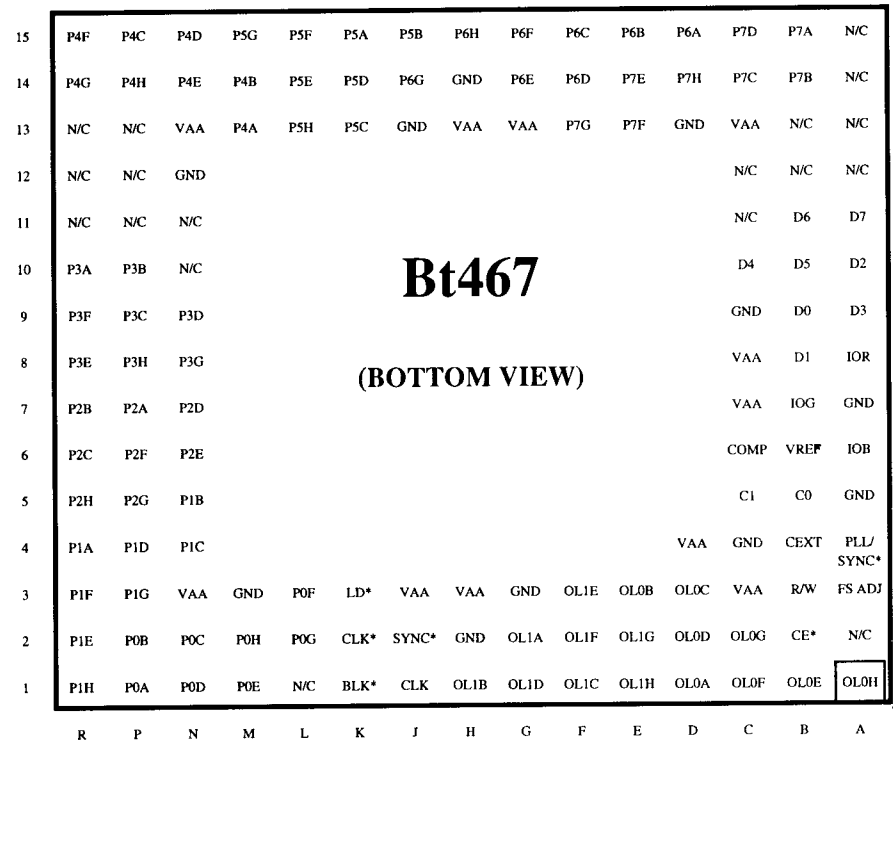
Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	K1	P5A	K15	D0	B9
SYNC*	J2	P5B	J15	D1	B8
LD*	K3	P5C	K13	D2	A10
CLOCK	J1	P5D	K14	D3	A9
CLOCK*	K2	P5E	L14	D4	C10
		P5F	L15	D5	B10
P0A	P1	P5G	M15	D6	B11
P0B	P2	P5H	L13	D7	A11
P0C	N2				
P0D	N1	P6A	D15	VAA	C3
P0E	M1	P6B	E15	VAA	C7
P0F	L3	P6C	F15	VAA	C8
P0G	L2	P6D	F14	VAA	C13
P0H	M2	P6E	G14	VAA	D4
		P6F	G15	VAA	G13
P1A	R4	P6G	J14	VAA	H3
P1B	N5	P6H	H15	VAA	H13
P1C	N4			VAA	J3
P1D	P4	P7A	B15	VAA	N3
P1E	R2	P7B	B14	VAA	N13
P1F	R3	P7C	C14		
P1G	P3	P7D	C15	GND	A5
P1H	R1	P7E	E14	GND	A7
		P7F	E13	GND	C4
P2A	P7	P7G	F13	GND	C9
P2B	R7	P7H	D14	GND	D13
P2C	R6			GND	G3
P2D	N7	OL0A	D1	GND	H2
P2E	N6	OL0B	E3	GND	H14
P2F	P6	OL0C	D3	GND	J13
P2G	P5	OL0D	D2	GND	M3
P2H	R5	OL0E	B1	GND	N12
		OL0F	C1		
P3A	R10	OL0G	C2	reserved	A2
P3B	P10	OL0H	A1	reserved	L1
P3C	P9			reserved	A12
P3D	N9	OL1A	G2	reserved	C12
P3E	R8	OL1B	H1	reserved	A14
P3F	R9	OL1C	F1	reserved	B13
P3G	N8	OL1D	G1	reserved	C11
P3H	P8	OL1E	F3	reserved	B12
		OL1F	F2	reserved	A13
P4A	M13	OL1G	E2	reserved	A15
P4B	M14	OL1H	E1	reserved	P13
P4C	P15			reserved	R12
P4D	N15	IOR	A8	reserved	P11
P4E	N14	IOG	B7	reserved	N10
P4F	R15	IOB	A6	reserved	R13
P4G	R14	PLL/SYNC*	A4	reserved	P12
P4H	P14			reserved	N11
		CE*	B2	reserved	R11
COMP	C6	R/W	B3		
FS ADJUST	A3	C0	B5		
VREF	B6	C1	C5		
		CEXT	B4		

Pin Descriptions (continued)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	N/C	P7A	P7D	P6A	P6B	P6C	P6F	P6H	P5B	P5A	P5F	P5G	P4D	P4C	P4F
14	N/C	P7B	P7C	P7H	P7E	P6D	P6E	GND	P6G	P5D	P5E	P4B	P4E	P4H	P4G
13	N/C	N/C	VAA	GND	P7F	P7G	VAA	VAA	GND	P5C	P5H	P4A	VAA	N/C	N/C
12	N/C	N/C	N/C										GND	N/C	N/C
11	D7	D6	N/C										N/C	N/C	N/C
10	D2	D5	D4										N/C	P3B	P3A
9	D3	D0	GND										P3D	P3C	P3F
8	IOR	D1	VAA										P3G	P3H	P3E
7	GND	IOG	VAA										P2D	P2A	P2B
6	IOB	VREF	COMP										P2E	P2F	P2C
5	GND	C0	C1										P1B	P2G	P2H
4	PLL/ SYNC*	CEXT	GND	VAA									P1C	P1D	P1A
3	FS ADJ	R/W	VAA	OL0C	OL0B	OL1E	GND	VAA	VAA	LD*	P0F	GND	VAA	P1G	P1F
2	N/C	CE*	OL0G	OL0D	OL1G	OL1F	OL1A	GND	SYNC*	CLK*	P0G	P0H	P0C	P0B	P1E
1	OL0H	OL0E	OL0F	OL0A	OL1H	OL1C	OL1D	OL1B	CLK	BLK*	N/C	P0E	P0D	P0A	P1H

Pin Descriptions (continued)



	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
15	P4F	P4C	P4D	P5G	P5F	P5A	P5B	P6H	P6F	P6C	P6B	P6A	P7D	P7A	N/C
14	P4G	P4H	P4E	P4B	P5E	P5D	P6G	GND	P6E	P6D	P7E	P7H	P7C	P7B	N/C
13	N/C	N/C	VAA	P4A	P5H	P5C	GND	VAA	VAA	P7G	P7F	GND	VAA	N/C	N/C
12	N/C	N/C	GND										N/C	N/C	N/C
11	N/C	N/C	N/C										N/C	D6	D7
10	P3A	P3B	N/C										D4	D5	D2
9	P3F	P3C	P3D										GND	D0	D3
8	P3E	P3H	P3G										VAA	D1	IOR
7	P2B	P2A	P2D										VAA	IOG	GND
6	P2C	P2F	P2E										COMP	VREF	IOB
5	P2H	P2G	P1B										C1	C0	GND
4	P1A	P1D	P1C									VAA	GND	CEXT	PLL/ SYNC*
3	P1F	P1G	VAA	GND	P0F	LD*	VAA	VAA	GND	OL1E	OL0B	OL0C	VAA	R/W	FS ADJ
2	P1E	P0B	P0C	P0H	P0G	CLK*	SYNC*	GND	OL1A	OL1F	OL1G	OL0D	OL0G	CE*	N/C
1	P1H	P0A	P0D	P0E	N/C	BLK*	CLK	OL1B	OL1D	OL1C	OL1H	OL0A	OL0F	OL0E	OL0H

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt467, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16). This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt467 power and ground lplanes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Ccomponents should be placed as close as possible to the associated RAMDAC pin. Whenever possiple, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt467 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt467 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located within 3 inches of the Bt467. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 33 µF capacitor shown in Figure 8 is for low-frequency power supply ripple; the 0.1 µF and 0.01-µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

PC Board Layout Considerations (continued)

Digital Signal Interconnect

The digital inputs to the Bt467 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt467 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt467 to minimize reflections. Unused analog outputs should be connected to GND.

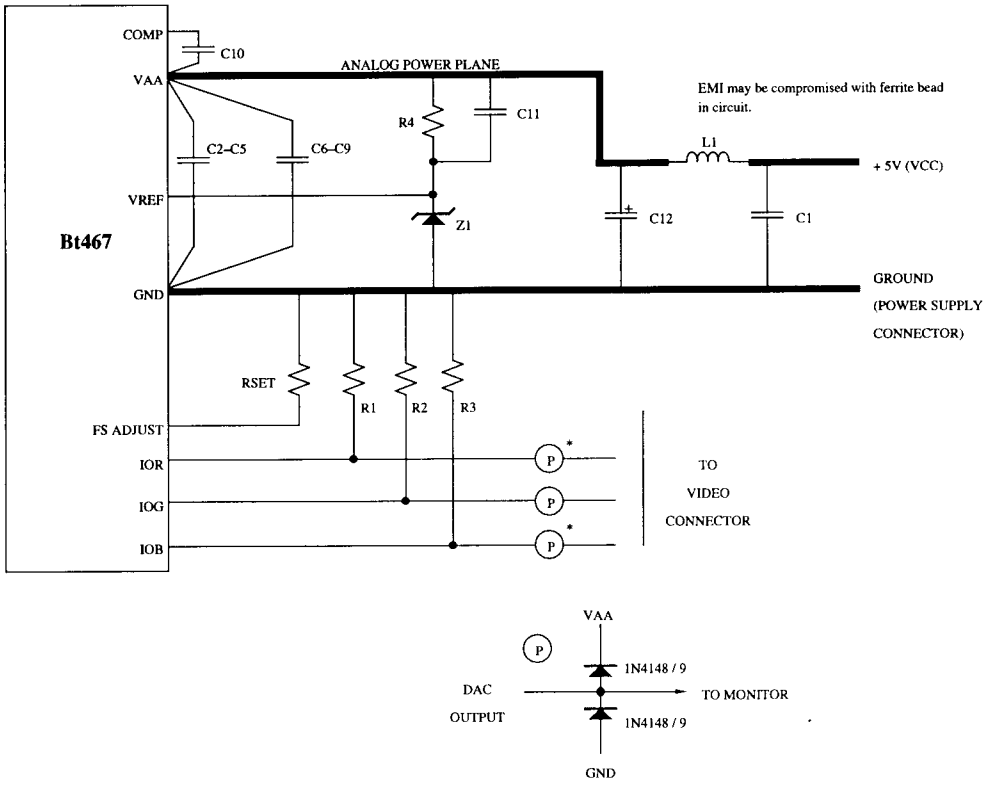
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt467 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 8 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111 *
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

* Or equivalent only.

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt467.

Figure 8. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt467 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 9.)

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt467 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by eight and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal only if fixed pipeline is not required. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt467 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt467, and will also optionally set the pipeline delay of the Bt467 to 8 clock cycles. The Bt438 may also be used to interface the Bt467 to a TTL clock. Figure 9 illustrates use of the Bt438 with the Bt467.

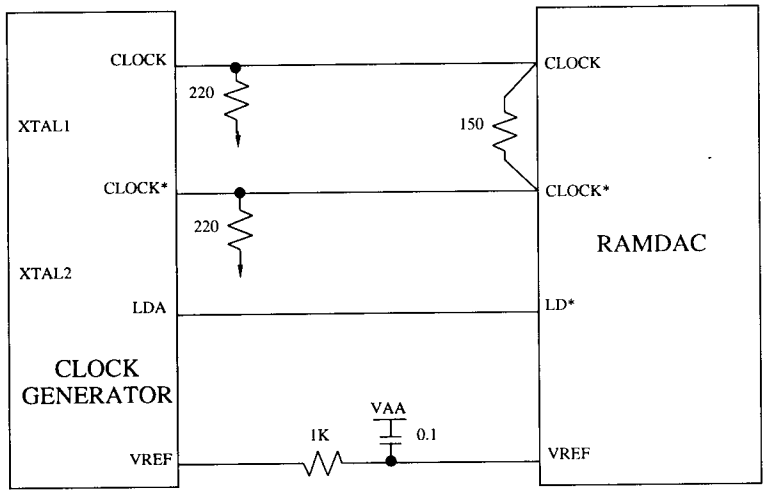


Figure 9. Generating the Bt467 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt467, although fixed after a power-up condition, may be anywhere from 6 to 13 clock cycles. The Bt467 contains additional circuitry enabling the pipeline delay to be fixed at 8 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt467.

To reset the Bt467, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

Resetting the Bt467 to an 8 clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt467s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask registers should be $00. Blinking may be done under software control via the read mask registers.

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Bt467 Color Display Applications

For color display applications when 1–4 Bt467s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt467, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt467 to eight clock cycles. The Bt439 may also be used to interface the Bt467 to a TTL clock. Figure 10 illustrates use of the Bt439 with the Bt467.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt467, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by 1–4 Bt467s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt467s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

If sub-pixel synchronization of multiple Bt467s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of 1–4 Bt467s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt467s must still have a 0.1 µF bypass capacitor to VAA.

Application Information (continued)

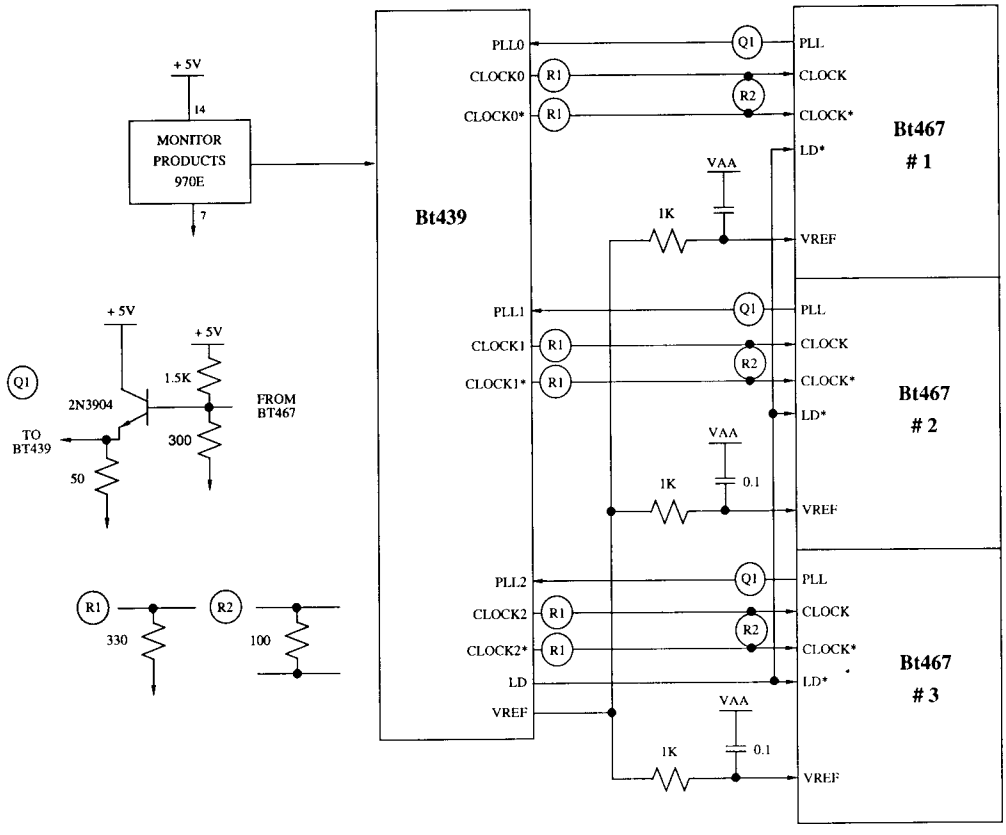


Figure 10. Generating the Bt467 Clock Signals (True-Color Application).

Application Information (continued)

Using Multiple Devices

When multiple RAMDACs are used, each RAMDAC should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each RAMDAC has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Bt467 Nonvideo Applications

The Bt467 may be used in nonvideo applications by disabling the video-specific control signals. BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}457 * VREF\ (V) / Iout\ (mA)$$

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 610 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

Initializing the Bt467 (Bt458 Register-Compatible Mode)

Following a power-on sequence, the Bt467 must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt467 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. CEXT is held low.

This sequence will configure the Bt467 as follows:

- 8:1 multiplexed operation
- 0 IRE pedestal
- no overlays
- no blinking
- sync output enabled

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10
Write $09 to address register	00
Write $06 to command register 2	10
Write $0B to address register	00
Write $00 to test register 1	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

5

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		487		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Clock Inputs	ΔVIN	.6			V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 0 IRE		0	5	50	µA
SETUP = 7.5 IRE		.95	1.44	1.90	mA
Blank Level on IOR, IOG, IOB		0	5	50	µA
LSB Size			75		µA
DAC-to-DAC Matching (Note 1)			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6	7.62	9	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–1.0		+2.5	V
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)			10		pF
Voltage Reference Input Current	IREF		10	100	µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 487 Ω and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

AC Characteristics

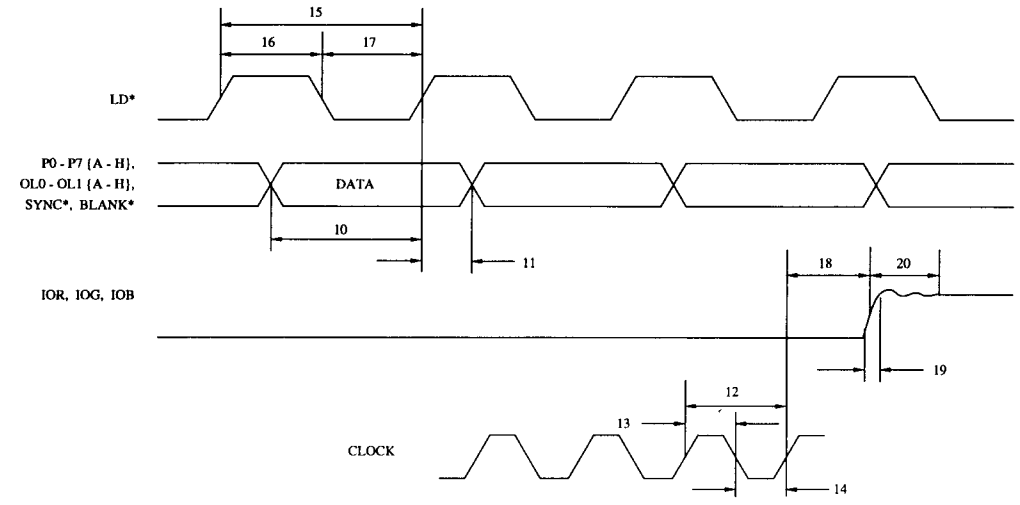
Parameter	Symbol	Min/Typ/ Max	230 MHz	170 MHz	135 MHz	Units
Clock Rate LD* Rate	Fmax LDmax	max	230 28.75	170 21.25	135 16.9	MHz MHz
R/W, C0, C1, EXT Setup Time R/W, C0, C1, EXT Hold Time	1 2	min min	0 10	0 10	0 10	ns ns
CE* Low Time CE* High Time CE* Asserted to Data Bus Driven CE* Asserted to Data Valid CE* Negated to Data Bus 3-Stated	3 4 5 6 7	min min min max max	45 25 7 45 15	45 25 7 45 15	45 25 7 45 15	ns ns ns ns ns
Write Data Setup Time Write Data Hold Time	8 9	min min	20 0	20 0	20 0	ns ns
Pixel and Control Setup Time Pixel and Control Hold Time	10 11	min min	3 2	3 2	3 2	ns ns
Clock Cycle Time Clock Pulse Width High Time Clock Pulse Width Low Time	12 13 14	min min min	4.34 1.9 1.9	5.88 2.5 2.5	7.4 3.2 3.2	ns ns ns
LD* Cycle Time LD* Pulse Width High Time LD* Pulse Width Low Time	15 16 17	min min min	34.8 14 14	47 20 20	59 24 24	ns ns ns
Analog Ouput Delay Analog Ouput Rise/Fall Time Analog Output Settling Time Clock and Data Feedthrough Glitch Impulse (Note 1) Analog Output Skew	18 19 20	typ typ max typ typ max	12 2 tbd tbd 50 1	12 2 tbd tbd 50 1	12 2 tbd tbd 50 1	ns ns ns dB pV-sec ns
Pipeline Delay		min max	6 13	6 13	6 13	Clocks Clocks
VAA Supply Current (Note 2)	IAA	typ max	450 tbd	380 tbd	360 tbd	mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 487 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. (See Figures 11 and 12 in the Timing Waveforms section.) As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2 x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 25° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms (continued)



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB for the Bt467.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 11. Video Input/Output Timing.

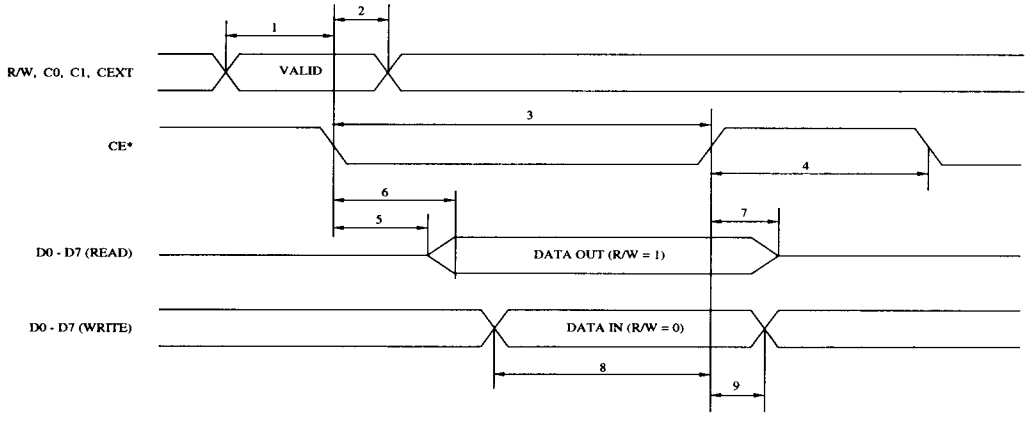


Figure 12. MPU Read/Write Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt467KG230	230 MHz	145 PGA	0° to +70° C
Bt467KG170	170 MHz	145 PGA	0° to +70° C
Bt467KG135	135 MHz	145 PGA	0° to +70° C