

DALLAS

SEMICONDUCTOR

DS1217M

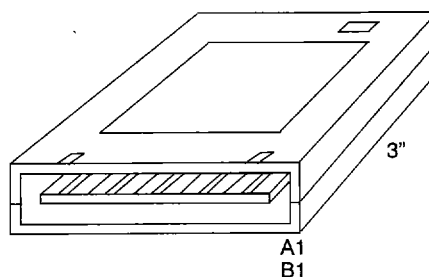
Nonvolatile Read/Write Cartridge

FEATURES

- User-insertable
- Data retention greater than 5 years
- Capacity up to 512K x 8
- Standard byte-wide pinout facilitates connection to JEDEC 28-pin DIP via ribbon cable
- Software-controlled banks maintain 32 x 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0°C to 70°C

PIN ASSIGNMENT

Name	Position	Name
Ground	A1	B1 No Connect
+5 Volts	A2	B2 Address 14
Write Enable	A3	B3 Address 12
Address 13	A4	B4 Address 7
Address 8	A5	B5 Address 6
Address 9	A6	B6 Address 5
Address 11	A7	B7 Address 4
Output Enable	A8	B8 Address 3
Address 10	A9	B9 Address 2
Cartridge Enable	A10	B10 Address 1
Data I/O 7	A11	B11 Address 0
Data I/O 6	A12	B12 Data I/O 0
Data I/O 5	A13	B13 Data I/O 1
Data I/O 4	A14	B14 Data I/O 2
Data I/O 3	A15	B15 Ground



See Mech. Drawing – Pg. 983

DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The Nonvolatile Cartridge has memory capacities from 64K x 8 to 512K x 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required

for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin byte-wide memory sites.

READ MODE

The DS1217M executes a read cycle whenever \overline{WE} (write enable) is inactive (high) and \overline{CE} (cartridge enable) is active (low). The unique address specified by the address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that \overline{CE} (cartridge enable) and \overline{OE} (output enable) access times are also satisfied. If \overline{OE} and \overline{CE} times are not satisfied, then data access must be measured from the late occurring signal (\overline{CE} or \overline{OE}) and the limiting parameter is either t_{CO} for \overline{CE} or t_{OE} for \overline{OE} rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217M is in the write mode whenever both the \overline{WE} and \overline{CE} signals are in the active (low) state after address inputs are stable. The last occurring falling edge of either \overline{CE} or \overline{WE} will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either \overline{CE} or \overline{WE} . All address inputs must be kept valid throughout the write cycle. \overline{WE} must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The \overline{OE} control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (\overline{CE} and \overline{OE} active) then \overline{WE} will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The Nonvolatile Cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC} . Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy

source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge thus has redundant batteries and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

BANK SWITCHING

Bank switching is accomplished via address lines A8, A9, A10, and A11. Initially, on power-up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64-bit pattern which will set the band switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 3 bits. Each set of address inputs is entered into the DS1217M by executing read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10, and A11. However, address line 8 defines which of the 16 banks is to be enabled, or all banks are deselected, as per Table 3. Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch Chip data sheet for more detail.)

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28-pin byte-wide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin cable connected to a 30-contact card edge connector, AMP Part

Number 499188-4. The 28-pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B1) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and the driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K x 8	2
DS1217M 1-25	128K x 8	4
DS1217M 2-25	156K x 8	8
DS1217M 3-25	384K x 8	12
DS1217M 4-25	512K x 8	16

ADDRESS INPUT PATTERN Table 2

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A9	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1	1
A10	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A11	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

BANK SELECT TABLE Table 3

BANK	A8 BIT SEQUENCE				
SELECTED	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	1	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0

BANK	A8 BIT SEQUENCE				
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground

-0.3V to + 7.0V

Operation Temperature

0°C to 70°C

Storage Temperature

-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-60		+60	μA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-10		+10	μA	
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Standby Current $\overline{CE} = 2.2V$	I_{CCS1}		15	25	mA	
Operating Current	I_{CCO1}		50	100	mA	

DC TEST CONDITIONS

Outputs Open

t Cycle = 250 ns

All Voltages Are Referenced to Ground

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			100	pF	
Input/Output Capacitance	C_{OUT}			100	pF	

AC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
\overline{OE} to Output Valid	t_{OE}			125	ns	
\overline{CE} to Output Valid	t_{CO}			210	ns	
\overline{OE} or \overline{CE} to Output Active	t_{COE}	5			ns	5
Output High Z From Deselection	t_{OD}			125	ns	5
Output Hold From Address Change	t_{OH}	5			ns	
Read Recovery Time	t_{RR}	40			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From \overline{WE}	t_{ODW}			100	ns	5
Output Active From \overline{WE}	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time From \overline{WE}	t_{DH}	20			ns	4

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate

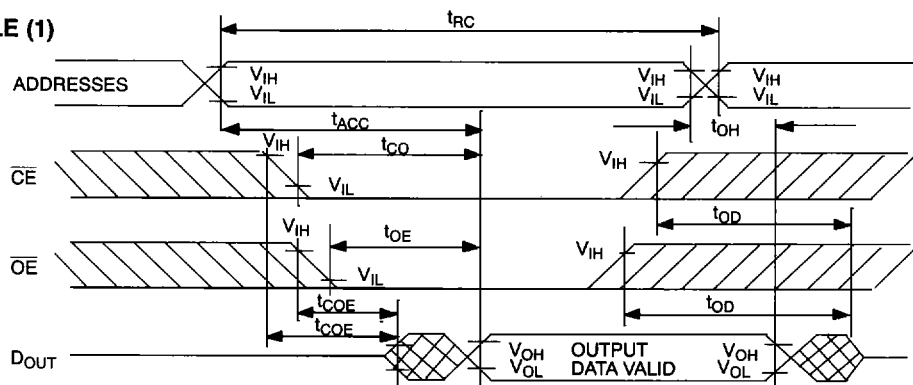
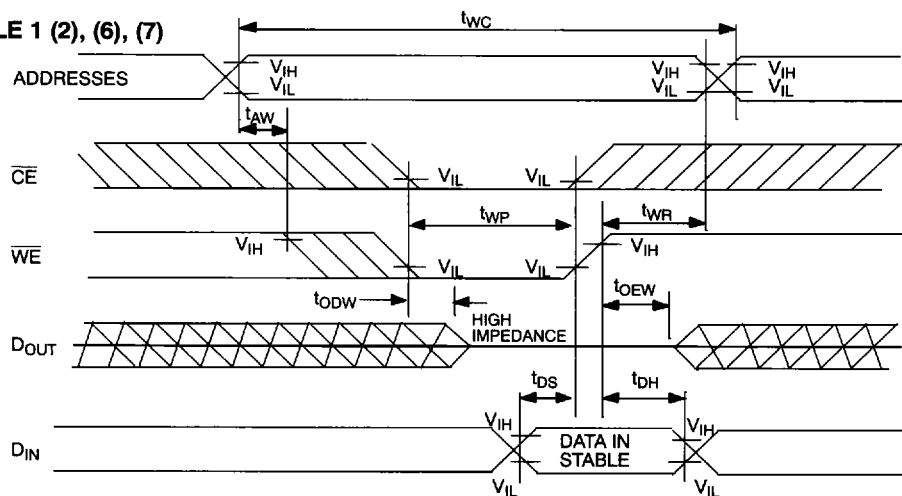
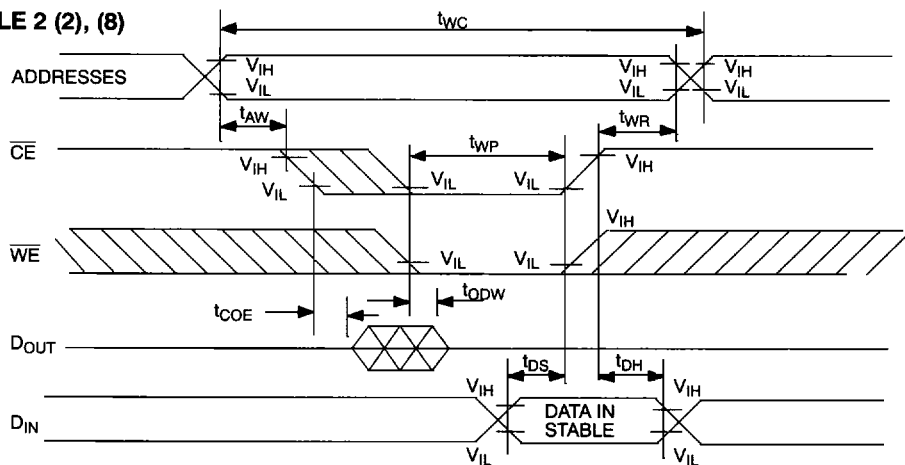
Input Pulse Levels: 0-3.0V

Timing Measurement Reference Levels

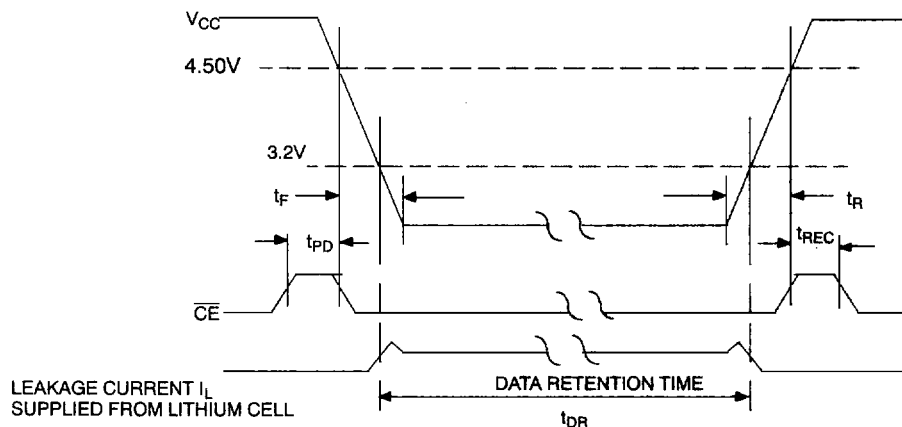
Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

READ CYCLE (1)**WRITE CYCLE 1 (2), (6), (7)****WRITE CYCLE 2 (2), (8)**

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(0° to 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PD}	\overline{CE} at V_{IH} before Power-Down	0			μs	10
t_F	V_{CC} slew from 4.5V to 0V (\overline{CE} at V_{IH})	100			μs	
t_R	V_{CC} slew from 0V to 4.5V (\overline{CE} at V_{IH})	0			μs	
t_{REC}	\overline{CE} at V_{IH} after Power-Up	2		125	ms	10

(t_A=25°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5			years	9

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. \overline{WE} is high for a read cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL} . If $\overline{OE} = V_{IH}$ during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of \overline{CE} and \overline{WE} . t_{WP} is measured from the latter of \overline{CE} or \overline{WE} going low to the earlier of \overline{CE} or \overline{WE} going high.
4. t_{DH} , t_{DS} are measured from the earlier of \overline{CE} or \overline{WE} going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the \overline{CE} low transition occurs simultaneously with or later than the \overline{WE} low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the \overline{CE} high transition occurs prior to or simultaneously with the \overline{WE} high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If \overline{WE} is low or the \overline{WE} low transition occurs prior to or simultaneously with the \overline{CE} low transition, the output buffers remain in a high impedance state in this period.
9. Each DS1217M is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.