



HV33

32 + 22 Channel Matrix Printhead Driver

Preliminary

T-51-15

Ordering Information

Device	Package Options			
	68 J - Lead Ceramic Quad Flatpack	68 J - Lead Plastic Quad Flatpack	Die	68 J - Lead Ceramic Quad Flatpack (MIL-STD-883 Processed*)
HV33	HV3304DJ	HV3304PJ	HV3304X	RBHV3304DJ

\* For Hi-Rel process flows, please refer to page 5-3 in the Databook

Features

- Separate data (32) and strobe (22) outputs
- Independant CLK and BLK functions
- 4MHz operation (either clock)
- Latched data outputs
- 68-pin QFP
- Mil version available

General Description

The HV33 is dual serial-to-parallel converter chip originally designed for driving printheads. Its dual converters have independent clock inputs and output blanking logic permitting considerable flexibility in driving small matrix arrays with one device.

Absolute Maximum Ratings

Supply voltage, $V_{DD}$	-0.5V to +7V	
Supply voltage, $V_{PD}$	36V	
Supply voltage, $V_{PS}$	36V	
Logic input levels	-0.5V to $V_{DD} + 0.5V$	
Continuous total power dissipation	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Ceramic	-40°C to +85°C
	Plastic	0°C to +70°C
Storage temperature range	-65°C to +150°C	

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**Electrical Characteristics** (over recommended operating conditions unless noted)

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**DC Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{DD}$	$V_{DD}$ Supply Current			25	mA	$f_{CLK} = 4\text{MHz}$ , $f_{DATA} = 2\text{MHz}$
$I_{DDQ}$	Quiescent $V_{DD}$ Supply Current			0.25	mA	All $V_{IN} = 0\text{V}$
$I_{PP}$	High Voltage Supply Current			0.5	mA	Output High and Low
$V_{OH}$	High-Level Data Out			36	V	$I_{OUT} = 4\text{mA}$
$I_{IH}$	High-Level Input Current			10	$\mu\text{A}$	$V_{IN} = \text{High}$
$I_{IL}$	Low-Level Input Current	-10			$\mu\text{A}$	$V_{IN} = 0\text{V}$

**AC Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$f_{CLK}$	Clock Frequency			4	MHz	
$t_W$	Clock Width High or Low	125			ns	
$t_{SU}$	Data Setup Time Before Clock Falls	50			ns	
$t_H$	Data Hold Time After Clock Falls	20			ns	
$t_{DHVS}$	Delay from -SBL to HV Strobe			2	$\mu\text{s}$	250 pF Load
$t_{DHVD}$	Delay from SCLK/DL to HV Date			2	$\mu\text{s}$	250 pF Load

**Functional Block Diagram**

