

DESCRIPTION

The HYM5V64100A is a 1M x 64-bit Fast page mode CMOS DRAM module consisting of sixteen HY51V4400B in 20/26 pin SOJ or TSOP-II and two 16-bit BiCMOS line driver in TSSOP on a 168 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.

The HYM5V64100ANG/ATNG/ASLNG/ASLTNG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- Low power dissipation
 Max. self-refresh 12.17mW (SL-part)
 Max. battery back-up 12.17mW (SL-part)
 Max. CMOS standby 9.29mW (SL-part)
 58.25mW

Max. TTL standby 115.85mW

Max. operating

Speed	Power
60	5.22W
70	4.64W
80	4.07W

- Single power supply of 3.3V ± 10%
- TTL compatible inputs and outputs
- Fast access time

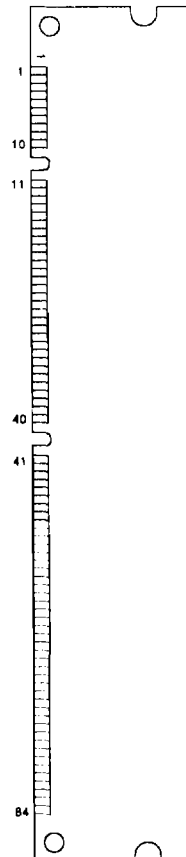
Speed	trAC	tcAC	tpC
60	60ns	20ns	40ns
70	70ns	25ns	45ns
80	80ns	25ns	50ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh
- 1024 refresh cycles / 128 ms (SL-part)
- 1024 refresh cycles / 16ms
- Buffered inputs (except RAS and DQ)
- 4 Byte interleave enabled, Dual address Inputs(A0,B0)

PIN DESCRIPTION

RAS0, RAS2	Row Address Strobe
CAS0-CAS7	Column Address Strobe
WE0, WE2	Write Enable
OE0, OE2	Output Enable
A0-A9, B0	Address Input
DQ0-DQ63	Data Input/Output
PD1-PD8	Presence Detect
PDE	Presence Detect Enable
ID0, ID1	ID Bit
Vcc	Power (+ 3.3V)
Vss	Ground

PIN CONNECTION



PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ32	128	NC
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS4	88	DQ34	130	CAS5
5	DQ3	47	CAS6	89	DQ35	131	CAS7
6	Vcc	48	WE2	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	NC	103	DQ45	145	NC
20	DQ14	62	NC	104	DQ46	146	NC
21	DQ15	63	NC	105	DQ47	147	NC
22	NC	64	NC	106	NC	148	NC
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ25	111	NC	153	DQ57
28	CAS0	70	DQ26	112	CAS1	154	DQ58
29	CAS2	71	DQ27	113	CAS3	155	DQ59
30	RAS0	72	DQ28	114	NC	156	DQ60
31	OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	NC	83	ID0(Vss)	125	NC	167	ID1
42	NC	84	Vcc	126	B0	168	Vcc

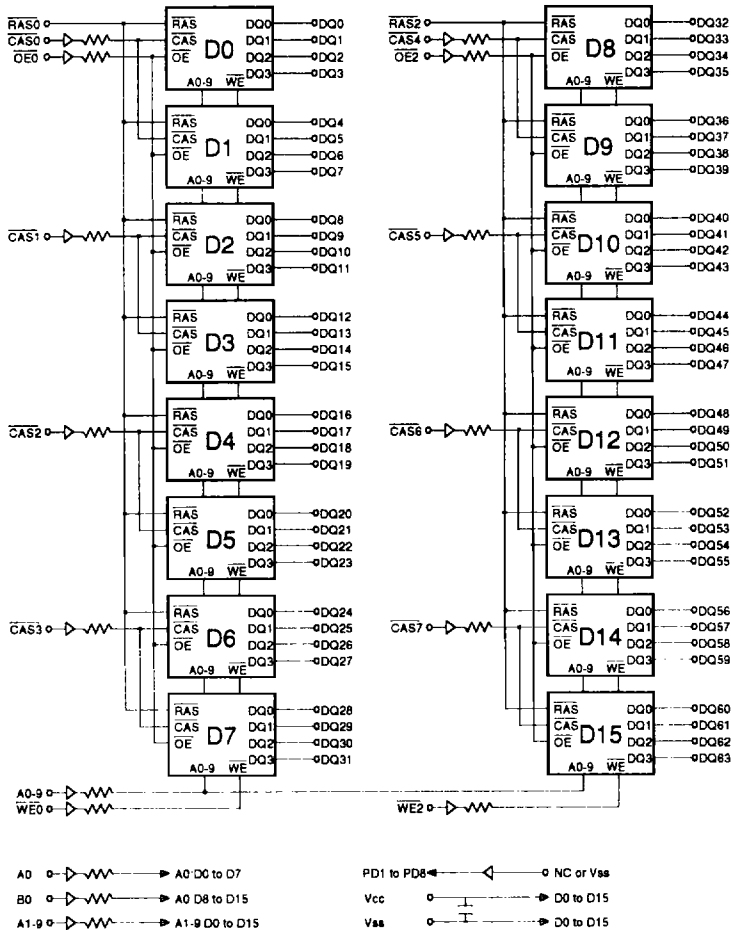
PRESENCE DETECT PINS

PIN	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	ID0	ID1
-60	Vss	Vss	NC	Vss	Vss	NC	NC	NC	Vss	NC or Vss
-70	Vss	Vss	NC	Vss	Vss	Vss	NC	NC	Vss	NC or Vss
-80	Vss	Vss	NC	Vss	Vss	NC	Vss	NC	Vss	NC or Vss

NOTE :

1. PDs are either open NC or driven to Vss via on-board buffer circuits.
2. IDs are connected directly to Vss without a buffer.
3. ID1 will be either open NC for Self-Refresh or driven to Vss for standard.

BLOCK DIAGRAM



NOTE : All resistors are 25 Ohm ± 5%

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-0.5 to 4.6	V
VCC	Voltage on VCC Relative to VSS	-0.5 to 4.6	V
Ios	Short Circuit Output Current	20	mA
PD	Power Dissipation	16.4	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	VCC+ 0.3	V
VIL	Input Low Voltage	0.3	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \leq V_{IN} \leq V_{CC} + 0.3$, other pins not under test = V_{SS}	All but $\overline{\text{RAS}}$ $\overline{\text{RAS}}$	-10 -80	10 80	μA	
I _{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ at V_{IH}		-10	10	μA	
I _{CC1}	V _{CC} Supply Current, Operating	t _{RC} = t _{RC} (min.)	60 70 80	- - -	1450 1290 1130	mA	1,2,3
I _{CC2}	V _{CC} Supply Current, TTL Standby	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ at V_{IH} , other inputs $\geq V_{SS}$		-	32.2	mA	
I _{CC3}	V _{CC} Supply Current, $\overline{\text{RAS}}$ -only refresh	t _{RC} = t _{RC} (min.)	60 70 80	- - -	1450 1290 1130	mA	1,3
I _{CC4}	V _{CC} Supply Current, Fast Page mode	t _{PC} = t _{PC} (min.)	60 70 80	- - -	970 810 650	mA	1,2,3
I _{CC5}	V _{CC} Supply Current, CMOS Standby	$\overline{\text{RAS}}$ & $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$	SL-part	- -	16.2 2.6	mA	5
I _{CC6}	V _{CC} Supply Current, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh	t _{RC} = t _{RC} (min.)	60 70 80	- - -	1450 1290 1130	mA	1,3
I _{CC7}	V _{CC} Supply Current, Battery Back Up (SL-part only)	t _{RC} = 125 μs , t _{TRAS} \leq 1 μs $\overline{\text{CAS}}$ = CBR cycling or 0.2V OE & WE = $V_{CC} - 0.2\text{V}$ A0-A9 = $V_{CC} - 0.2\text{V}$ or 0.2V DQ0-DQ63 = $V_{CC} - 0.2\text{V}$, 0.2V, or open		-	3.38	mA	1,4,5
I _{CC8}	V _{CC} Supply Current, Self Refresh (SL-part only)	$\overline{\text{RAS}}$ & $\overline{\text{CAS}} \leq 0.2\text{V}$ other pins same as I _{CC7}		-	3.38	mA	5
V _{OL}	Output Low Voltage	I _{OL} = 2.0mA		-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -2.0mA		2.4	-	V	

NOTE :

- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
- I_{CC1}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
- I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{\text{RAS}} = V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{\text{CAS}} = V_{IH}$.
- Only t_{TRAS}(max.) = 1 μs is applied to refresh of battery backup but t_{RAS}(max.) = 10 μs is applied to normal functional operation.
- I_{CC5}(max.) = 6.4mA, I_{CC7} and I_{CC8} are applied to SL-parts (HYM5V64100ASLNG/ASLTNG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V64100A N-Series						UNIT	NOTE
			-60		-70		-90			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	158	-	193	-	213	-	ns	14,15
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	83	-	98	-	108	-	ns	13,15
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	25	-	25	ns	4,9,15
7	tAA	Access Time from Column Address	-	36	-	41	-	46	ns	4,10,15
8	tCPA	Access Time from CAS Precharge	-	40	-	45	-	50	ns	4,15
9	tCLZ	CAS to Output Low Impedance	2	-	2	-	2	-	ns	4,13
10	tOFF	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	5,17
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3,12
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	RAS Hold Time	20	-	25	-	25	-	ns	15
16	tCSH	CAS Hold Time	58	-	68	-	78	-	ns	14
17	tCAS	CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	18	40	18	45	18	55	ns	9,16
19	tRAD	RAS to Column Address Delay Time	13	24	13	29	13	34	ns	10,16
20	tCRP	CAS to RAS Precharge Time	15	-	15	-	15	-	ns	15
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	6	-	6	-	6	-	ns	15
23	tRAH	Row Address Hold Time	8	-	8	-	8	-	ns	14
24	tASC	Column Address Set-up Time	2	-	2	-	2	-	ns	13
25	tCAH	Column Address Hold Time	17	-	17	-	17	-	ns	13
26	tAR	Column Address Hold Time from RAS	48	-	53	-	58	-	ns	14
27	tRAL	Column Address to RAS Lead Time	36	-	41	-	46	-	ns	15
28	tRCS	Read Command Set-up Time	2	-	2	-	2	-	ns	13
29	tRCH	Read Command Hold Time Referenced to CAS	2	-	2	-	2	-	ns	6,13
30	tRRH	Read Command Hold Time Referenced to RAS	-2	-	-2	-	-2	-	ns	6,14
31	tWCH	Write Command Hold Time	17	-	17	-	17	-	ns	13
32	tWCR	Write Command Hold Time from RAS	48	-	53	-	58	-	ns	14
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	25	-	25	-	ns	15
35	tCWL	Write Command to CAS Lead Time	17	-	22	-	22	-	ns	13
36	tDS	Data-In Set-up Time	-2	-	-2	-	-2	-	ns	7,14
37	tDH	Data-In Hold Time	20	-	20	-	25	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to RAS	48	-	53	-	58	-	ns	14
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	18
		SL-part	-	128	-	128	-	128		
40	tWCS	Write Command Set-up Time	2	-	2	-	2	-	ns	8,13

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V64100A N-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	45	-	50	-	50	-	ns	8,15
42	tRWD	RAS to WE Delay Time	83	-	98	-	113	-	ns	8,14,15
43	tAWD	Column Address to WE Delay Time	59	-	69	-	79	-	ns	8,14,15
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	15
45	tCHR	CAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	14
46	tRPC	RAS to CAS Precharge Time	-2	-	-2	-	-2	-	ns	14
47	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	RAS Hold Time Referenced to OE	15	-	15	-	15	-	ns	15
49	tOEA	OE Access Time	-	20	-	25	-	25	ns	15
50	tOED	OE to Data Delay	20	-	25	-	25	-	ns	15
51	tOEZ	Output Buffer Turn Off Delay Time from OE	2	20	2	50	2	25	ns	5,17
52	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	63	-	73	-	83	-	ns	8,14,15
54	tRHCP	RAS Hold Time from CAS Precharge	32	-	37	-	42	-	ns	13
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	8	-	8	-	8	-	ns	15
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	14
57	tPD	PDE to Valid Presence Detect Data	-	10	-	10	-	10	ns	11
58	tPDOFF	PDE Inactive to Presence Detects Inactive	2	-	2	-	2	-	ns	12

NOTE :

1. An initial pause of 200µs is required after power-up followed by 8 \overline{RAS} cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} -only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS} = V_{SS}$ during power-up, the HYM5V64100A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that \overline{RAS} and \overline{CAS} track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY51V4400B data sheet for detailed information.
4. Measured at $V_{OH} = 2.4V$ and $V_{OL} = 0.4V$ with a load equivalent to 1 TTL loads and 100pF.
5. $t_{OFF(max.)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to \overline{CAS} leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA} .
11. Measured with the specified current load and 100pF.
12. $t_{PDOff(max.)}$ is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent SIMM position.
13. $A + 2ns$ timing skew from the DRAM to the DIMM resulted from the addition of buffers (DRAM loading may add to skew).
14. $A - 2ns$ timing skew from the DRAM to the DIMM resulted from the addition of buffers (DRAM loading may add to skew).
15. $A + 5ns$ ($\overline{CAS}, \overline{WE}, \overline{OE}$) or $+ 6ns$ (address) timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add skew).
16. $A - 2ns$ min and a $-5ns$ ($\overline{CAS}, \overline{WE}, \overline{OE}$) or $-6ns$ (address) max timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add to skew).
17. $A + 2ns$ min and a $+ 5ns$ ($\overline{CAS}, \overline{WE}, \overline{OE}$) or $+ 6ns$ (address) max timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add to skew).
18. A burst of 1024 \overline{CAS} -before- \overline{RAS} refresh cycles must be executed within 16ms (256ms for SL-part) after exiting self refresh.

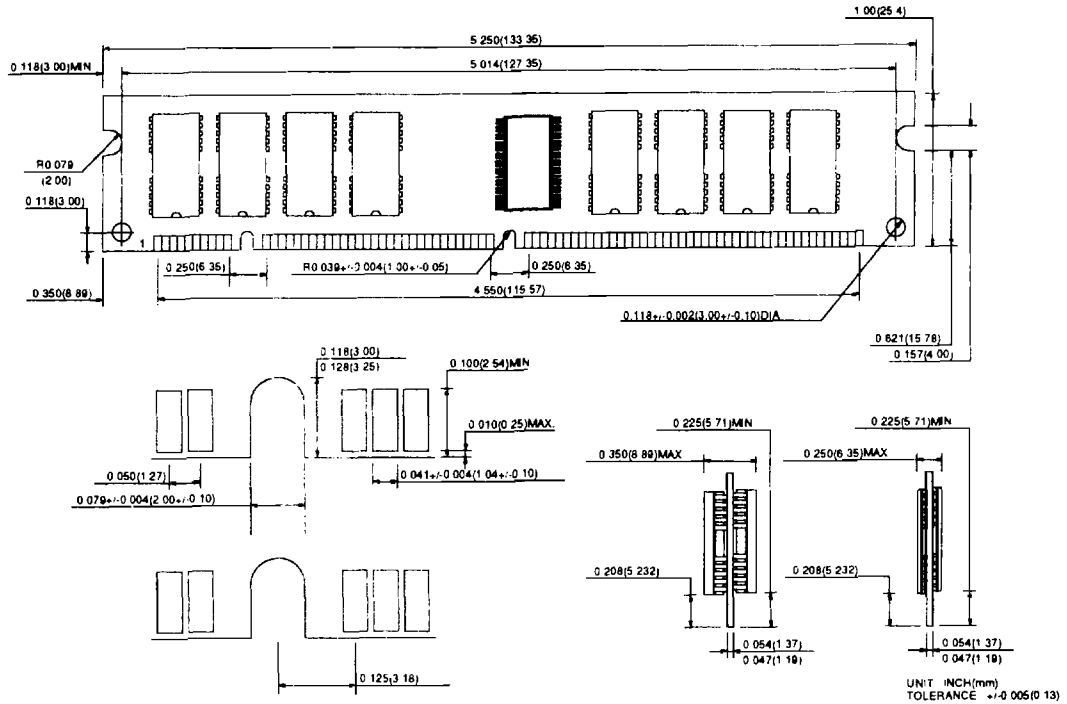
CAPACITANCE

($T_A = 25^\circ C$, $V_{CC} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $f = 1MHz$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9,B0)	-	20	pF
CIN2	Input Capacitance ($\overline{RAS0}, \overline{RAS2}$)	-	80	pF
CIN3	Input Capacitance ($\overline{CAS0}-\overline{CAS7}, \overline{WE0}, \overline{WE2}, \overline{OE0}, \overline{OE2}$)	-	20	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ63)	-	15	pF

PACKAGE INFORMATION

168 pin Dual In-line Memory Module (NG ; Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V64100ANG	60/70/80		DIMM	Gold
HYM5V64100ATNG	60/70/80		DIMM	Gold
HYM5V64100ASLNG	60/70/80	SL-part	DIMM	Gold
HYM5V64100ASLTNG	60/70/80	SL-part	DIMM	Gold