MOTOROLA

Military 54F182

Carry Lookahead Generator

ELECTRICALLY TESTED PER:
MIL-M-38510/33802

The 54F182 is a high-speed carry lookahead generator. It is generally used with the F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

- Provides Lookahead Carries Across a Group of Four ALUs
- Multi-Level Lookahead High-Speed Arithmetic Operation Over Long Word Lengths

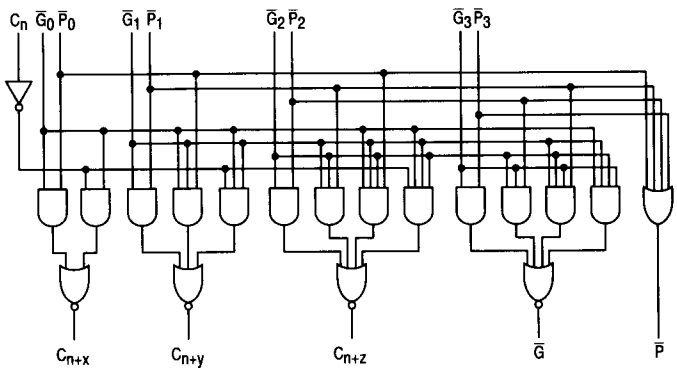
AVAILABLE AS:

1) JAN: JM38510/33802BXA
2) SMD: N/A
3) 883: 54F182/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

LOGIC DIAGRAM

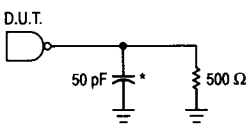


PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{G}_1$	1	1	2	V_{CC}
$\overline{P}_1$	2	2	3	V_{CC}
$\overline{G}_0$	3	3	4	V_{CC}
$\overline{P}_0$	4	4	5	V_{CC}
$\overline{G}_3$	5	5	7	V_{CC}
$\overline{P}_3$	6	6	8	V_{CC}
$\overline{P}$	7	7	9	OPEN
GND	8	8	10	GND
C_{n+z}	9	9	12	OPEN
$\overline{G}$	10	10	13	OPEN
C_{n+y}	11	11	14	OPEN
C_{n+x}	12	12	15	OPEN
C_n	13	13	17	V_{CC}
$\overline{G}_2$	14	14	18	V_{CC}
$\overline{P}_2$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TEST LOAD



*Includes Jig and Probe Capacitance

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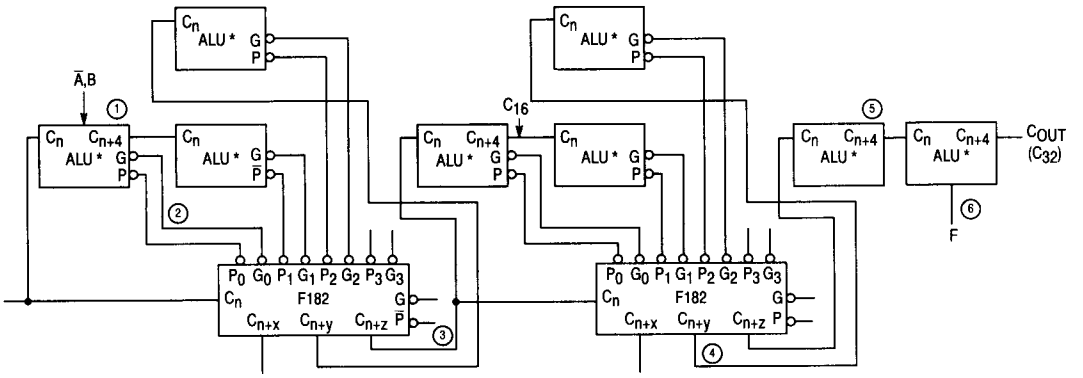
FUNCTIONAL DESCRIPTION

The F182 carry lookahead generator accepts up to four pairs of active-LOW Carry Propagation ($\overline{P}_0$–$\overline{P}_3$) and Carry Generate ($\overline{G}_0$–$\overline{G}_3$) signals and an active-HIGH Carry input (C_n) and provides anticipated active-HIGH Carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The F182 also has active-LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the output are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$P = \overline{P_3P_2P_1P_0}$$

Also, the F182 can be used with binary ALUs in an active-LOW or active-HIGH input operand mode. The connections (Figure A) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last F381.

Figure A — 32-bit ALU with Ripple Carry between 16-Bit Lookahead ALUs



*ALUs are F381.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	L	X						L			
X	L	X	X	L						H			
X	X	L	X	L						H			
H	X	X	X	L						H			
X	X	X	X	H	H	H					L		
X	X	H	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	X	X	L	X					L		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				L	
	X		X	X	H	X	H	X				L	
	X		H	H	H	X	H	X				L	
	H		H	X	H	X	H	X				L	
	X		X	X	L	X	L	X				H	
	X		X	X	X	L	L	X				H	
	X		L	X	X	L	L	X				H	
	X		X	L	X	L	L	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

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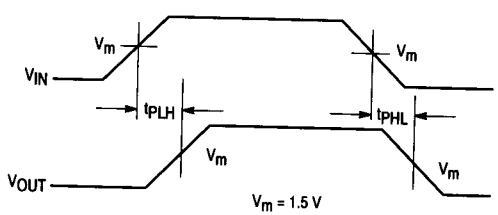
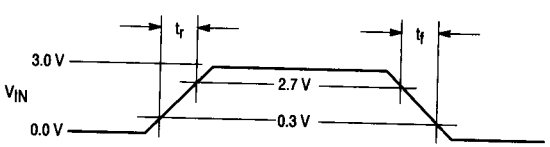
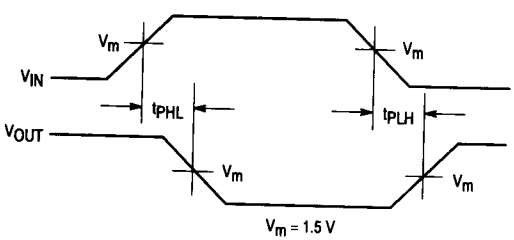
SWITCHING WAVEFORMS

NON-INVERTING FUNCTIONS





INVERTING FUNCTIONS



NOTES:

1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, and $Z_{OUT} = 50\ \Omega$.
2. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
3. $R_L = 500\ \Omega \pm 5.0\%$.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V (all inputs).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V (all inputs).
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = GND, C_n = 4.5 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs = GND, C_n = 4.5 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs = GND, V_{OUT} = 0 V.
I_{OD}	Output Diode Current	60		60		60		mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, V_{OUT} = 2.5 V
I_{IL}	Logical "0" Input Current, (G_1)	−4.0	−9.6	−4.0	−9.6	−4.0	−9.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, other inputs are open, C_n = GND.
I_{IL}	Logical "0" Input Current, (P_1, P_0, G_3)	−1.5	−3.6	−1.5	−3.6	−1.5	−3.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, C_n = GND, other inputs are open.
I_{IL}	Logical "0" Input Current, (G_0, G_2)	−3.5	−8.4	−3.5	−8.4	−3.5	−8.4	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, C_n = GND, other inputs are open.
I_{IL}	Logical "0" Input Current, (P_3)	−0.1	−2.4	−0.1	−2.4	−0.1	−2.4	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, C_n = GND, other inputs are open.
I_{IL}	Logical "0" Input Current, (P_2)	−1.5	−3.6	−1.5	−3.6	−1.5	−3.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, C_n = GND, other inputs are open.
I_{IL}	Logical "0" Input Current, (C_n)	−0.5	−1.2	−0.5	−1.2	−0.5	−1.2	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, other inputs are open.
I_{CCH}	Power Supply Current Off		28		28		28	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (G_3, P_3), other inputs = GND.
I_{CCL}	Power Supply Current Off		36		36		36	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (G_1, G_0, G2), other inputs = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, **(Repeat at)**, V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output C_n to C_n (X, Y, Z)	3.0	9.0	2.5	11	2.5	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output C_n to C_n (X, Y, Z)	3.0	8.5	3.0	11.5	3.0	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PHL2}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_n (X, Y, or Z)	1.0	5.0	1.0	7.0	1.0	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH2}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_n (X, Y, or Z)	2.5	8.5	2.0	10.5	2.0	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PHL3}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_n (X, Y, or Z)	1.0	5.2	1.0	7.0	1.0	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH3}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_n (X, Y, or Z)	2.5	8.5	2.0	11	2.0	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PHL4}	Propagation Delay /Data-Output $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	2.5	8.0	2.5	10	2.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH4}	Propagation Delay /Data-Output $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	2.5	10	2.0	12	2.0	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PHL5}	Propagation Delay /Data-Output $\overline{G}_n$ to $\overline{G}$	2.5	7.5	2.5	10	2.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH5}	Propagation Delay /Data-Output $\overline{G}_n$ to $\overline{G}$	3.0	10.5	2.5	12	2.5	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{P}_n$ to $\overline{P}$	1.5	5.5	1.5	8.0	1.5	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH6}	Propagation Delay /Data-Output $\overline{P}_n$ to $\overline{P}$	2.5	7.5	2.5	10	2.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.