
Electrical Specifications

This chapter specifies the following electrical behavior of the 21152:

- PCI electrical conformance
- Absolute maximum ratings
- dc specifications
- ac timing specifications

14.1 PCI Electrical Specification Conformance

The 21152 PCI pins conform to the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.1*. See that document for a complete description of the PCI I/O protocol and pin ac specifications.

14.2 Absolute Maximum Ratings

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The 21152 is specified to operate at a maximum frequency of 33 MHz at a junction temperature (T_j) not to exceed 125°C. Table 14–1 lists the absolute maximum ratings for the 21152. These are stress ratings only; extended exposure to the maximum ratings may affect the reliability of the device.

Table 14–1 Absolute Maximum Ratings

Parameter	Minimum	Maximum
T_j	—	125°C
T_a	0°C	70°C
P_{wc}	—	1.2 W @ 33 MHz
Storage temperature range	-55°C	125°C

14.3 dc Specifications

Table 14–2 defines the dc parameters met by all 21152 signals under normal operating conditions.

Table 14–2 dc Parameters

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{cc}	Supply voltage	—	3.0	3.6	V
V_{il}	Low-level input voltage ¹	—	–0.5	0.3 V_{cc}	V
V_{ih}	High-level input voltage ¹	—	0.5 V_{cc}	$V_{cc} + 0.5$ V	V
V_{ol}	Low-level output voltage ²	$I_{out} = 1500 \mu A$	—	0.1 V_{cc}	V
V_{ol5V}	Low-level output voltage ³	$I_{out} = 6$ mA	—	0.55	V
V_{oh}	High-level output voltage ²	$I_{out} = -500 \mu A$	0.9 V_{cc}	—	V
V_{oh5V}	High-level output voltage ³	$I_{out} = -2$ mA	2.4	—	V
I_{il}	Low-level input leakage current ^{1,4}	$0 < V_{in} < V_{cc}$	—	± 10	μA
C_{in}	Input pin capacitance	—	—	10.0	pF
C_{IDSEL}	p_idsel pin capacitance	—	—	8.0	pF
C_{clk}	p_clk, s_clk pin capacitance	—	5.0	12.0	pF

¹Guarantees meeting the specification for the 5-V signaling environment.

²For 3.3-V signaling environment.

³For 5-V signaling environment.

⁴Input leakage currents include high-Z output leakage for all bidirectional buffers with tristate outputs.

Note

In Table 14–2, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (–) current.

14.4 ac Timing Specifications

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The next sections specify the following:

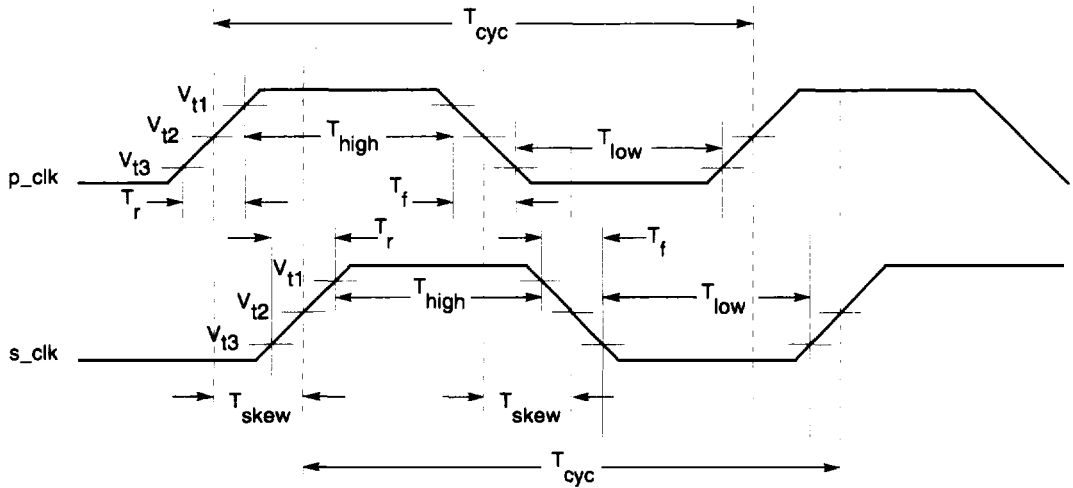
- Clock timing specifications
- PCI signal timing specifications
- Reset timing specifications

14.4.1 Clock Timing Specifications

The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain within the 21152.

Figure 14–1 shows the ac parameter measurements for the **p_clk** and **s_clk** signals, and Table 14–3 specifies **p_clk** and **s_clk** parameter values for clock signal ac timing. See also Figure 14–2 for a further illustration of signal timing.

Figure 14-1 PCI Clock Signal ac Parameter Measurements



Note:

- V_{t1} - 2.0 V for 5-V clocks; 0.5 V_{cc} for 3.3-V clocks
- V_{t2} - 1.5 V for 5-V clocks; 0.4 V_{cc} for 3.3-V clocks
- V_{t3} - 0.8 V for 5-V clocks; 0.3 V_{cc} for 3.3-V clocks

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14.4 ac Timing Specifications

Table 14–3 PCI Clock Signal ac Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	p_clk, s_clk cycle time	30	∞	ns
T_{high}	p_clk, s_clk high time	11	—	ns
T_{low}	p_clk, s_clk low time	11	—	ns
	p_clk, s_clk slew rate ¹	1	4	V/ns
T_{rclk}	Delay from p_clk to s_clk	0	7	ns
T_{rclk_r}	p_clk rising to s_clk_o rising	0	5	ns
T_{rclk_f}	p_clk falling to s_clk_o falling ²	0	5	ns
T_{dskew}	s_clk_0 duty cycle skew from p_clk duty cycle ²	—	0.750	ns
T_{skew}	s_clk_0 <x> to s_clk_0 <y>	—	0.500	ns

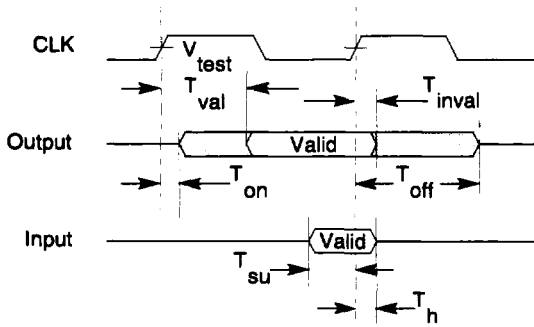
¹0.2 V_{cc} to 0.6 V_{cc}.

²Measured with 30-pF lumped load.

14.4.2 PCI Signal Timing Specifications

Figure 14–2 and Table 14–4 show the PCI signal timing specifications.

Figure 14–2 PCI Signal Timing Measurement Conditions



Note:
 V_{test} – 1.5 V for 5-V signals; 0.4 V_{CC} for 3.3-V signals

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14.4 ac Timing Specifications

Table 14–4 PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay—bused signals ^{1,2,3}	2	11	ns
$T_{val(ptp)}$	CLK to signal valid delay—point-to-point ^{1,2,3}	2	12	ns
T_{on}	Float to active delay ^{1,2}	2	—	ns
T_{off}	Active to float delay ^{1,2}	—	28	ns
T_{su}	Input setup time to CLK—bused signals ^{1,2,3}	7	—	ns
$T_{su(ptp)}$	Input setup time to CLK—point-to-point ^{1,2,3}	10, 12	—	ns
T_h	Input signal hold time from CLK ^{1,2}	0	—	ns

¹See Figure 14–2.

²All primary interface signals are synchronized to **p_clk**. All secondary interface signals are synchronized to **s_clk**.

³Point-to-point signals are **p_req_l**, **s_req_l<3:0>**, **p_gnt_l**, and **s_gnt_l<3:0>**. Bused signals are **p_ad**, **p_cbe_l**, **p_par**, **p_perr_l**, **p_serr_l**, **p_frame_l**, **p_irdy_l**, **p_trdy_l**, **p_lock_l**, **p_devsel_l**, **p_stop_l**, **p_idsel**, **s_ad**, **s_cbe_l**, **s_par**, **s_perr_l**, **s_serr_l**, **s_frame_l**, **s_irdy_l**, **s_trdy_l**, **s_lock_l**, **s_devsel_l**, and **s_stop_l**.

14.4.3 Reset Timing Specifications

Table 14–5 shows the reset timing specifications for **p_rst_l** and **s_rst_l**.

Table 14–5 Reset Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{ret}	p_rst_l active time after power stable	1	—	μ s
$T_{ret-clk}$	p_rst_l active time after p_clk stable	100	—	μ s
$T_{ret-off}$	p_rst_l active-to-output float delay	—	40	ns
T_{reset}	s_rst_l active after p_rst_l assertion	—	40	ns
$T_{reset-on}$	s_rst_l active time after s_clk stable	100	—	μ s
T_{dreset}	s_rst_l deassertion after p_rst_l deassertion	20	25	Cycles
	p_rst_l slew rate ¹	50	—	mV/ns

¹Applies to rising (deasserting) edge only.