



HV38

Preliminary

## 32-Channel Gray-Shade Display Column Driver

### Ordering Information

Device	Package Options			
	64-Lead 3-sided Plastic Gullwing	80-Lead Ceramic Gullwing	Die	80-Lead Ceramic Gullwing (MIL-STD-883 Processed*)
HV38	HV3806PG	HV3806DG	HV3806X	RBHV3806DG

\* For Hi-Rel process flows, refer to page 5-3 of the Databook.

### Features

- 5V CMOS inputs
- Up to 60V modulation voltage
- Capable of 16 levels of gray shading
- 16MHz data throughput rate
- 32 Outputs per device (can be cascaded)
- Minimum 15 mA high-voltage output source/sink capability
- Pin-programmable shift direction (DIR)
- D/A conversion can be performed in as little as 3.2 $\mu$ s
- Diodes in output structure allow usage in energy recovery systems
- Integrated high-voltage CMOS technology
- Available in 3-sided 64-lead gullwing package or as dice

### Absolute Maximum Ratings<sup>1</sup>

Supply voltage, $V_{DD}$	-0.5V to +7.5V	
Supply voltage, $V_{PP1}/V_{PP2}$	-0.5V to +70V	
Logic input levels	-0.5 to $V_{DD} + 0.5V$	
Ground current <sup>2</sup>	1.5A	
Continuous total power dissipation <sup>2,3</sup>	Plastic	1200mW
	Ceramic	1500mW
Operating temperature range	-40°C to +85°C	
Storage temperature range	-65°C to +150°C	
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C	

#### Notes:

1. All voltages are referenced to  $V_{SS}$ .
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

### General Description

The HV38 is a 32-channel column driver IC designed for gray-shade display use. A bidirectional shift register working on both clock edges is used to index input data, in groups of 4, into a set of data latches. These are compared to the contents of a master binary counter. Each time the master counter begins to increment, a hold capacitor ( $C_H$ ) on each channel is charged until the contents of the data latches is matched by that in the counter. Each channel's  $C_H$  thus is charged to an individual level,  $V_H$ , which is then transferred to the output by a source-follower structure that allows both sourcing and sinking of output current.

DIR is a shift-direction-select pin which has been provided to allow the user to interchange the shift register data input. When the DIR input is high, data is shifted in thru D1 to D4 in ascending order from HV<sub>OUT</sub>1 to HV<sub>OUT</sub>32. When the DIR input is low, data is shifted in descending order from HV<sub>OUT</sub>32 to HV<sub>OUT</sub>1.

In the HV38, the ramp generator circuitry ( $V_R$ ) obtains its (low-current) bias from  $V_{PP1}$ . This allows the output bias,  $V_{PP2}$ , to be ramped down to zero when output current is not required, thus saving energy.

# Electrical Characteristics (at 25°C, unless otherwise specified)

## Low-Voltage DC Characteristics

Symbol	Parameter	Min	Typ <sup>1</sup>	Max	Units	Conditions
$V_{DD}$	Low-voltage supply	4.5	5.0	5.5	V	$f_{SC} = 8\text{MHz}$
$I_{DD}$	$V_{DD}$ supply current (active)		6.0	10.0	mA	$f_{CC} = 6\text{MHz}$ $F_{DATA} = 8\text{MHz}$
$I_{DDS}$	$V_{DD}$ supply current (standby)			100	$\mu\text{A}$	All $V_{IN} = 0\text{V}$ , $V_{DD} = \text{min}$
$V_{IH}$	High-level input voltage	$V_{DD} - 1$		$V_{DD}$	V	
$V_{IL}$	Low-level input voltage	0		1	V	
$I_{IH}$	High-level input current		1.0	50	$\mu\text{A}$	$V_{IH} = V_{DD}$
$I_{IL}$	Low-level input current		-1.0	-50	$\mu\text{A}$	$V_{IL} = 0\text{V}$
$C_{IN}$	Input capacitance (data, LC, SC, CC)			10	pF	$V_{IN} = 0\text{V}$ , $f = 1\text{MHz}$
$T_A$	Operating free-air temperature	-40		85	$^{\circ}\text{C}$	
$V_{OH}$	High-level output voltage	$V_{DD} - 1$			V	$I_{OH} = -4\text{mA}$ , $V_{DD} = \text{min}$
$V_{OL}$	Low-level output voltage			0.4	V	$I_{OL} = 4\text{mA}$ , $V_{DD} = \text{min}$
$I_{OH}$	High-level output current			-4.0	mA	
$I_{OL}$	Low-level output current			4.0	mA	

Note 1. All typical values are at  $V_{DD} = 5.0\text{V}$ .

## High-Voltage DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{PP}$	High-voltage supply	-0.3		60	V	
$I_{PP}$	$V_{PP}$ supply current			100	$\mu\text{A}$	$V_{PP} = 60\text{V}$ , outputs high or low, no load
$V_R$	Ramp voltage	0		$V_{PP} - 2$	V	
$I_{AOH \text{ max}}$	Maximum high-voltage analog output source current <sup>1</sup>			-15	mA	$V_{PP} = 60\text{V}$
$I_{AOH}$	High-voltage analog output source current <sup>1</sup>	-10			mA	$V_{PP} = 60\text{V}$ $V_R = 30\text{V}$ , $V_{AO} = 25\text{V}$
		-100			$\mu\text{A}$	$V_{AO} = 28.75\text{V}$
$I_{AOL \text{ max}}$	Maximum high-voltage analog output sink current <sup>2</sup>			15	mA	$V_{PP} = 60\text{V}$
$I_{AOL}$	High-voltage analog output sink current <sup>2</sup>	10			mA	$V_{PP} = 60\text{V}$ $V_R = 30\text{V}$ , $V_{AO} = 25\text{V}$
		100			$\mu\text{A}$	$V_{AO} = 31.25\text{V}$

### Notes:

1. Either by N-CH transistor or P-CH output diode.
2. Either by P-CH transistor or N-CH output diode.
3. Power-up sequence should be the following:
  1. Connect ground.
  2. Apply  $V_{DD}$ .
  3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
  4. Apply  $V_{PP}$ .
 Power-down sequence should be the reverse of the above.

## Electrical Characteristics

AC Characteristics ( $V_{DD} = 5V$ ,  $T_A = 25^\circ C$ )

### Logic Timing

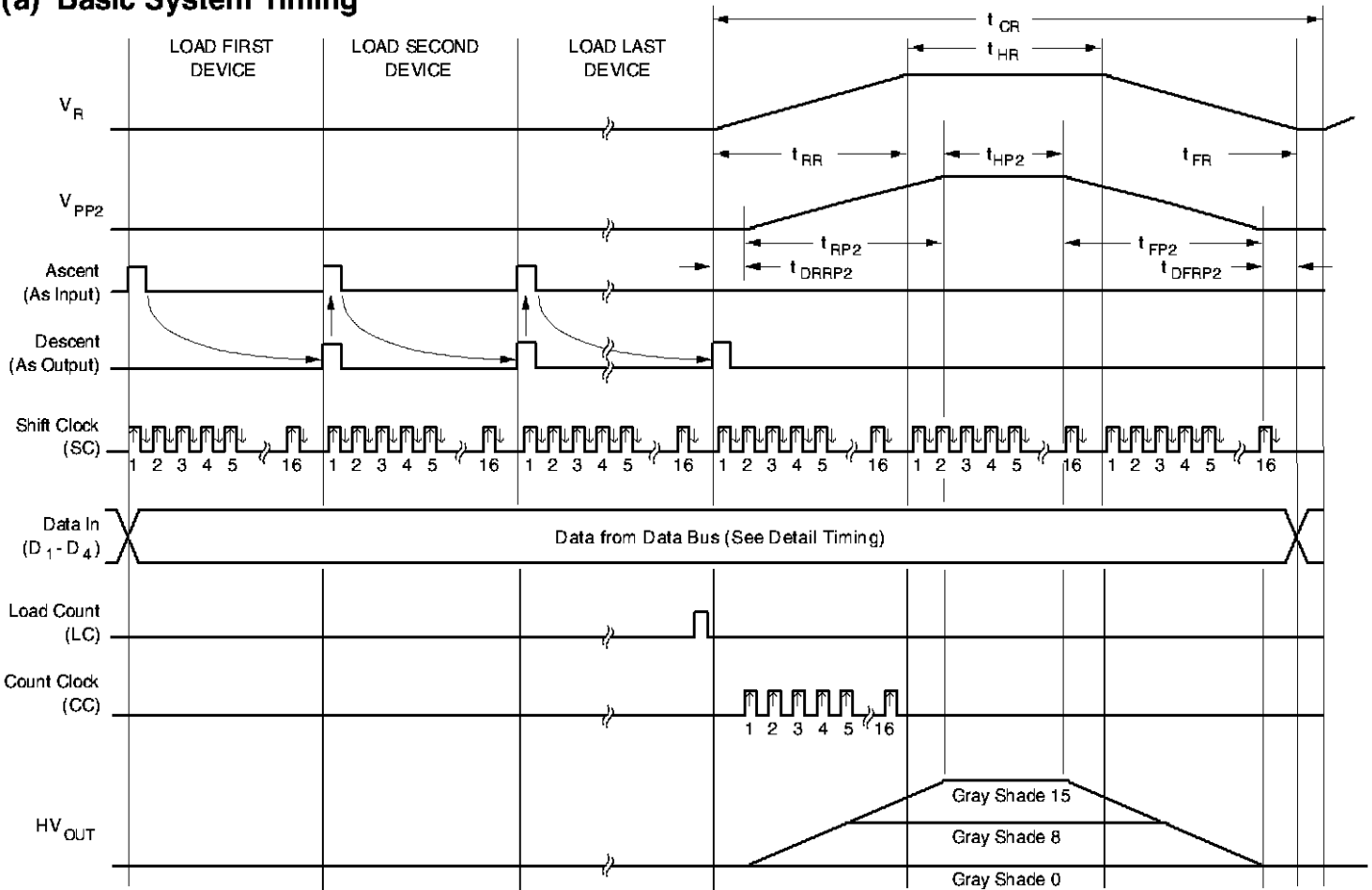
Symbol	Parameter	Min	Typ	Max	Units	Conditions
$f_{SC}$	Shift clock operating frequency			8	MHz	
$f_{DIN}$	Data-in frequency			16	MHz	
$t_{SS}$	Ascent/Descent pulse to shift clock setup time		20		ns	
$t_{HS}$	Ascent/Descent pulse to shift clock hold time		40		ns	
$t_{WA}$	Ascent pulse width		55		ns	
$t_{DS}$	Data to shift clock setup time		0		ns	
$t_{DH}$	Data to shift clock hold time		50		ns	
$t_{WD}$	Data-in pulse width		55		ns	
$t_{WLC}$	Load count pulse width		200		ns	
$t_{DLCR}$	Load count to ramp delay			100	ns	
$t_{DLCC}$	Load count to count clock delay		70		ns	
$t_{WLC}$	Load count pulse width		200		ns	
$t_{DSL}$	Shift clock to load count delay time		200		ns	
$t_{CSC}$	Shift clock cycle time			125	ns	
$t_{CCC}$	Count clock cycle time	190			ns	
$t_{WCC}$	Count clock pulse width	90			ns	

### V<sub>RAMP</sub> Timing

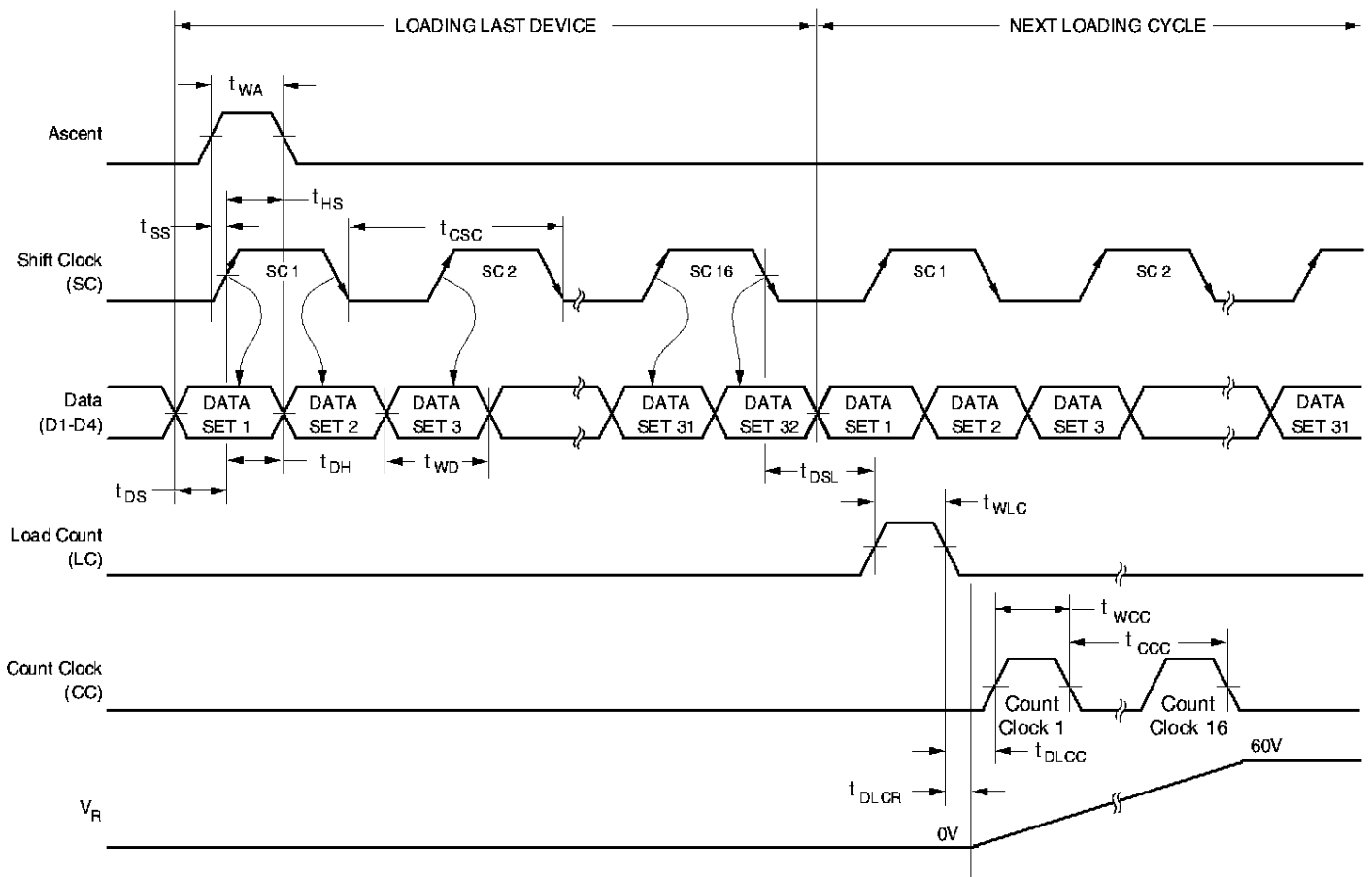
Symbol	Parameter	Min	Typ	Max	Units	Conditions
$t_{CR}$	Cycle time of ramp signal	8			$\mu s$	
$t_{RR}$	Ramp rise time	3			$\mu s$	
$t_{HR}$	Ramp hold time	2			$\mu s$	
$t_{FR}$	Ramp fall time	3			$\mu s$	
$t_{DRRP2}$	Rise time delay from $V_R$ to $V_{PP2}$	TBD			$\mu s$	
$t_{HP2}$	$V_{PP2}$ hold time	TBD			$\mu s$	
$t_{RP2}$	$V_{PP2}$ ramp-up time	TBD			$\mu s$	
$t_{FP2}$	$V_{PP2}$ ramp-down time	TBD			$\mu s$	
$t_{DFRP2}$	Fall time delay from $V_R$ to $V_{PP2}$	TBD			$\mu s$	

# Timing Diagrams

## (a) Basic System Timing



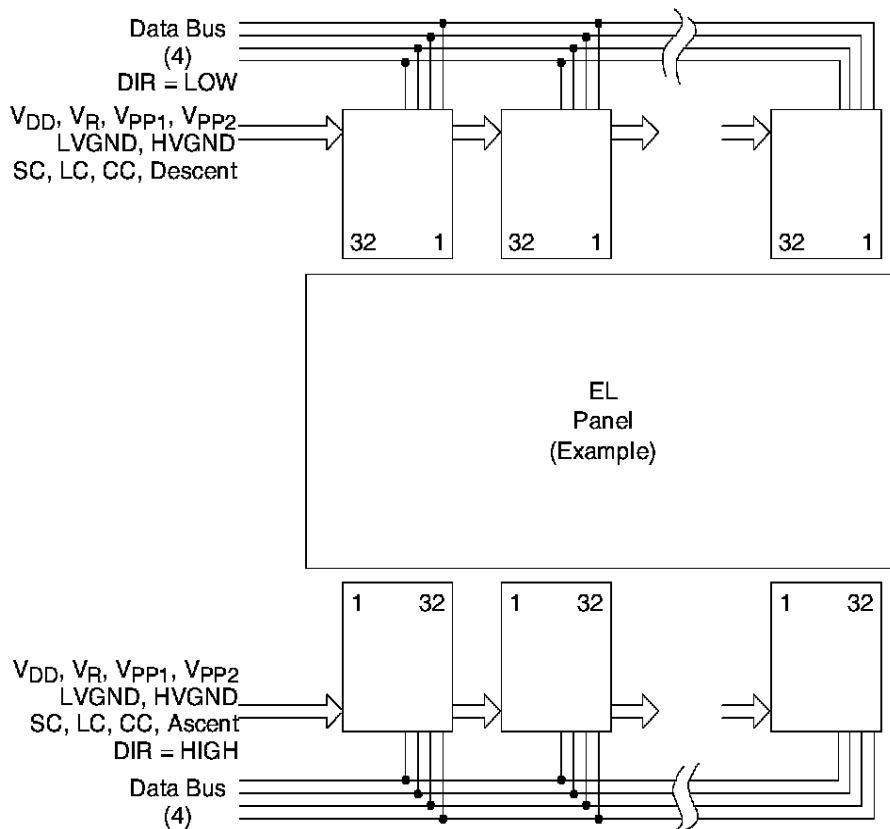
## (b) Detailed Device Timing



# Pin Definitions

Pin #	Name	Function
27-30	D1-D4	Inputs for binary-format parallel data
26	Shift clock	Triggers data on both rising and falling edges. This implies that the data rate is always twice the clock rate (data rate = 16MHz max if clock rate = 8MHz max)
22	Ascent	Input pin for the Ascent pulse (when DIR is high). Output pin for Descent pulse (when DIR is low).
43	Descent	Input pin for the Descent pulse (when DIR is low). Output pin for the Ascent pulse (when DIR is high).
40	Load Count	Input for a pulse whose rising edge causes data from the input latches to enter the comparator latches, and whose falling edge initiates the conversion of this binary data to an output level (D-to-A).
42	Count Clock	Input to the count clock generator whose increments are compared to the data in the comparator latches.
18,47	$V_R$	High-voltage ramp input for charging the output stage hold capacitors ( $C_H$ ). This input can be linear or non-linear as desired.
32	DIR	When this pin is connected to $V_{DD}$ , input data is shifted in ascending order, i.e. corresponding to $HV_{OUT1}$ to $HV_{OUT32}$ . When connected to LVGND, input data is shifted in descending order, i.e. corresponding to $HV_{OUT32}$ to $HV_{OUT1}$ .
31	LVGND	This is ground for the logic section. It may be connected to the HVGND pin, or kept separate in energy recovery circuits.
20,45	HVGND	This is ground for the high-voltage (output) section. It may be connected to the LVGND pin, or kept separate in energy recovery circuits.
19,46	$V_{PP1}$	This input biases the level translators and the P-channel transistors that charge the holding caps ( $C_H$ ).
17,48	$V_{PP2}$	This input biases the output source followers. It can be set equal to $V_{PP1}$ or can be ramped (especially in energy recovery schemes).
1-16 49-64	$HV_{OUT1}$ - $HV_{OUT32}$	High-voltage source-follower outputs.
33	$V_{DD}$	Low-voltage logic power supply.

# Typical EL Panel Connections



# Theory of Operation

The HV38 has two primary functions:

- 1) Loading data from the data bus and,
- 2) Gray-shade conversion  
(converting latched data to output voltages).

Since the device was developed initially for electroluminescent displays, the operation will be described in terms that pertain to that technology. As shown by the Typical EL Drive Scheme, several HV38 packages are mounted at the top and bottom of a display panel. Data exists on a 4-bit bus (adjacent PC board traces) at top and bottom. The D1 through D4 inputs of each chip take data from the bus when either an ASCENT or DESCENT pulse is present at the chip. These pulses therefore act as a combination CHIP SELECT and LOCATION STROBE. Because of the way the chip HV<sub>OUT</sub> pins are sequenced, data on the bus at the bottom of the display panel will be entered into the left-most chip as HV<sub>OUT1</sub>, HV<sub>OUT2</sub>, etc. up to HV<sub>OUT32</sub>. The ASCENT pulse will accomplish this with DIR = High.

## Loading Data from Data Bus

Here is the full data-entry sequence:

- 1) The microcontroller puts data on the bus (4 bits)
- 2) To enter the data into the 32 sets of 4 latches on the first chip, the shift clock rises. This positive transition is combined with the ASCENT pulse (sometimes called a SEED BIT) and is generated only once to strobe the data into the first set of latches. (These latches eventually send data to the HV<sub>OUT1</sub>). The data on the bus then changes, the shift clock falls, and this negative transition is combined with the ASCENT pulse, which is now propagated internally, to strobe the new data into the next set of 4 latches (which will end up as HV<sub>OUT2</sub>). This internal ASCENT pulse therefore runs at twice the shift clock rate.
- 3) When the last set of 4 latches in the first chip has been loaded (HV<sub>OUT32</sub>), the ASCENT pulse leaves chip 1 and enters chip 2. The exit pin is called DESCENT and the chip 2 entry pin is ASCENT. For chips at the top of the panel things are reversed: DIR is low, entry pins are DESCENT and exit pins are ASCENT, because the data-into-latches sequence is in descending order, HV<sub>OUT32</sub> down to HV<sub>OUT1</sub>.

- 4) The buses may of course be separate, and data can be strobed in on an interleaved basis, etc., but those complications will be left to systems designers.

When data has been loaded into all 32 outputs of all chips (top and bottom of the display panel), the load count pin is pulsed. On its rising transition, all the data in the input latches is transferred to a like number of comparator latches, (thus leaving the data latches ready to receive new data during the following operations). After the transfer, the load count pin is brought low. This transition begins the events that convert the binary data into a gray-shade level.

## Gray-shade Conversion

- 1) The COUNT CLOCK is started. This external signal is applied to the COUNT CLOCK pin, causing the counter on each chip to increment from binary 0000 to 1111 (0 to 15).
- 2) At the same time, the V<sub>R</sub> voltage is applied to all chips, via charging transistors, causing the HOLD CAPACITORS (C<sub>H</sub>) on each output to experience a rise in voltage.
- 3) If each set of comparator latches held binary 1111 (a count of 15), the V<sub>R</sub> voltage would charge each C<sub>H</sub> to the full value of V<sub>R</sub>. The voltage followers on each output would thus present this level as a maximum-brightness output to the panel.
- 4) On the other hand, if the count in the comparator latches is less than maximum, when the COUNT CLOCK had incremented the master counter to a value that matched the latch value, that particular charging transistor would be cut off, leaving that C<sub>H</sub> at some other value of voltage (gray-shade level).

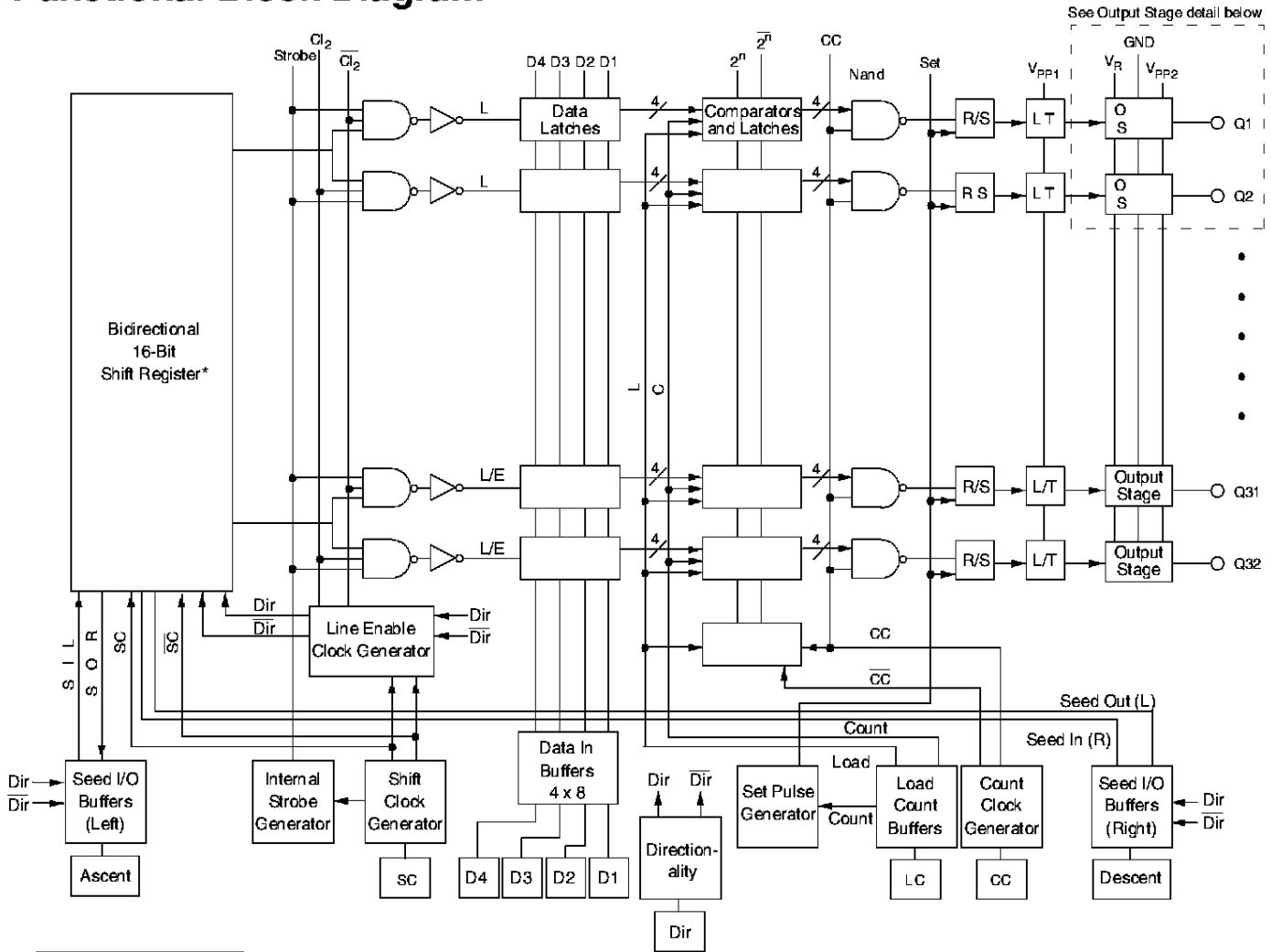
It should be clear that :

- a) Data continues until all latches in all chips are loaded. The shift clock and the internal ASCENT/DESCENT pulses last for the same duration.
- b) Count clock endures for 16 counts after load count goes low.

## Function Table

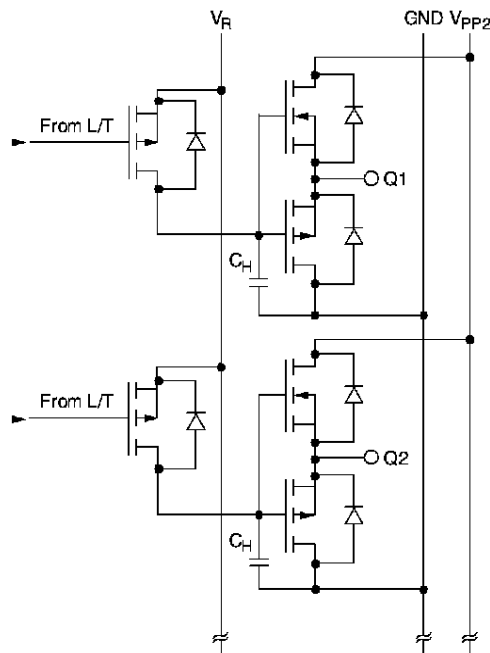
Sequence	Function	DIR	Data-In (D1 - D4)	Ascent	Descent	Shift Clock	Load Count	Count Clock	V <sub>R</sub>
1	Shift Data from HV <sub>OUT1</sub> to 32	H	H/L		Output		L	L	L
2	Shift Data from HV <sub>OUT32</sub> to 1	L	H/L	Output			L	L	L
3	Load Shift Register	X	X	Pre-defined by 1 or 2			L	L	L
4	Load Counter	X	X			L		L	L
5	Counting/Voltage Conversion	X	X			L	L		Initiates V <sub>RAMP</sub>

# Functional Block Diagram



\* Uses both dock edges.

## Output Stage Detail



# Pin Configuration

# Package Outlines

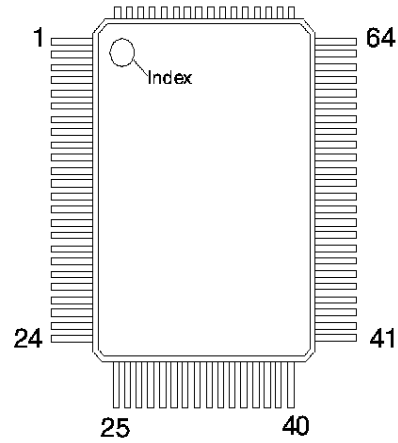
## 64-Pin PG Package

Pin	Function	Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 1	23	NC	45	HVGND
2	HV <sub>OUT</sub> 2	24	NC	46	V <sub>PP1</sub>
3	HV <sub>OUT</sub> 3	25	NC	47	V <sub>R</sub>
4	HV <sub>OUT</sub> 4	26	Shift Clock	48	V <sub>PP2</sub>
5	HV <sub>OUT</sub> 5	27	D <sub>4</sub>	49	HV <sub>OUT</sub> 17
6	HV <sub>OUT</sub> 6	28	D <sub>3</sub>	50	HV <sub>OUT</sub> 18
7	HV <sub>OUT</sub> 7	29	D <sub>2</sub>	51	HV <sub>OUT</sub> 19
8	HV <sub>OUT</sub> 8	30	D <sub>1</sub>	52	HV <sub>OUT</sub> 20
9	HV <sub>OUT</sub> 9	31	LVGND	53	HV <sub>OUT</sub> 21
10	HV <sub>OUT</sub> 10	32	DIR	54	HV <sub>OUT</sub> 22
11	HV <sub>OUT</sub> 11	33	V <sub>DD</sub>	55	HV <sub>OUT</sub> 23
12	HV <sub>OUT</sub> 12	34	NC	56	HV <sub>OUT</sub> 24
13	HV <sub>OUT</sub> 13	35	NC	57	HV <sub>OUT</sub> 25
14	HV <sub>OUT</sub> 14	36	NC	58	HV <sub>OUT</sub> 26
15	HV <sub>OUT</sub> 15	37	NC	59	HV <sub>OUT</sub> 27
16	HV <sub>OUT</sub> 16	38	NC	60	HV <sub>OUT</sub> 28
17	V <sub>PP2</sub>	39	NC	61	HV <sub>OUT</sub> 29
18	V <sub>R</sub>	40	Load Count	62	HV <sub>OUT</sub> 30
19	V <sub>PP1</sub>	41	NC	63	HV <sub>OUT</sub> 31
20	HVGND	42	Count Clock	64	HV <sub>OUT</sub> 32
21	NC	43	DESCENT		
22	ASCENT	44	NC		

\*Pins 65 to 80 are NC (ceramic only)

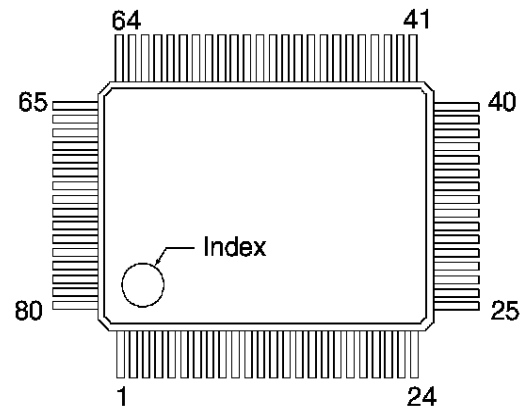
# Gray Shade Decoding Scheme

Brightest Shade No.	D4	D3	D2	D1	
15	1	1	1	1	Brightest
14	1	1	1	0	
13	1	1	0	1	
12	1	1	0	0	
11	1	0	1	1	
10	1	0	1	0	
9	1	0	0	1	
8	1	0	0	0	
7	0	1	1	1	
6	0	1	1	0	
5	0	1	0	1	
4	0	1	0	0	
3	0	0	1	1	
2	0	0	1	0	
1	0	0	0	1	
0	0	0	0	0	Dimmest



top view

3-sided Plastic 64-pin Gullwing Package



top view

80-pin Ceramic Gullwing Package