National Semiconductor

ADVANCE INFORMATION

74LCX273
Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

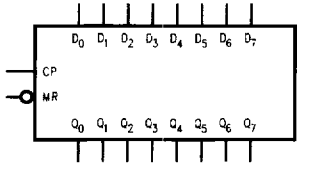
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX273 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 273
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



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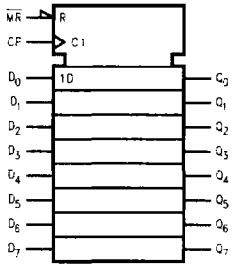
IEEE/IEC



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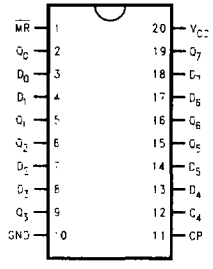
Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX273WM 74LCX273WMX	74LCX273SJ 74LCX273SJX	74LCX273MSA 74LCX273MSAX	74LCX273MTC 74LCX273MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20