HM53051 Series

262,144-word × 4-bit Frame Memory

HM53051P is a 262,144-word × 4-bit frame memory, using the most advanced 1.3 µm CMOS processes. It performs serial access by an internal address generator, and offers a fast cycle time of 34 ns, 45 ns, or 60 ns (min). Input and output data can be written or read in any cycle, synchronized with a system clock. The delay between data read/write operations is variable. Y/C separation and frozen pictures can be attained easily in 8 fsc NTSC digital TV or VCR systems. HM53051 features random access in 32-word × 4-bit data blocks. This function allows picture-in-picture or a multiplexed picture to be displayed with ease.

Features

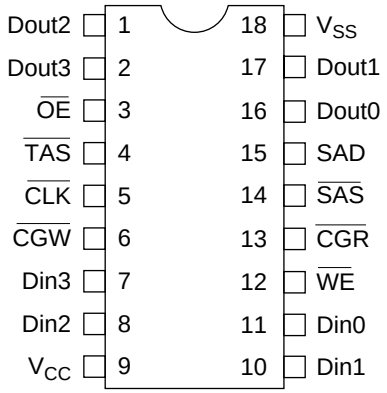
- 262,144-word × 4-bit serial access memory
- Dual ports
  - — Serial input: 4-bit
  - — Serial output: 4-bit
- High speed
  - — Read/write cycle time: 34/45/60 ns (min)
  - — Access time: 30/35/40 ns (max)
- Semi-synchronous read/write cycle
- Low power
  - — Active HM53051-34: 225 mW (typ)
    HM53051-45/60: 200 mW (typ)
- Random access in 32-word × 4-bit blocks
- No external refresh control required

Ordering Information

Type No.	Cycle Time	Package
HM53051P-34	34 ns	300-mil, 18-pin plastic DIP
HM53051P-45	45 ns	
HM53051P-60	60 ns	
HM53051FP-34	34 ns	28-pin plastic SOP
HM53051FP-45	45 ns	
HM53051FP-60	60 ns	

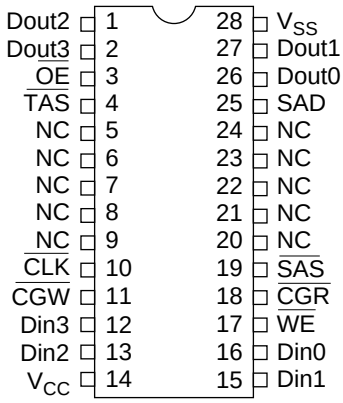
Pin Arrangement

HM53051P Series



(Top view)

HM53051FP Series

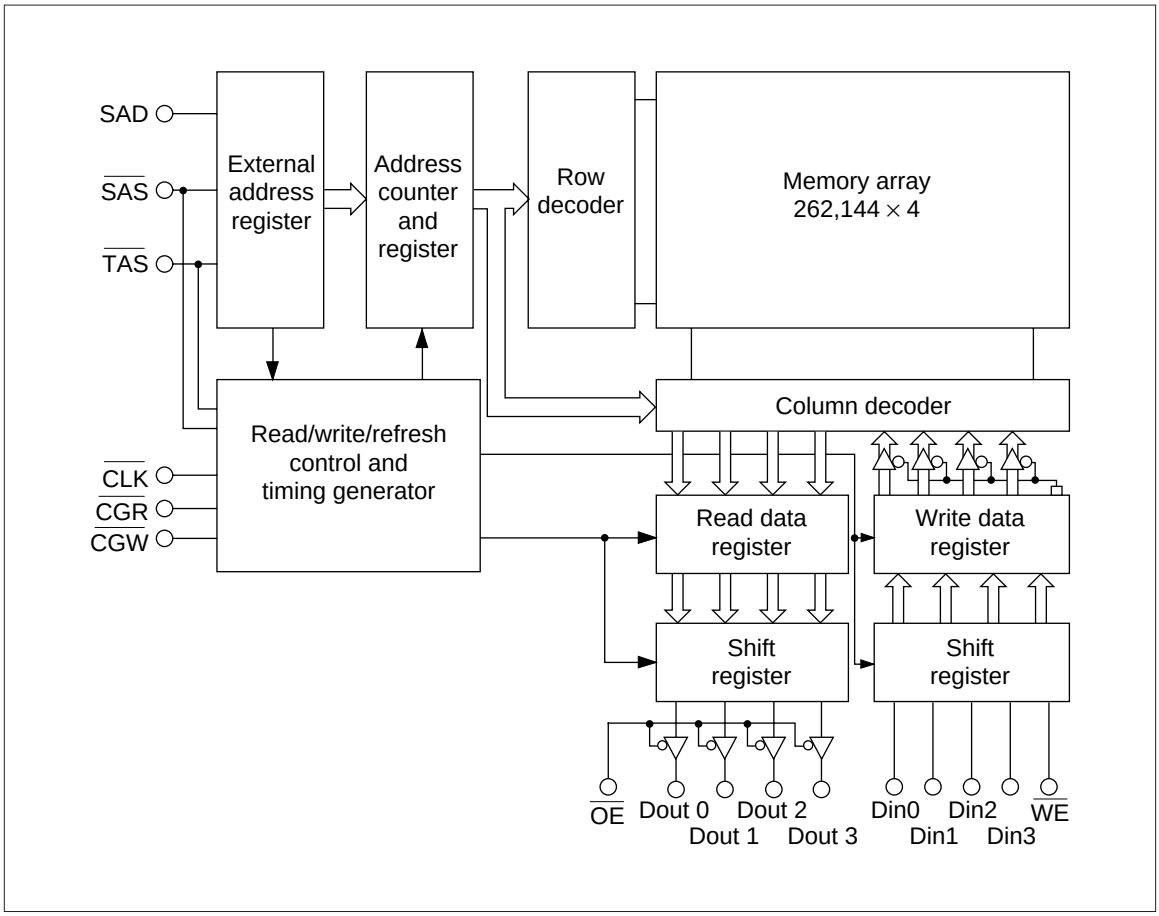


(Top view)

Pin Description

Pin Name	Function
Din	Data input
Dout	Data output
$\overline{OE}$	Output enable
$\overline{TAS}$	Transfer address strobe
$\overline{CLK}$	System clock
$\overline{CGW}$	Clock gate (write)
$\overline{CGR}$	Clock gate (read)
SAD	Serial address
$\overline{SAS}$	Serial address strobe
$\overline{WE}$	Write enable

Block Diagram



Functional Description

Serial Access Memory with Separate I/O

HM53051 read and write cycles can be operated independently, synchronized with a system clock. This allows time compression or picture expansion for picture-in-picture digital TV.

- Write cycle by CGW

Write data is clocked in at the falling edge of $\overline{CLK}$, when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter the write cycle (cycle time is defined by the system clock cycle) (figure 1). Time is compressed easily with $\overline{CGW}$.

- Read cycle by $\overline{CGR}$

Read data is output at the falling edge of the system clock, $\overline{CLK}$, when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter the read cycle (cycle time is defined by the system clock cycle). Read time is increased by increasing the $\overline{CGR}$ signal time (figure 2).

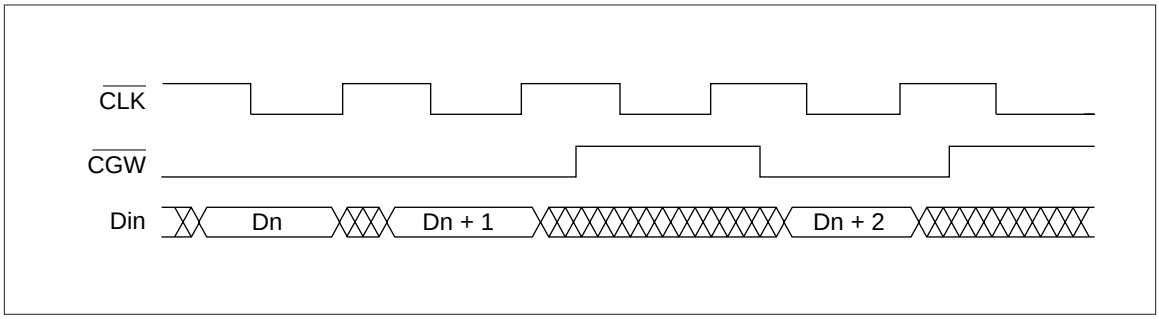


Figure 1 $\overline{CGW}$ Write Cycle

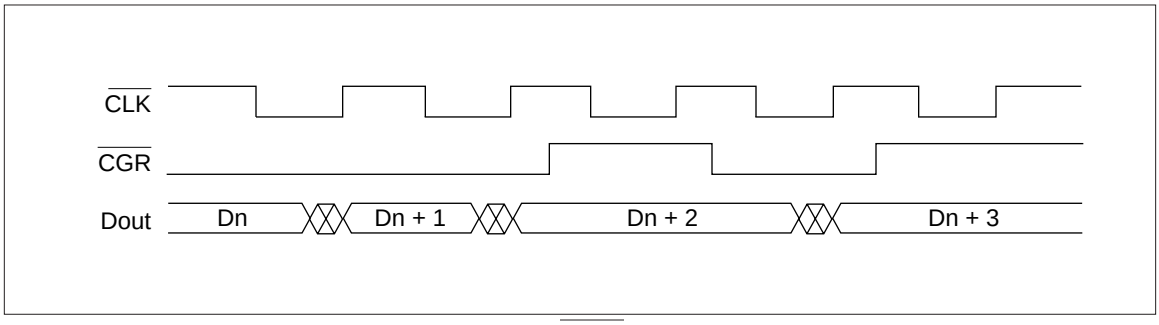


Figure 2 $\overline{CGR}$ Read Cycle

Random Access

The HM53051 is also capable of random access by serial address input (SAD). Random access (in 32-word × 4-bit blocks) is performed when $\overline{TAS}$ is low after read addresses (AR0–AR12), write addresses. (AW0–AW12), and mode setting flags $\overline{RF}$ (read flag), $\overline{WF}$ (write flag), and $\overline{MF}$ (mode flag) are read by SAD, synchronous with $\overline{SAS}$. The address specified by SAD increments automatically, assuring continuous data output (figure 3).

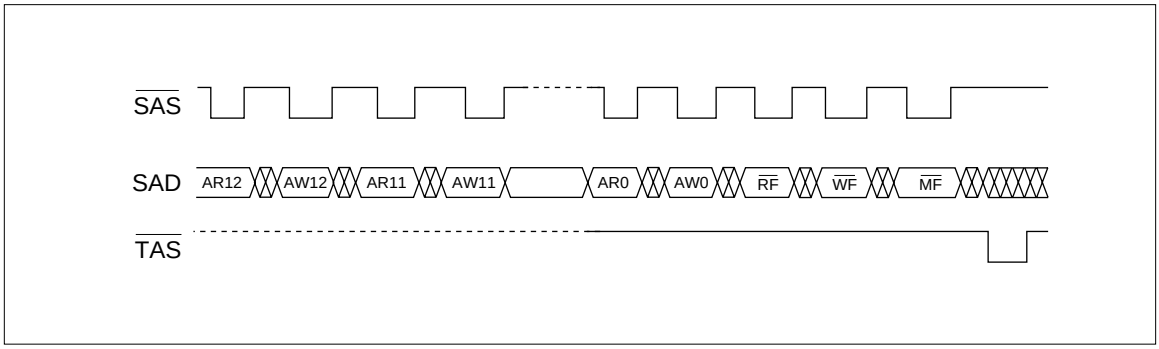


Figure 3 Random Access Timing

Mode Programming

Operation mode in HM53051 is programmed by the combination of five SAD bits.

MF	WF	RF	AW0	AR0	Mode
0	0	0	x	x	Write/read address asynchronous transfer
0	0	1	x	x	Write address asynchronous transfer
0	1	0	x	x	Read address asynchronous transfer
0	1	1	x	x	—
1	0	0	x	x	Write/read address synchronous transfer
1	0	1	x	x	Write address synchronous transfer
1	1	0	x	x	Read address synchronous transfer
1	1	1	1	1	System reset
1	1	1	0	0	Inhibit
1	1	1	0	1	
1	1	1	1	0	

Note: x = Don't care.

Read/Write Address Asynchronous Transfer Mode

- Read address asynchronous transfer mode 1 ($\overline{CGR}$ low)

The data block at read address AR, specified by SAD, is output starting from the 32nd system clock pulse after the rising edge of $\overline{TAS}$ (figure 4).

- Read address asynchronous transfer mode 2 ($\overline{CGR}$ high)

The data block at read address AR, specified by SAD, is output starting from the 32nd system clock after the falling edge of $\overline{TAS}$. If $\overline{CGR}$ goes low after the 33rd clock from the falling edge of $\overline{TAS}$, the data at read address AR (D2, D3, D4…) is output with synchronous $\overline{CLK}$ (while $\overline{CGR}$ is low) (figure 5).

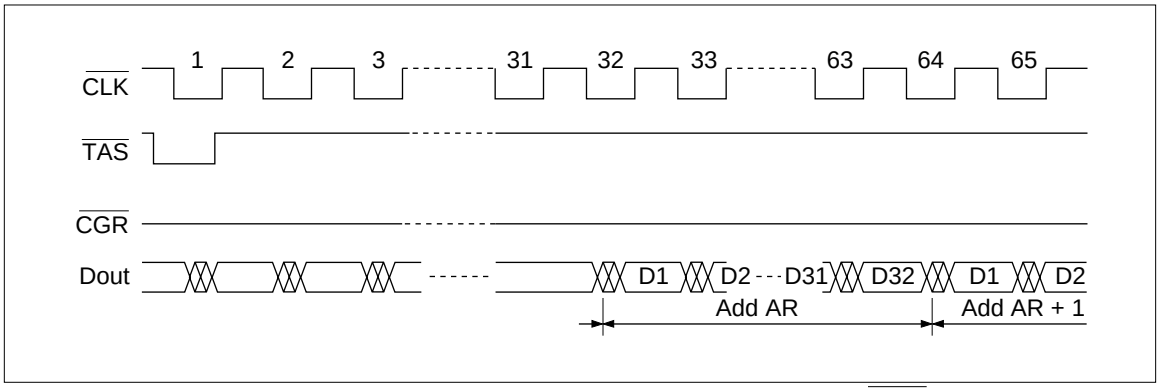


Figure 4 Read Address Asynchronous Transfer Mode 1 ($\overline{CGR}$ Low)

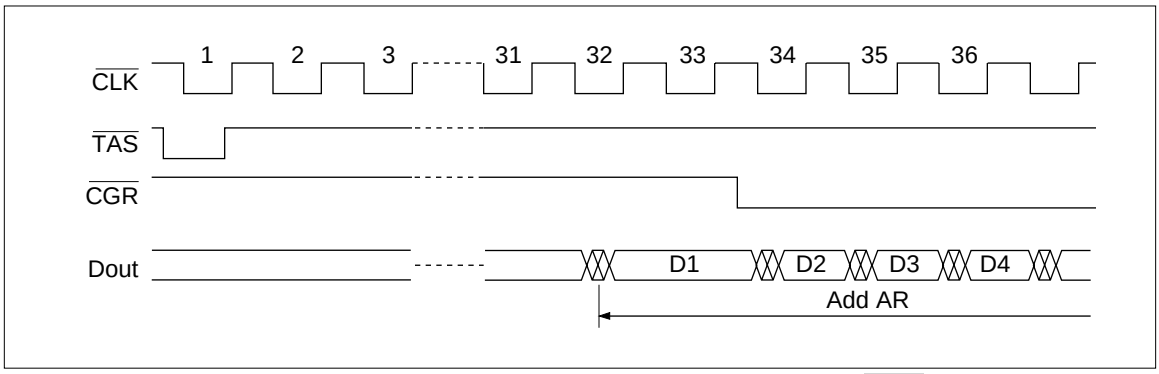


Figure 5 Read Address Asynchronous Transfer Mode 2 ($\overline{CGR}$ High)

- Write address asynchronous transfer mode 1 ($\overline{CGW}$ low)

The data block at write address AW, specified by SAD, is input starting from the first clock after the falling edge of $\overline{TAS}$ (figure 6).

- Write address asynchronous transfer mode 2 ($\overline{CGW}$ high)

If $\overline{CGW}$ goes low after the falling edge of $\overline{TAS}$, then the data block at write address AW is input with synchronous $\overline{CLK}$ (figure 7).

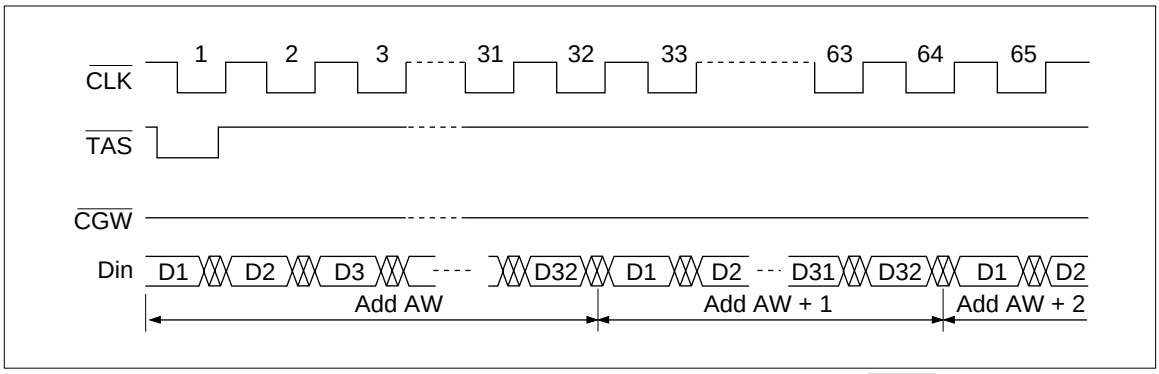


Figure 6 Write Address Asynchronous Transfer Mode 1 ($\overline{CGW}$ Low)

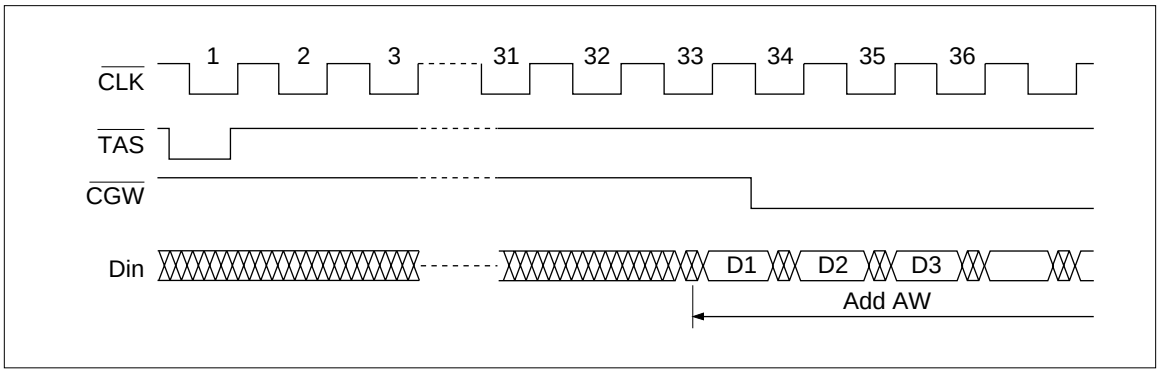


Figure 7 Write Address Asynchronous Transfer Mode 2 ($\overline{CGW}$ High)

Read/Write Address Synchronous Transfer Mode

- Read address synchronous transfer mode

When $\overline{TAS}$ goes low, the data block at read address AR, specified by SAD, is output after the data block at the present read address ARN, and the next address ARN + 1 is output (figure 8).

- Write address synchronous transfer mode

When $\overline{TAS}$ goes low, the data block being written is written to write address AW (figure 9).

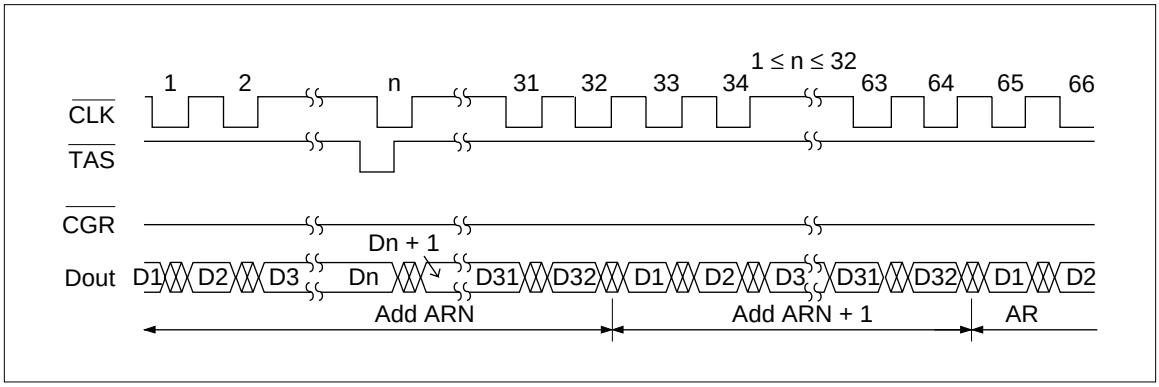


Figure 8 Read Address Synchronous Transfer Mode

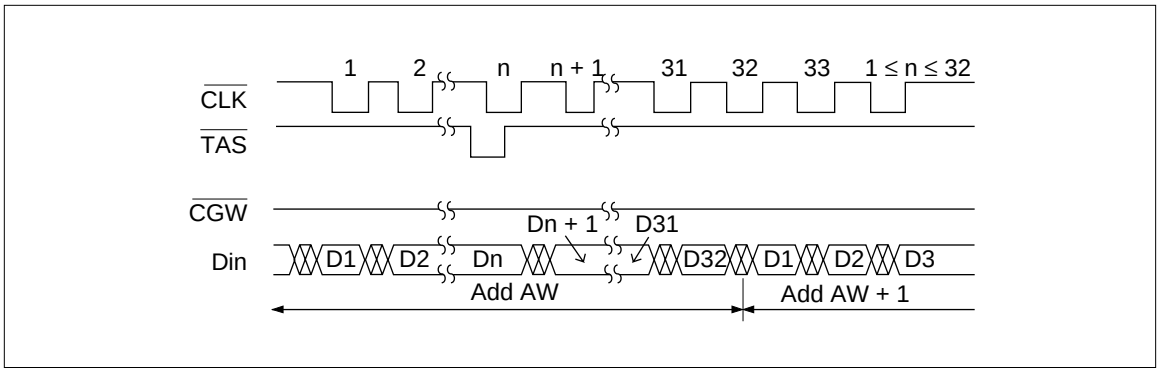


Figure 9 Write Address Synchronous Transfer Mode

System Reset Mode

System reset mode is the same as read/write address asynchronous transfer mode, except that the read/write addresses are reset to 0.

- System reset by SAD

System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0, and AR0 are all high.

- System reset by $\overline{SAS}$ and $\overline{TAS}$

System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of $\overline{CLK}$ (figure 10)

- 1 field delay

Field-delayed data is output when $\overline{CGR}$ and $\overline{CGW}$ turn to high before the system reset at the beginning of every field, and goes low simultaneously after the 33rd clock from system reset.

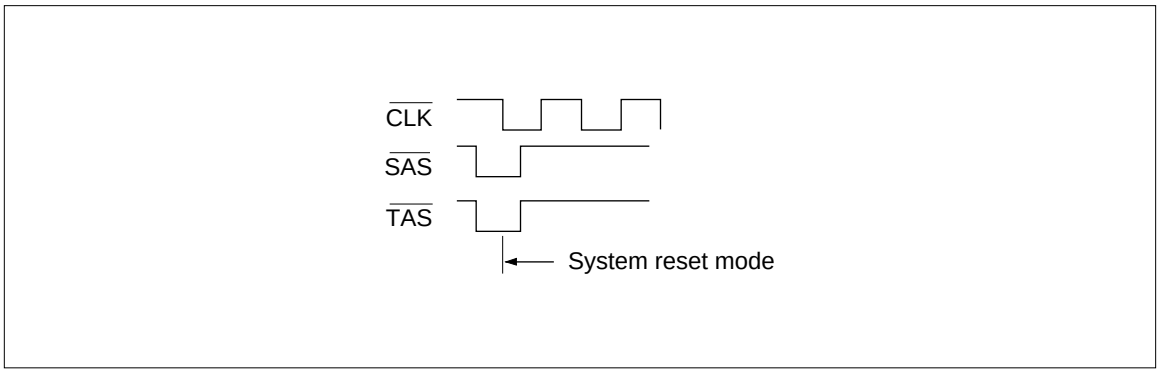


Figure 10 System Reset by $\overline{SAS}$ and $\overline{TAS}$

Using HM53051

• Input/output data of 32 words is not written or read in read/write address asynchronous transfer mode or during system reset. The data is written or read in blocks (32-word × 4-bit). Input data of less than 32 words is not written in write address asynchronous transfer mode or during system reset. When asynchronous read address transfer mode or system reset mode is activated, output from the current data block continues. When output data from the current data block is finished, the next data block is not read out if it has less than 32 words.

• Input data is not read out immediately. The data (32 word × 4-bit) is written into the memory array in the next 32 cycles after it is taken in. The data can be read out only after writing to the memory array is completed. If read address transfer mode is programmed after the 33 word clock from an input data block, new data can be read out. If this mode is programmed before the 33 word clock, new data or old data is output.

• Mode programming

Do not re-program read address transfer mode before a read operation of the previous read address transfer mode, or system reset mode, is completed. If the mode is re-programmed during a read operation, the address will be invalid, and the device may malfunction.

Do not re-program the write address transfer mode or system reset mode before a write operation of the previous write address transfer mode or system reset mode is completed. If the mode is re-programmed during a write operation, the address will be invalid, and the device may malfunction.

• Addresses must be set by read and write address asynchronous transfer or system reset 100 µsec after powerup. Before an address can be set, 32 $\overline{CLK}$ initialization cycles or more are required.

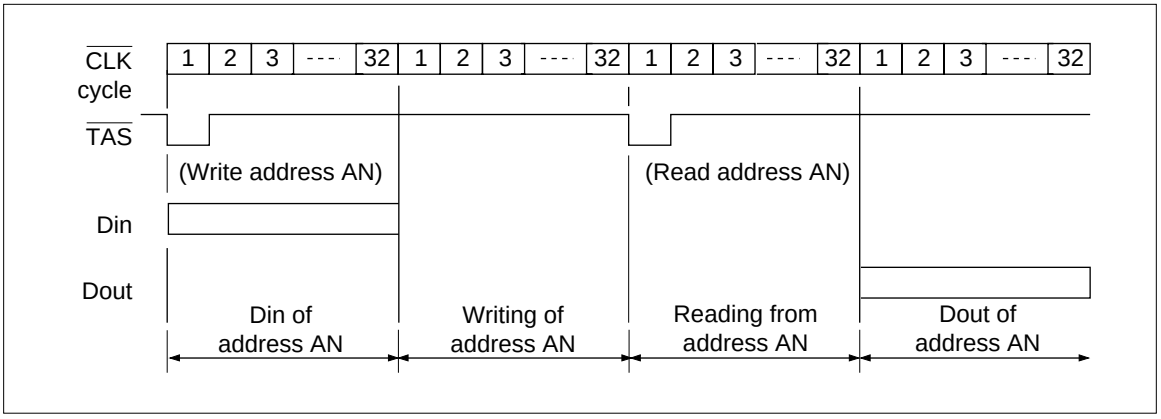


Figure 11 Read/Write Address Asynchronous Transfer Mode

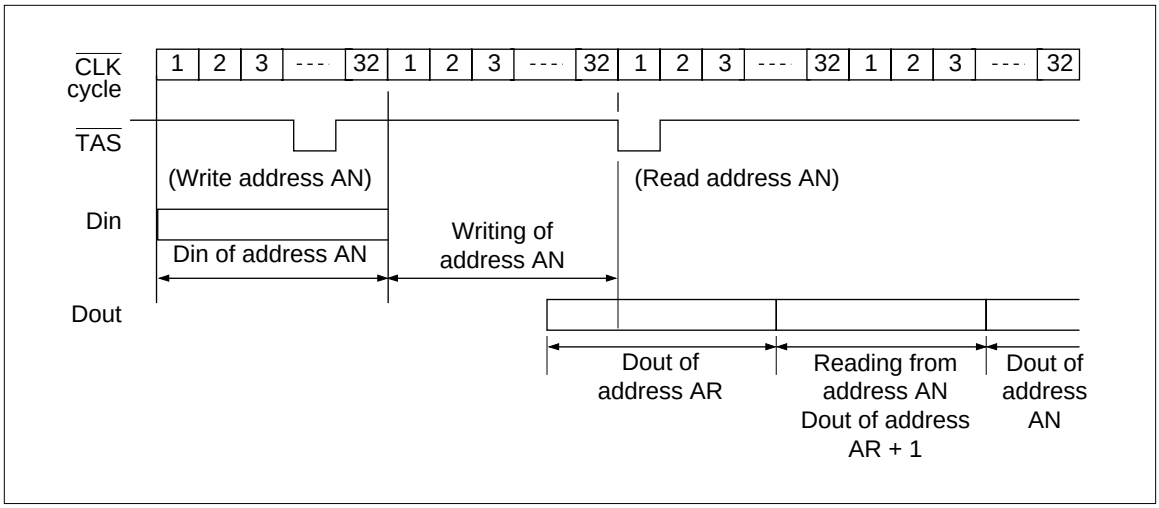


Figure 12 Read/Write Address Synchronous Transfer Mode

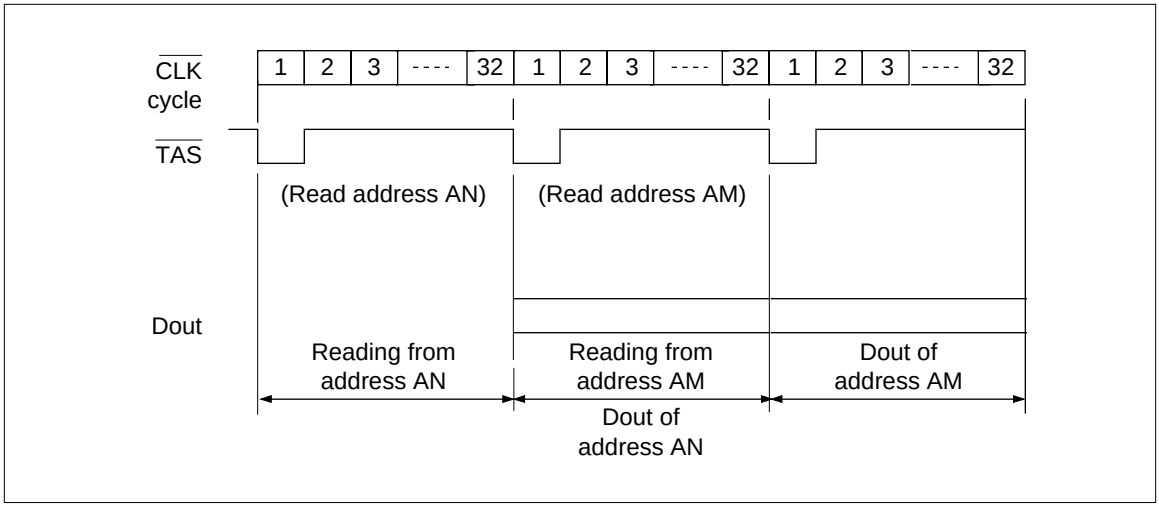


Figure 13 Read Address Asynchronous Transfer Mode

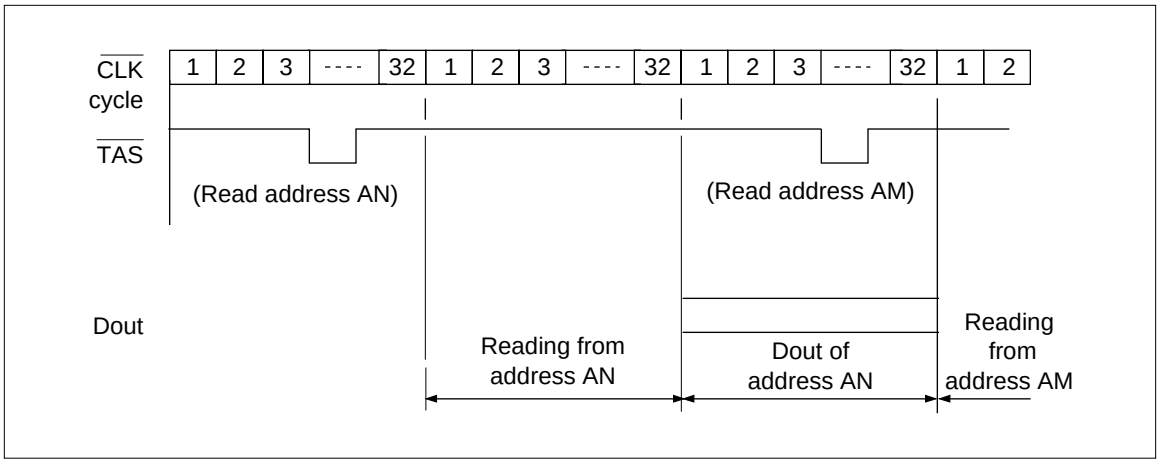


Figure 14 Read Address Synchronous Transfer Mode

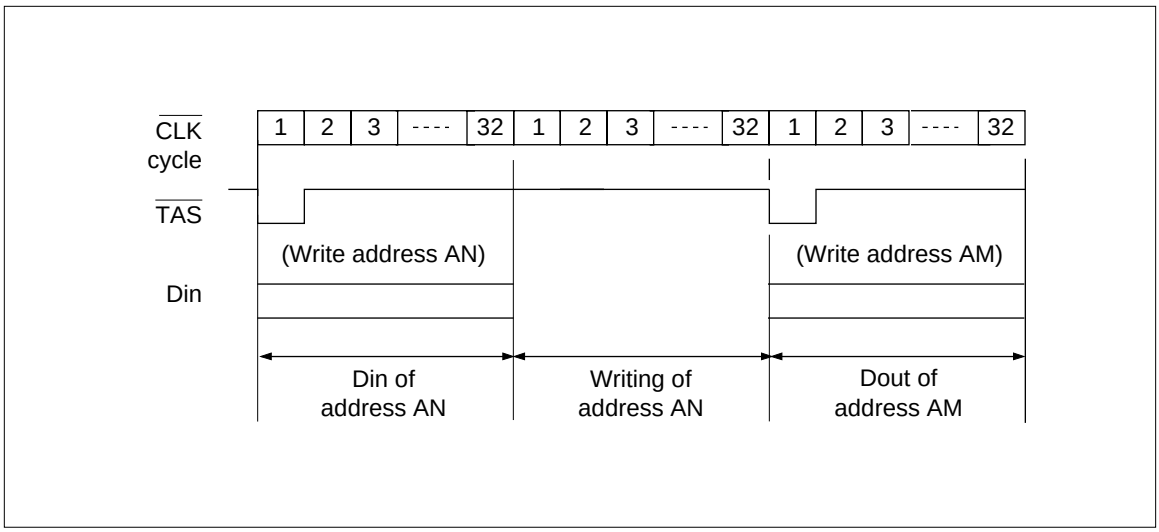


Figure 15 Write Address Asynchronous Transfer Mode

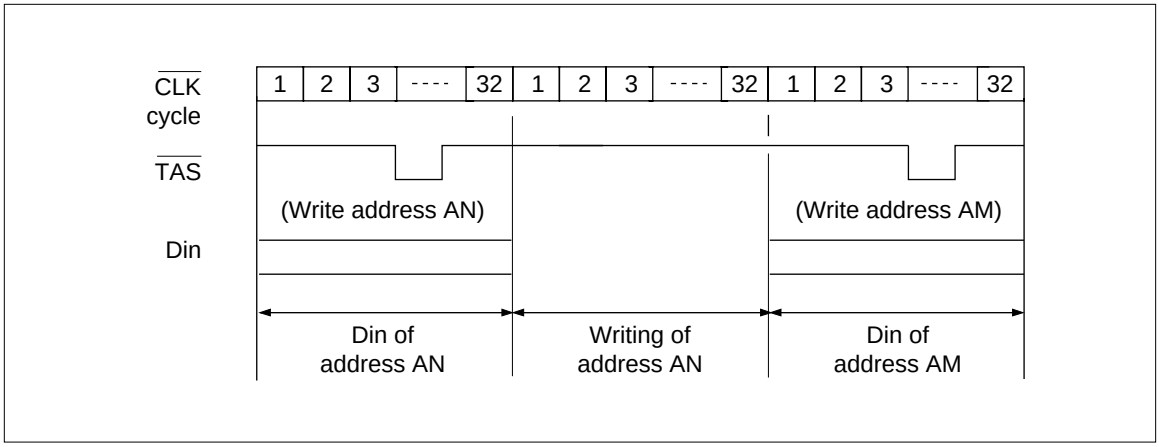


Figure 16 Write Address Synchronous Transfer Mode

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature (under bias)	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage ($\overline{CLK}$, $\overline{SAS}$)	V_{IH}	2.7	—	6.5	V
	V_{IL}	–0.5 *1	—	0.8	V
Input voltage($\overline{CLK}$, $\overline{SAS}$) (All pins except $\overline{CLK}$ and $\overline{SAS}$)	V_{IH}	2.4	—	6.5	V
	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. –3.0 V for pulse width ≤ l0 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM53051-34			HM53051-45/60				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Operating power supply current	I_{CC}	—	45	60	—	40	60	mA	Min cycle, Iout = 0 mA
Input leakage current	I_{LI}	–10	—	10	–10	—	10	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	–10	—	10	µA	OE = V_{IH}, Vout = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 4.2 mA
	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –2 mA

Home Print

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	5	pF	Vin = 0 V
Output capacitance	Cout	—	—	7	pF	Vout = 0 V

Note: These parameters are sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 5 ns
- Output load: 2 TTL + 50 pF (including scope and jig)

Read Cycle

Parameter	Symbol	HM53051-35 Min	HM53051-35 Max	HM53051-45 Min	HM53051-45 Max	HM53051-60 Min	HM53051-60 Max	Unit
System clock cycle time	t_{CC}	34	300	45	300	60	300	ns
$\overline{CLK}$ pulse width	t_{CL}	15	—	15	—	15	—	ns
	t_{CH}	15	—	15	—	15	—	ns
Access time from $\overline{CLK}$	t_{AC}	—	30	—	35	—	40	ns
Output hold time	t_{OH}	5	—	5	—	8	—	ns
Output enable access time	t_{OEA}	—	25	—	25	—	30	ns
Output enable to output in low Z	t_{OLZ}	5	—	5	—	5	—	ns
Output disable to output in high Z	t_{OHZ}	0	20	0	20	0	20	ns
$\overline{CGR}$ setup time	t_{GRS}	15	—	15	—	15	—	ns
$\overline{CGR}$ hold time	t_{GRH}	5	—	5	—	5	—	ns
$\overline{CGW}$ setup time	t_{GWS}	15	—	15	—	15	—	ns
$\overline{CGW}$ hold time	t_{GWH}	5	—	5	—	5	—	ns
Write command setup time	t_{WCS}	15	—	15	—	15	—	ns
Write command hold time	t_{WCH}	5	—	5	—	5	—	ns
Data input setup time	t_{DS}	15	—	15	—	15	—	ns
Data input hold time	t_{DH}	5	—	5	—	5	—	ns
$\overline{SAS}$ cycle time	t_{SC}	34	—	45	—	60	—	ns
$\overline{SAS}$ pulse width	t_{SL}	15	—	15	—	15	—	ns
	t_{SH}	15	—	15	—	15	—	ns
Serial address setup time	t_{SAS}	15	—	15	—	15	—	ns
Serial address hold time	t_{SAH}	5	—	5	—	5	—	ns
$\overline{SAS}$ setup time during mode programming	t_{SSH}	15	—	15	—	15	—	ns
$\overline{SAS}$ hold time during mode programming	t_{SHH}	5	—	5	—	5	—	ns
$\overline{TAS}$ setup time	t_{TS}	15	—	15	—	15	—	ns
$\overline{TAS}$ hold time	t_{TH}	5	—	5	—	5	—	ns
$\overline{SAS}$ setup time during system reset by $\overline{SAS}$/$\overline{TAS}$	t_{SSL}	15	—	15	—	15	—	ns
$\overline{SAS}$ hold time during system reset by $\overline{SAS}$/$\overline{TAS}$	t_{SHL}	5	—	5	—	5	—	ns

Timing Waveforms

• Read/write cycle

The write cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data is not written when $\overline{WE}$ is high. Time compression mode is realized by controlling $\overline{CGW}$. Read cycle starts when $\overline{CGR}$ is low. Time expansion mode is realized by controlling $\overline{CGR}$.

• Read cycle ($\overline{OE}$ control)

t_{OHZ} is defined by the time at which the output achieves the open circuit condition. t_{OLZ} and t_{OHZ} are sampled and are not 100% tested.

• Mode selection

$\overline{SAS}$ operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of $\overline{CLK}$, the address transfer cycle starts. $\overline{SAS}$ should be high during the address transfer cycle.

• $\overline{SAS}$ and $\overline{TAS}$ reset modes

The mode which was selected by SAD before $\overline{SAS}$ and $\overline{TAS}$ reset, if $\overline{SAS}$ and $\overline{TAS}$ are reset, should be changed because SAD is newly taken into by $\overline{SAS}$. The mode should be reselected by SAD after $\overline{SAS}$ and $\overline{TAS}$ reset.

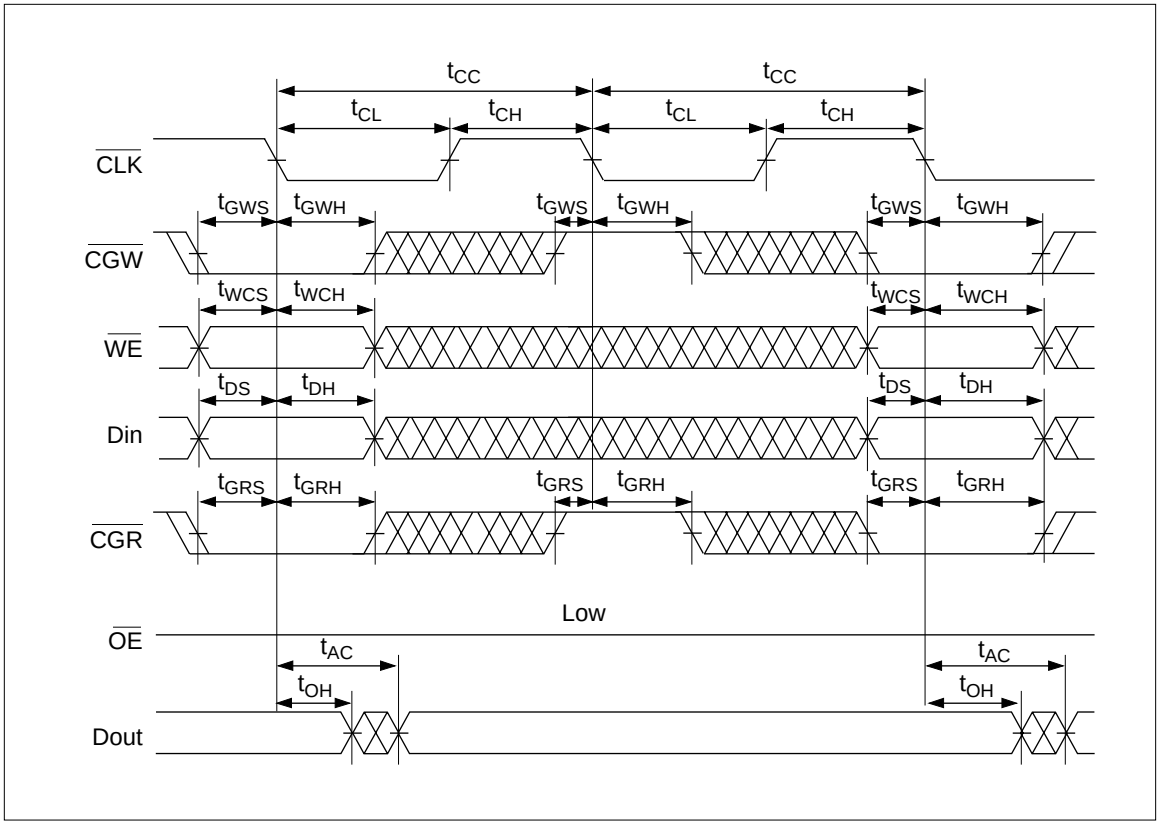


Figure 17 Read/Write Cycle

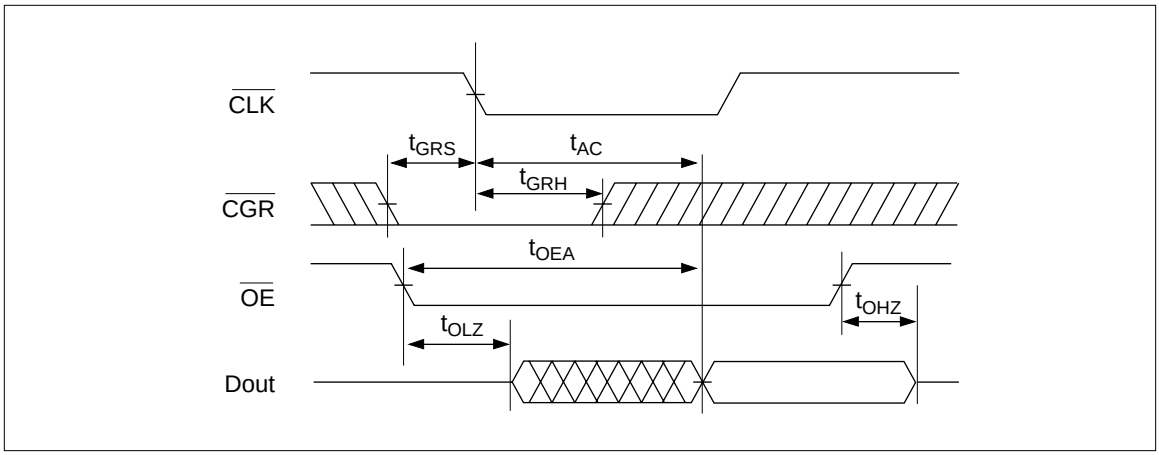


Figure 18 Read Cycle ($\overline{OE}$ Control)

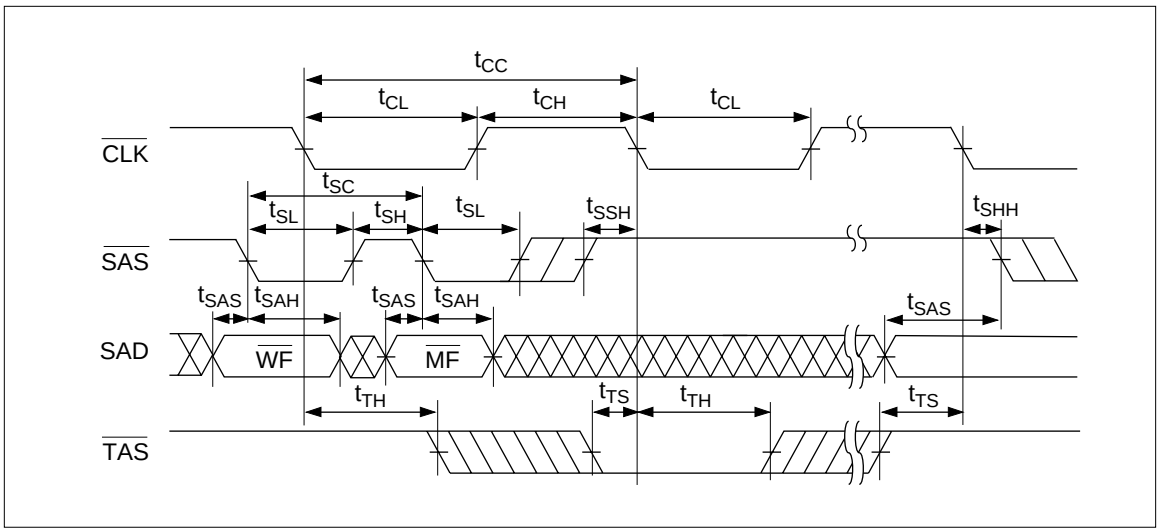


Figure 19 Mode Selection

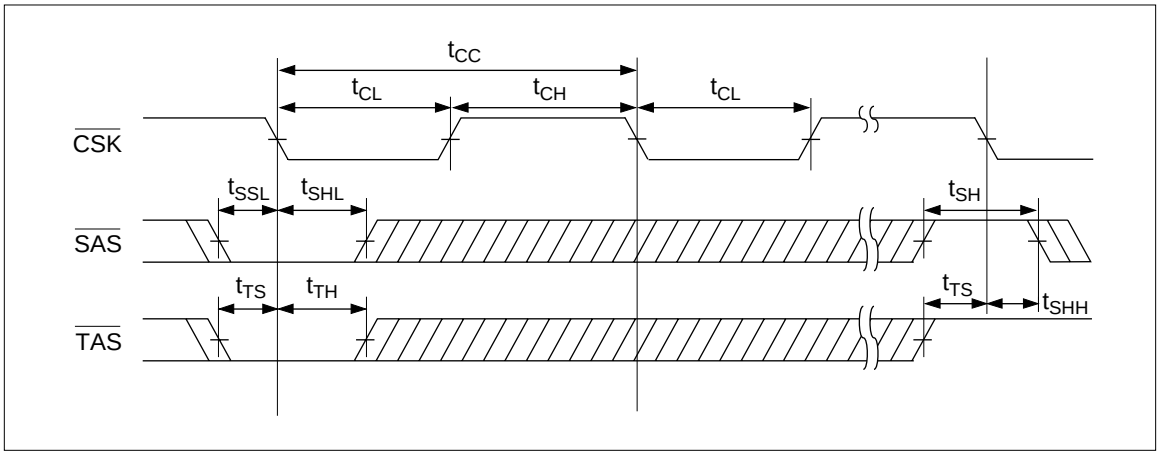


Figure 20 $\overline{SAS}$ and $\overline{TAS}$ Reset Mode