IP4853CX24

SD, MMC and microSD memory card integrated level shifter with PSU, EMI filter and ESD protection

Rev. 02 — 15 June 2009 Product data sheet

1. Product profile

1.1 General description

The IP4853CX24 is a device that fully integrates a bidirectional level shifter or voltage translator, EMI filter and ESD protection diodes. It is specifically designed to be used for memory card interfaces such as SD, microSD and MultiMediaCard (MMC) memory cards.

The integrated power supply unit supplies memory cards with 2.9 V directly from the battery. This enables a 1.8 V operating host-side device (e.g. a processor interface) to communicate with a 2.9 V compliant memory card using its integrated level shifter. Radiation from digital signals in the higher harmonics, close to typical mobile phone frequencies, is suppressed by the EMI filter.

The IP4853CX24 is fabricated using monolithic silicon technology in a Wafer Level Chip-Scale Package (WLCSP) with 0.4 mm pitch.

1.2 Features

- Dark Green compliant.
- Pb-free, RoHS compliant
- Integrated EMI filters
- Feedback channel for clock synchronization
- Integrated ESD protection according to IEC 61000-4-2, level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- SD memory card, microSD memory card and MMC interfaces in latest electronic appliances such as:
  - Mobile phone or smart phone
  - Digital camera
  - Card reader in (laptop) computer
- Appliances requiring one or several of the following features:
  - Level shifting and voltage translation from 1.8 V to 2.9 V and from 2.9 V to 1.8 V
  - ESD protection according to IEC 61000-4-2, level 4
  - Power supply regulation from battery to 2.9 V card memory voltage
  - EMI filtering
  - Integration of interface-specific biasing resistor network

2. Pinning information

2.1 Pinning

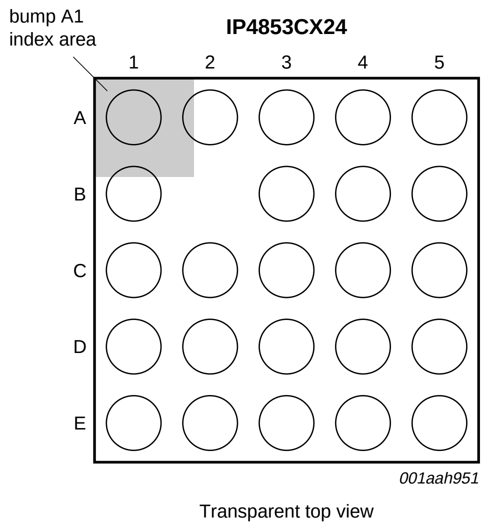


Fig 1. Pin configuration for WLCSP24 package

Table 1. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A1	DATA2_H	A2	DIR_CMD	A3	DIR_0	A4	V_{BAT}	A5	DATA2_SD
B1	DATA3_H	B2	n.c.	B3	V_{CC}	B4	VSD	B5	DATA3_SD
C1	CLK_IN	C2	ENABLE	C3	GND	C4	GND	C5	CLK_SD
D1	DATA0_H	D2	CMD_H	D3	CD	D4	CMD_SD	D5	DATA0_SD
E1	DATA1_H	E2	CLK_FB	E3	DIR_1_3	E4	WP	E5	DATA1_SD

2.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Description
DATA2_H	A1	I/O	data 2 input or output on host-side
DIR_CMD	A2	I	direction control input for command
DIR_0	A3	I	direction control input for data 0
V_{BAT}	A4	S	supply voltage from battery for regulator
DATA2_SD	A5	I/O	data 2 input or output on memory card-side
DATA3_H	B1	I/O	data 3 input or output on host-side
n.c.	B2	-	not connected
V_{CC}	B3	S	supply voltage for host-side circuits
VSD	B4	O	output supply voltage for memory card
DATA3_SD	B5	I/O	data 3 input or output on memory card-side
CLK_IN	C1	I	clock signal input

Table 2. Pin description *…continued*

Symbol[1]	Pin	Type[2]	Description
ENABLE	C2	I	device enable input
GND	C3	S	supply ground
GND	C4	S	supply ground
CLK_SD	C5	O	clock signal output on memory card-side
DATA0_H	D1	I/O	data 0 input or output on host-side
CMD_H	D2	I/O	command input or output on host-side
CD	D3	O	card detect switch biasing output
CMD_SD	D4	I/O	command input or output on memory card-side
DATA0_SD	D5	I/O	data 0 input or output on memory card-side
DATA1_H	E1	I/O	data 1 input or output on host-side
CLK_FB	E2	O	clock feedback output to host
DIR_1_3	E3	I	direction control input for data 1, data 2 and data 3
WP	E4	O	write protect switch biasing output
DATA1_SD	E5	I/O	data 1 input or output on memory card-side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards.

[2] I = input, O = output, I/O = input and output, S = power supply.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
IP4853CX24	WLCSP24	wafer level chip-size package; 24 bumps; 2.01 × 2.01 × 0.61 mm	IP4853CX24

4. Block diagram

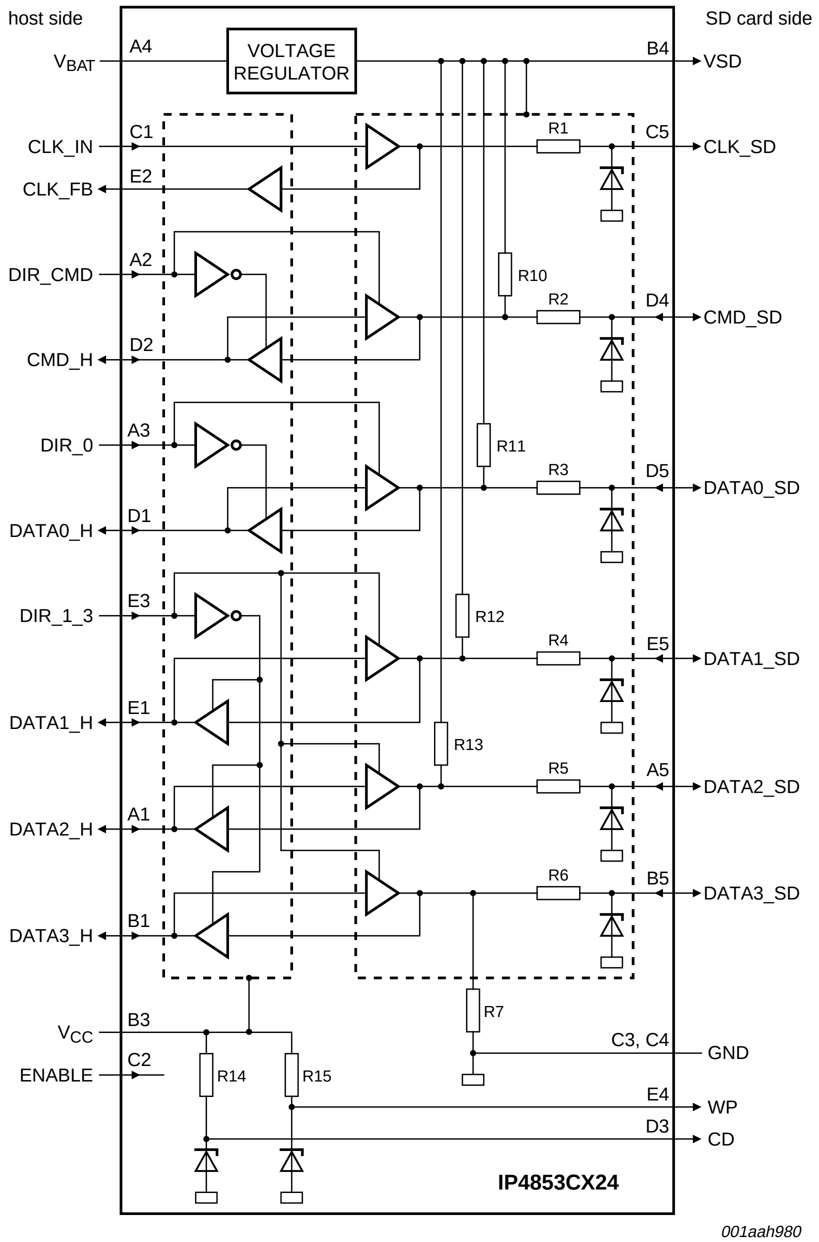


Fig 2. Block diagram

5. Functional description

5.1 Logic control signals

Table 4. Control signal truth table

$V_{BAT} \geq 2.7$ V.

Control		Host-side		Memory card-side	
Pin	**Level[1]**	**Pin**	**Function**	**Pin**	**Function**
Pin ENABLE = HIGH and $V_{CC} \geq 1.62$ V					
DIR_CMD	H	CMD_H	input	CMD_SD	output
	L	CMD_H	output	CMD_SD	input
DIR_0	H	DATA0_H	input	DATA0_SD	output
	L	DATA0_H	output	DATA0_SD	input
DIR_1_3	H	DATA1_H, DATA2_H, DATA3_H	input	DATA1_SD, DATA2_SD, DATA3_SD	output
	L	DATA1_H, DATA2_H, DATA3_H	output	DATA1_SD, DATA2_SD, DATA3_SD	input
-	-	CLK_FB	output	CLK_SD	output
Pin ENABLE = LOW or $V_{CC} \leq 0.8$ V					
DIR_CMD	X	CMD_H	high-Z	CMD_SD	high-Z
DIR_0	X	DATA0_H	high-Z	DATA0_SD	high-Z
DIR_1_3	X	DATA1_H, DATA2_H, DATA3_H	high-Z	DATA1_SD, DATA2_SD, DATA3_SD	high-Z
-	-	CLK_FB	high-Z	CLK_SD	high-Z

[1] H = HIGH; L = LOW and X = don’t care.

6. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+3.5	V
V_{BAT}	battery supply voltage	4 ms transient	–0.5	+5.5	V
		operating	–0.5	+5.0	V
V_I	input voltage	at I/O pins			
		4 ms transient	–0.5	+5.5	V
		operating	–0.5	+5.0	V
P_{tot}	total power dissipation	T_{amb} = –30 °C to +70 °C	-	550	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–30	+85	°C
V_{ESD}	electrostatic discharge voltage	pin V_{BAT} and all memory card-side pins to ground; according to IEC 61000-4-2, level 4			
		contact	-	±8000	V
		air discharge	-	±15000	V
		all other pins to ground; according to IEC 61340-3-1, human body model	-	±2000	V

7. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.62	2.1	V
V_{BAT}	battery supply voltage		2.7[1]	5.0	V
V_I	input voltage	host-side	0	2.1	V
		memory card-side; $V_{BAT} \geq 3.2$ V	0	2.9	V
V_O	output voltage	active mode; pin ENABLE = HIGH			
		host-side	0	V_{CC}	V
		memory card-side	0	$V_{O(reg)}$	V
$\Delta t/\Delta V$	time difference over voltage change	host-side; between $0.2V_{CC}$ and $0.7V_{CC}$	-	2	ns/V
		memory card-side; between $0.2V_{O(reg)}$ and $0.7V_{O(reg)}$	-	2	ns/V

[1] The device is still fully functional, but the voltage on pin VSD might drop below the recommended memory card supply voltage.

8. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; T_{amb} = −30 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Voltage regulator output: pin VSD							
$V_{O(reg)}$	regulator output voltage	C_L = 1 μF					
		$I_{O(reg)}$ = 0 A		-	2.9	2.987	V
		$I_{O(reg)}$ = 200 mA; V_{BAT} ≥ 2.9 V		2.75	-	-	V
$\Delta V_{do(reg)}$	regulator dropout voltage variation	$I_{O(reg)}$ = 200 mA		-	-	150	mV
$I_{O(reg)}$	regulator output current			-	200	-	mA
$I_{O(sc)}$	short-circuit output current			-	-	500	mA
$I_{q(reg)}$	regulator quiescent current	pin ENABLE = HIGH (active mode)		-	-	200	μA
		pin ENABLE = LOW (not active mode)		-	-	2	μA
C_{ext}	external capacitance	recommended capacitor at pin VSD		-	1.0	-	μF
Control and data inputs							
Host-side: pins ENABLE, DIR_0, DIR_1_3, DIR_CMD, CLK_IN and DATA0_H to DATA3_H							
V_{IH}	HIGH-level input voltage			0.65 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3	V
C_{ch}	channel capacitance	V_I = 0 V; f_i = 1 MHz	[2]	-	-	20	pF
Memory card-side: pins CMD_SD and DATA0_SD to DATA3_SD							
V_{IH}	HIGH-level input voltage			0.65 × $V_{O(reg)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3	V
C_{ch}	channel capacitance	V_I = 0 V; f_i = 1 MHz	[2]	-	-	20	pF
Control and data outputs							
Host-side: pins CLK_FB, CMD_H and DATA0_H to DATA3_H							
V_{OH}	HIGH-level output voltage	I_O = −3 mA; V_I = V_{IH}		V_{CC} − 0.45	-	-	V
V_{OL}	LOW-level output voltage	I_O = 3 mA; V_I = V_{IL}		-	-	0.45	V
Memory card-side: pins CLK_SD, CMD_SD and DATA0_SD to DATA3_SD, CD and WP							
V_{OH}	HIGH-level output voltage	I_O = −6 mA; V_I = V_{IH}		$V_{O(reg)}$ − 0.45	-	-	V
V_{OL}	LOW-level output voltage	I_O = 6 mA; V_I = V_{IL}		-	-	0.45	V
I_{LRzd}	Zener diode reverse leakage current	V_I = 3 V		-	-	100	nA
R_s	series resistance	R1 to R6; tolerance ±20 %		32	40	48	Ω
R_{pd}	pull-down resistance	R7; tolerance ±30 %		329	470	611	kΩ
R_{pu}	pull-up resistance	R10; tolerance ±30 %		10.5	15	19.5	kΩ
		R11 to R13; tolerance ±30 %		49	70	91	kΩ
		R14 and R15; tolerance ±30 %		70	100	130	kΩ

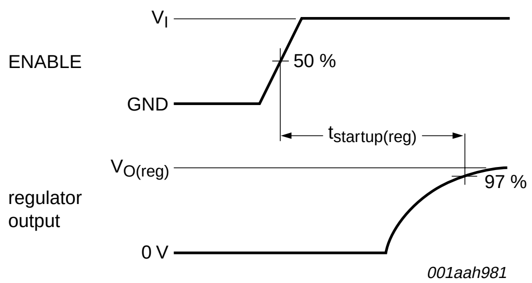
[1] Typical values are measured at T_{amb} = 25 °C.

[2] EMI filter line capacitance per data channel from I/O pin to driver; C_{ch} is guaranteed by design.

9. Dynamic characteristics

Table 8. Voltage regulator
T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage regulator output: pin VSD						
PSRR	power supply rejection ratio	V_{BAT} = 3.0 V; $V_{ripple(p-p)}$ = 223.6 mV (0 dBm); R_{source} = 50 Ω				
		f_{ripple} = 1 kHz	40	-	-	dB
		f_{ripple} = 10 kHz	30	-	-	dB
$t_{startup(reg)}$	regulator start-up time	V_{CC} = 1.8 V; V_{BAT} = 3.0 V; $I_{O(reg)}$ = 200 mA; C_L = 1 μF; see Figure 3	-	-	200	μs



Measuring points: ENABLE signal at $0.5V_{CC}$ and regulator output signal at $0.97V_{O(reg)}$.

Fig 3. Regulator start-up time

Table 9. Frequency response of integrated EMI filters
T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock, command and data channels[1]						
α_{il}	insertion loss	R_{source} = 50 Ω; C_L = 10 pF; R_L = 50 Ω				
		f_i = 401 MHz to 800 MHz	9	-	-	dB
		f_i = 801 MHz to 1.4 GHz	-	17	-	dB
		f_i = 1.4 GHz to 6.0 GHz	-	32	-	dB

[1] Guaranteed by design.

Table 10. Output rise and fall times

V_{BAT} = 3.5 V; $V_{O(reg)}$ = 2.9 V; unless otherwise specified; transition time is the same as output rise time and output fall time; see Figure 4 for timing diagram and Figure 5 for test circuit.

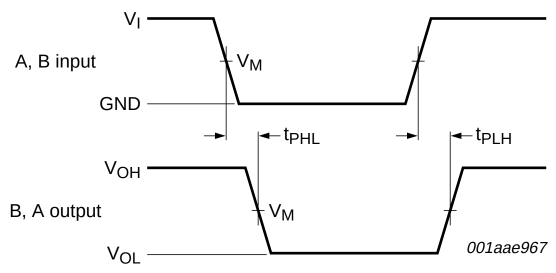
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Memory card-side outputs: pins CLK_SD, CMD_SD and DATA0_SD to DATA3_SD						
Reference points at 70 % and 20 %						
t_t	transition time	C_L = 20 pF; R_L = 100 kΩ				
		T_{amb} = +25 °C; V_{CC} = 1.8 V	-	1.5	2.5	ns
		T_{amb} = –30 °C; V_{CC} = 1.9 V	-	1.5	2.5	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V	-	1.8	2.8	ns
		C_L = 40 pF; R_L = 100 kΩ				
		T_{amb} = +25 °C; V_{CC} = 1.8 V	-	2.7	3.6	ns
		T_{amb} = –30 °C; V_{CC} = 1.9 V	-	2.7	3.6	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V	-	2.9	3.8	ns
Reference points at 90 % and 10 %						
t_t	transition time	C_L = 20 pF; R_L = 100 kΩ				
		T_{amb} = +25 °C; V_{CC} = 1.8 V	-	3.0	4.2	ns
		T_{amb} = –30 °C; V_{CC} = 1.9 V	-	2.9	4.1	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V	-	3.7	4.9	ns
Host-side outputs: pins CLK_FB, CMD_H and DATA0_H to DATA3_H						
Reference points at 70 % and 20 %						
t_t	transition time	C_L = 5 pF; R_L = 100 kΩ				
		T_{amb} = +25 °C; V_{CC} = 1.8 V	-	1.5	2.4	ns
		T_{amb} = –30 °C; V_{CC} = 1.9 V	-	1.3	2.3	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V	-	1.6	2.5	ns
		C_L = 20 pF; R_L = 100 kΩ				
		T_{amb} = +25 °C; V_{CC} = 1.8 V	-	1.7	2.9	ns
		T_{amb} = –30 °C; V_{CC} = 1.9 V	-	1.4	2.5	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V	-	1.8	3.0	ns
Reference points at 90 % and 10 %						
t_t	transition time	C_L = 5 pF; R_L = 100 kΩ				
		T_{amb} = +25 °C; V_{CC} = 1.8 V	-	2.4	3.1	ns
		T_{amb} = –30 °C; V_{CC} = 1.9 V	-	2.3	3.0	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V	-	2.5	3.2	ns

Table 11. Propagation delay of time domain response driver part

V_{BAT} = 3.5 V; $V_{O(reg)}$ = 2.9 V; R_{source} = 50 Ω; propagation delay measurements include PCB delays and connectors; see Figure 4 for timing diagram and Figure 5 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Host-side inputs to memory card-side outputs							
t_{PD}	propagation delay	nominal case; T_{amb} = +27 °C; V_{CC} = 1.8 V	[1]				
		C_L = 20 pF		6.2	7.0	7.8	ns
		C_L = 40 pF		7.3	8.2	9.1	ns
		best case; T_{amb} = −30 °C; V_{CC} = 1.9 V					
		C_L = 20 pF		5.7	6.5	7.3	ns
		C_L = 40 pF		6.5	7.5	8.5	ns
		worst case; T_{amb} = +70 °C; V_{CC} = 1.62 V					
		C_L = 20 pF		6.7	7.8	8.9	ns
		C_L = 40 pF		7.5	8.8	10.1	ns
Memory card-side inputs to host-side outputs							
t_{PD}	propagation delay	nominal case; T_{amb} = +27 °C; V_{CC} = 1.8 V	[1]				
		C_L = 5 pF		4.2	6.0	7.8	ns
		C_L = 20 pF		6.3	7.2	8.1	ns
		best case; T_{amb} = −30 °C; V_{CC} = 1.9 V					
		C_L = 5 pF		4	5.9	6.9	ns
		C_L = 20 pF		5.1	6.7	8.5	ns
		worst case; T_{amb} = +70 °C; V_{CC} = 1.62 V					
		C_L = 5 pF		5.4	6.5	7.7	ns
		C_L = 20 pF		6.7	8.0	9.2	ns
Host-side pins CLK_IN to CLK_FB							
t_{PD}	propagation delay	nominal case; T_{amb} = +27 °C; V_{CC} = 1.8 V	[1]				
		C_L = 5 pF		7.6	9.2	10.7	ns
		C_L = 20 pF		8.2	9.9	11.6	ns
		best case; T_{amb} = −30 °C; V_{CC} = 1.9 V					
		C_L = 5 pF		6.7	8.1	9.5	ns
		C_L = 20 pF		7.6	8.8	10.5	ns
		worst case; T_{amb} = +70 °C; V_{CC} = 1.62 V					
		C_L = 5 pF		8.5	10.7	12.9	ns
		C_L = 20 pF		9.1	11.4	13.9	ns

[1] t_{PD} is the same as HIGH-to-LOW propagation delay (t_{PHL}) and LOW-to-HIGH propagation delay (t_{PLH}).



Measuring points: host-side at $0.5V_{CC}$ and memory card-side at $0.5V_{O(reg)}$.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Output rise and fall times and data input to output propagation delay times (host-side to card-side or card-side to host-side)

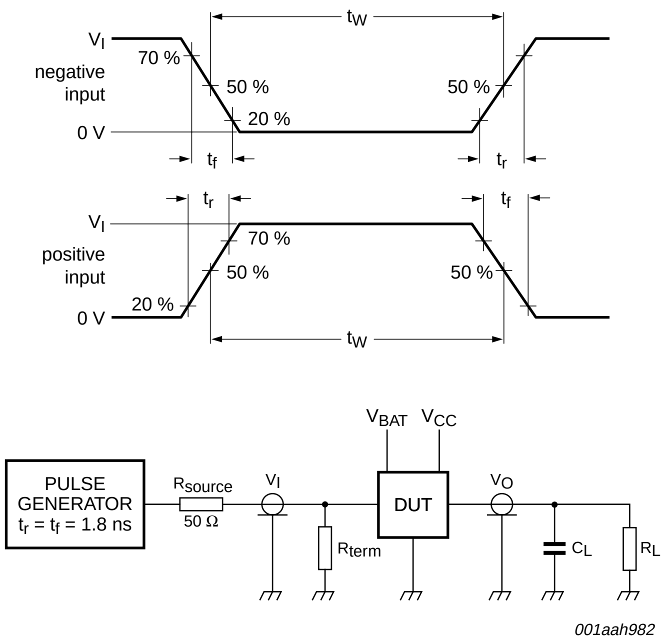
Table 12. Power dissipation per channel

V_{CC} = 1.8 V; V_{BAT} = 4 V; all values are typical; memory card-side C_L = 20 pF and host-side C_L = 5 pF.

Frequency (MHz)	I_{BAT} (mA)	I_{CC} (mA)	P (mW)[1]
Host-side input to memory card-side output			
Data channel			
1.0	0.79	0.002	3.16
10.0	3.30	0.020	13.3
20.0	5.79	0.037	23.2
50.0	12.3	0.090	49.4
Clock channel			
1.0	0.44	0.05	1.85
10.0	3.1	0.59	13.5
20.0	5.4	0.97	23.4
50.0	12.2	2.36	53.1
Memory card-side input to host-side output			
Data channel			
1.0	0.18	0.1	0.9
10.0	0.42	0.96	3.41
20.0	0.66	1.91	6.1
50.0	1.4	4.5	13.7

[1] Power consumption is largely dependent on capacitive load connected to a driver output: $P = V_{CC} \times I_{CC} + V_{BAT} \times I_{BAT}$.

10. Test information



Definitions test circuit:

R_{source} = source resistance of pulse generator.

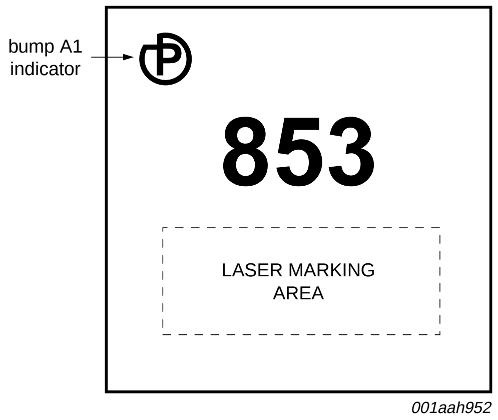
R_{term} = termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Fig 5. Load circuitry for measuring switching time

11. Marking

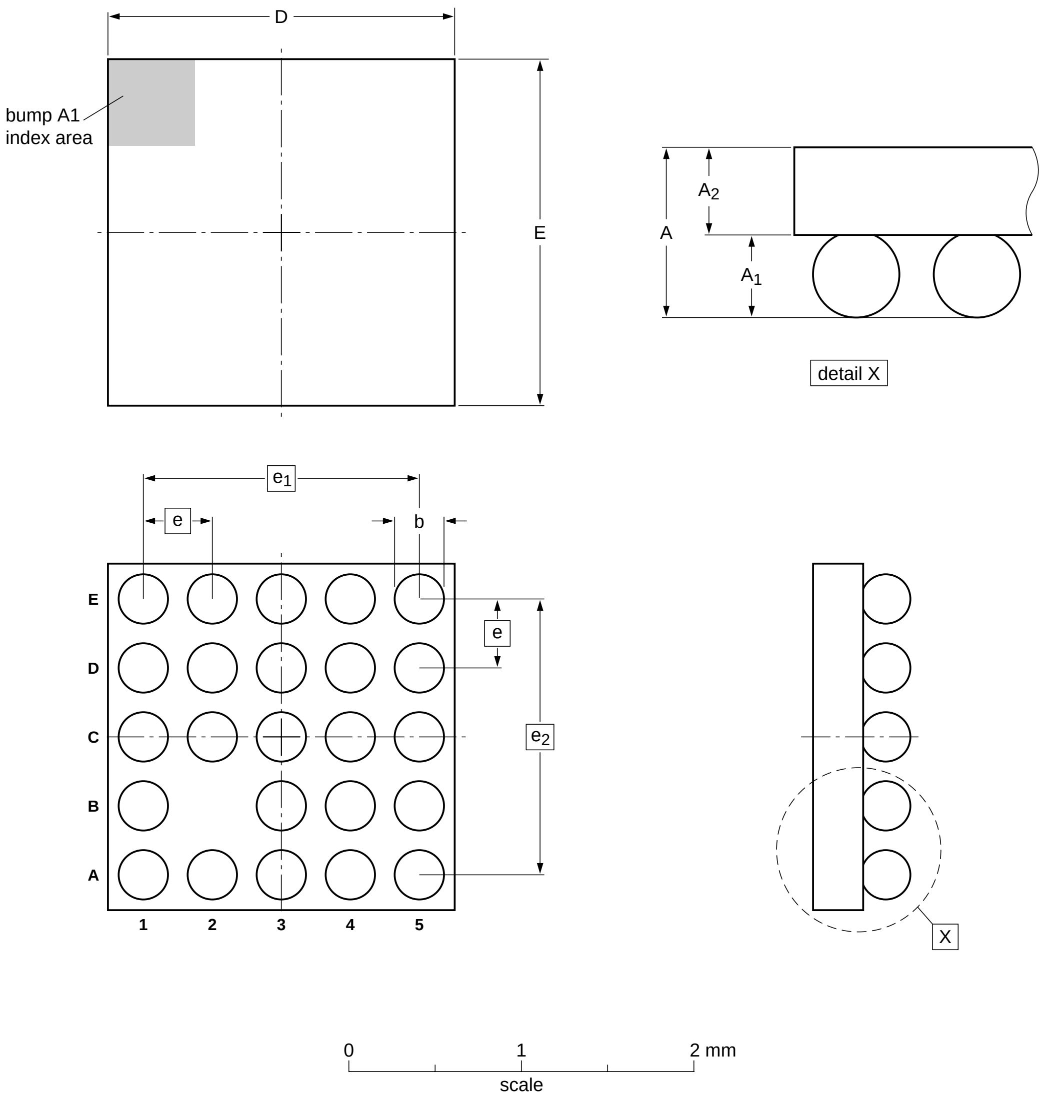


top view

Fig 6. Marking of IP4853CX24

12. Package outline

WLCSP24: wafer level chip-size package; 24 bumps; 2.01 x 2.01 x 0.61 mm **IP4853CX24**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2
mm	max	0.66	0.22	0.44	0.29	2.06	2.06	0.4	1.6	1.6
	nom	0.61	0.20	0.41	0.26	2.01	2.01			
	min	0.56	0.18	0.38	0.23	1.96	1.96			

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
IP4853CX24						~~08-04-14~~ 09-06-11

Fig 7. Package outline IP4853CX24 (WLCSP24)

13. Packing information

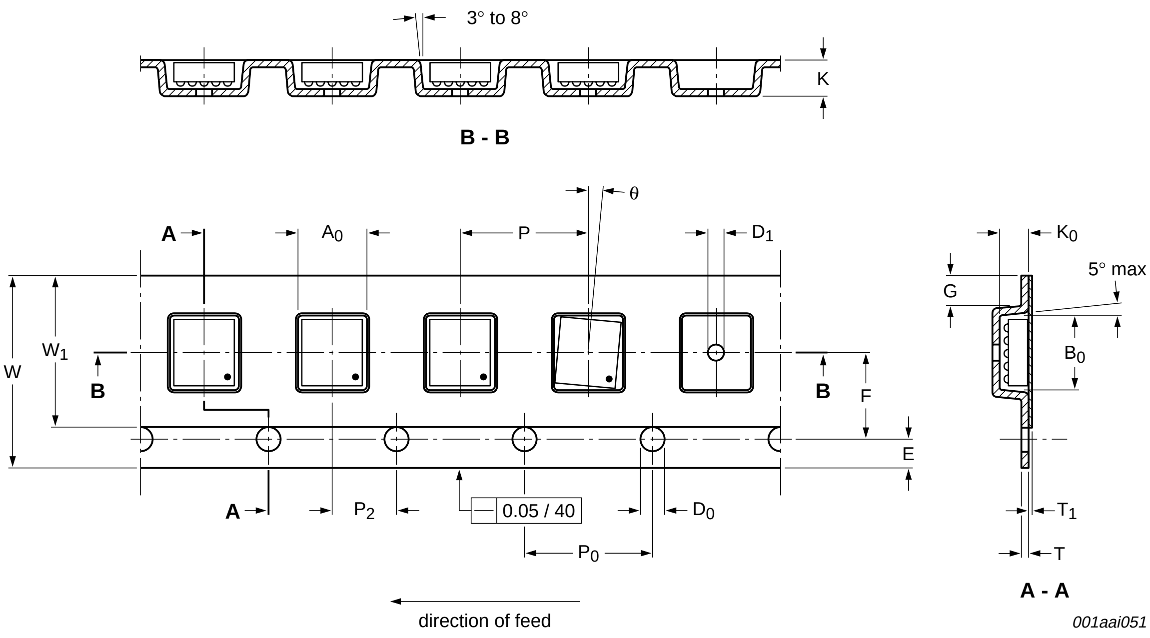


Fig 8. Tape and reel information

Table 13. Tape dimensions

Description	Item	Symbol	Specification (mm)	
			Dimension	Tolerance
Overall dimensions	tape width	W	8.00	±0.1
	thickness	K	1.20	max.
	distance	G	0.75	min.
Sprocket holes[1]	diameter	D_0	1.50	+0.1
	distance	E	1.75	±0.1
	pitch	P_0	4.00	±0.1
Distance between center lines	length direction	P_2	2.00	±0.05
	width direction	F	3.50	±0.05
Compartments	length	A_0	2.20	±0.05
	width	B_0	2.20	±0.05
	depth	K_0	0.80	±0.05
	hole diameter	D_1	0.50	+0.1
	pitch	P	4.00	±0.1
Device	rotation	θ	20°	max.
Carrier tape antistatic[2]	film thickness	T	0.25	±0.07
Cover tape[3]	width	W_1	5.75	max.
	film thickness	T_1	0.1	max.
Bending radius	in winding direction	R	30	min.

[1] Cumulated pitch error: ±0.2 mm per 10 pitches.

[2] Carbon loaded polystyrene 100 % recyclable.

[3] The cover tape shall not overlap the sprocket holes.

14. Design and assembly recommendations

14.1 PCB design guidelines

To achieve optimum performance it is recommended to use a Non-Solder Mask Design (NSMD) PCB design, also known as a copper defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 14 for the recommended PCB design parameters.

Table 14. Recommended PCB design parameters

PCB pad size	225 μm diameter
Micro-via diameter	100 μm
Solder mask opening	335 μm diameter
Copper thickness	20 μm to 40 μm
Copper finish	OSP
PCB material	FR4

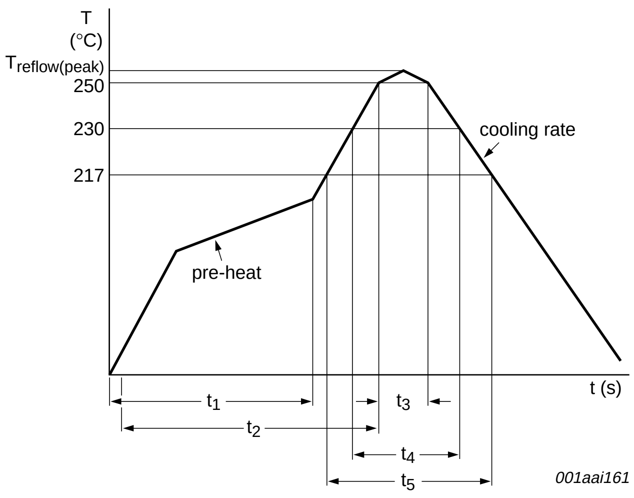
14.2 PCB assembly guidelines for Pb-free soldering

Table 15. Assemble recommendations

Solder screen aperture size	255 μm diameter
Solder screen thickness	100 μm (0.004")
Solder paste: Pb-free	SnAg[1]Cu[2]
Solder/flux ratio	50 : 50
Solder reflow profile	see Figure 9

[1] 3 to 4.

[2] 0.5 to 0.9.



The device is capable of withstanding at least three reflows of this profile.

Fig 9. Pb-free solder reflow profile

Table 16. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature	ΔT = 0 °C to +5 °C	230	-	255	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time from T = 25 °C to $T_{reflow(peak)}$	240	-	300	s
t_3	time 3	time during T ≥ 250 °C	-	-	30	s
t_4	time 4	time during T ≥ 230 °C	10	-	50	s
t_5	time 5	time during T > 217 °C	30	-	150	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

15. Abbreviations

Table 17. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
MMC	MultiMediaCard
NSMD	Non-Solder Mask Design
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PSU	Power Supply Unit

Table 17. Abbreviations *…continued*

Acronym	Description
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
WLCSP	Wafer Level Chip-Scale Package

16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4853CX24_2	20090615	Product data sheet	-	IP4853CX24_1
Modifications:	• Table 11: Added minimum values and values for ‘host-side pins CLK_IN to CLK_FB’. • Table 7: Changed maximum value for regulator quiescent current (not active mode). • Table 8: Moved values from maximum to minimum for power supply rejection ratio. • Removed /LF from all instances of type number IP4853CX24.			
IP4853CX24_1	20080722	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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