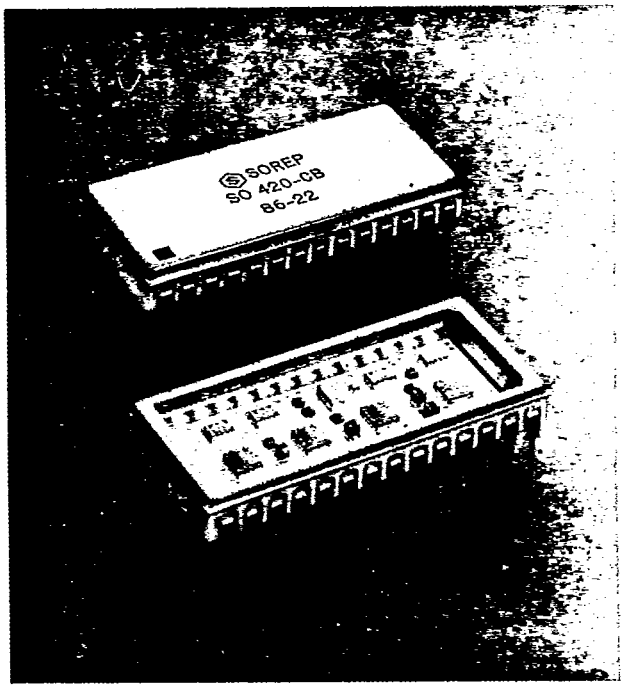
SO 420

QUAD 12-BIT DAC

T-51-09-12

FEATURES

- Four complete CMOS 12-Bit DAC's.
- Monotonicity guaranteed over F.T.R.
- Voltage output.
- Independant control of each DAC.
- Internal voltage reference.
- Microprocessor compatible.



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APPLICATIONS

- Instrumentation (ATE).
- Process controllers.
- Vector stroke displays.
- Actuators, servos.
- Signal processing.
- Waveform generators.

DESCRIPTION

The SO 420 consists of 4 complete 12 bit DACs, with voltage output and reference circuit in a single 28 pin DIL package. The two-stage storage register preceeding each of the 4 DACs allows easy interfacing to all common microprocessor. The input registers are sectionned into two individually adressable segments, 8 bit and 4 bit wide to allow simple interfacing to 8 bit data-buses. The DAC-register, following the input registers, is a parallel 12 bit register for holding the DAC data while the input registers are updated. Only the data held in the DAC register determines the analog value of the converters. The control logic of the SO 420 includes chip enable and latch enable inputs for flexible memory mapping. All control inputs are level-triggered to allow static or dynamic operation. Protection against latch-up is provided by two diodes per DAC. The internal -10^{V} reference outputs sufficient current to supply the 4 DACs. All data and control inputs are TTL - and CMOS - compatible, whereby the CMOS logic level can vary from + 5 to + 15 V.
The SO 420 is available in the commercial range (0; 70°C) *

REV 1

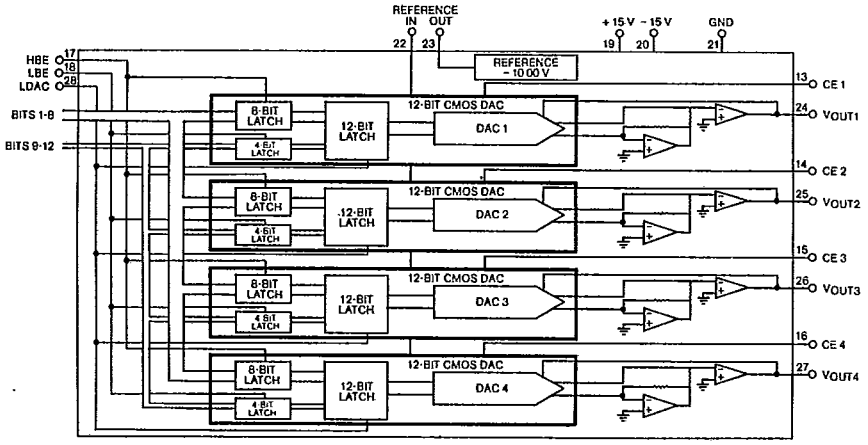
ABSOLUTE MAXIMUM RATINGS Ta = 25°C

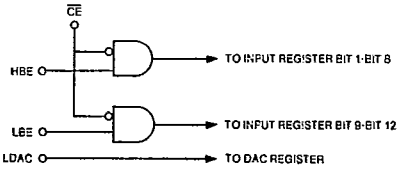
PARAMETER	MIN	MAX	UNIT
V_{DD}	−0.3	+17	V
V_{EE}	+0.3	−17	V
V_{In} Logic Inputs	Gnd	V_{DD}	V
$V_{Ref\ IN}$	−20	+20	V

PARAMETER	
DAC/REF OUTPUT	Infinite short to Gnd
POWER DISSIPATION	1800 mW
TEMP. SOLDERING	10 sec @ 300°C
STORAGE	−65 to +150°C

Exceeding any one of these parameters may cause permanent damage to the unit.
CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed.

FUNCTIONAL DIAGRAM



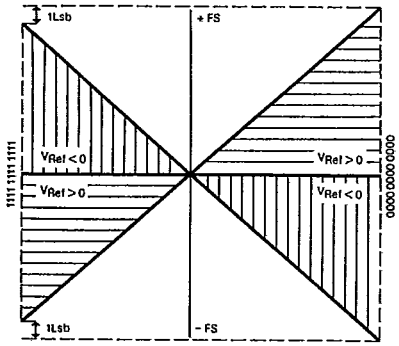


NOTE: The transfer from input register to DAC register can be performed without Enabling Chip.

The SO 420 is supplied with a precision internal −10 V reference, trimmed to within ± 5 millivolts. The reference is available for external use and can supply up to 8 mA of output current. In normal operation, the REF OUT (Pin 23) is connected to REF IN (Pin 22). If a system reference is available, an external reference may be used. It is recommended if an external reference is used, it supplies a minimum of 8 milliamps of current.

TRANSFER FUNCTION

FOUR QUADRANT MULTIPLIER



$$V_{OUT} = V_{Ref}\left(1 - \frac{D}{2048}\right)$$

$$1\ Lsb = \frac{V_{Ref}}{2048}$$

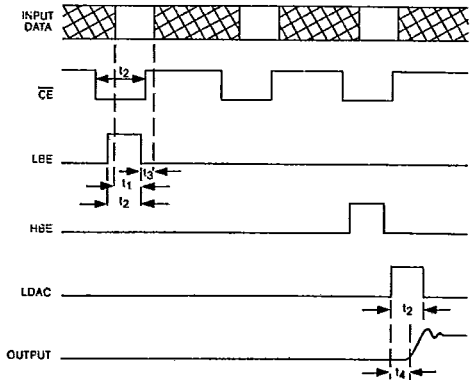
SO 420 TABLE CODE

INPUT DATA	V_{OUT}
1111 1111 1111	− FS+1Lsb
1100 0000 0000	−1/2 FS
1000 0000 0001	−1 Lsb
1000 0000 0000	zéro
0111 1111 1111	+1 Lsb
0100 0000 0000	+1/2 FS
0000 0000 0000	+FS

$V_{Ref} = +10.000\ V = +FS$

FS = Full-Scale

TIMING DIAGRAM



TIME AXIS NOT TO SCALE. ALL STROBES ARE LEVEL TRIGGERED.
t_1: Data Setup Time. Time data must be stable before strobe (byte enable/LDAC) goes to "0", t_1 (min) = 250 nsec.
t_2: Strobe Width, t_2 (min) = 250 nsec. (CE, LBE, HBE, LDAC).
t_3: Hold Time. Time data must be stable after strobe goes to "0", t_3 = 0 nsec.
t_4: Delay from LDAC to Output. t_4 = 200 nsec.

NOTE: Minimum common active time for CE and any byte enable is 250 nsec.

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{Ref} = +10.000$ V, $V_{DD} = +15.0$ V, $V_{EE} = -15.0$ V, $V_{L,H} = 0,5$ V unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	LEVEL	COMMENTS
DIGITAL INPUT Resolution	12 bits Inverted offset binary					
V_{IL}			0.8	VOLTS	IV	Logic inputs are CMOS
V_{IH}	2.4			VOLTS	IV	and TTL compatible
Input current			±4.0	µA	IV	
Data set up time	250			nS	IV	
Data hold time	0.0			nS	IV	
Strobe width	250			nS	IV	
REFERENCE INPUT						
Voltage range			±10	VOLTS	IV	AC or DC
Input impedance	1.2	2.5	3.8	KΩ	IV	
REFERENCE OUTPUT						
Output voltage	−9.995	−10	−10.005	VOLTS	I	T = 25°C; R load = 2.5 K
Total available current			10	mA	IV	T_{min} to T_{max}
Voltage drift		5	10	ppm/°C	I	T_{min} to T_{max}; "Box" definition
STATIC DAC PERFORMANCE						T = 25°C; 10.000 V ext. ref.
Integral linearity		±0.5	±0.75	LSB	I	"End-Points" definition
Bipolar zero error		±1	±2	LSB	I	
Gain error		±2	±4	LSB	I	
Gain error matching		±2		LSB	IV	
DYNAMIC PERFORMANCE						T = 25°C
Small signal settling		2		µS	V	to 0.012%
Full scale settling		5		µS	V	to 0.012%
Slew rate	8	12		V/µS	IV	
DRIFT (T_{min} to T_{max})						10.000 V ext. ref.
Gain		5	10	ppm FS/°C	I	
Bipolar zero		5	10	ppm FS/°C	I	
Integral linearity			0.6	ppm FS/°C	I	
Differential linearity	Monotonicity guaranted over FTR				I	
POWER SUPPLY						
V_{DD}	+13.5		+16.5	VOLTS	IV	
V_{EE}	−13.5		−16.5	VOLTS	IV	
I_{DD}			42	mA	II	$V_{DD} = 15.0$ V ± 5%
I_{EE}			60	mA	II	$V_{EE} = -15.0$ V ± 5%
PSR V_{DD}		0.002		% FS/%	IV	
PSR V_{EE}		0.001		% FS/%	IV	
POWER DISSIPATION		0.70		W	V	
TEMPERATURE RANGE Operating						
SO 420 CB, CZ	−55		+125	°C		
SO 420 CC	0		+70	°C		

TEST LEVEL

I 100% production tested and QA tested per QA test plan QA200.
II 100% production tested at T = 25°C and QA sample tested at 25°C and Tmin and Tmax per QA test plan QA200.
III QA sample tested per QA test plan QA200.
IV Parameter guaranted by design and characterisation.
V Typical value for information.

APPLICATION INFORMATION

The SO 420 has been designed for maximum flexibility in connecting to bus oriented systems. The SO 420 is designed to accept 12-bit parallel data or 8-bit/4-bit data formatted by control pins CE 1 - CE 4, HBE, LBE and LDAC. The input registers are double buffered allowing any primary register to be updated indepentently of the others. Loading on any given primary register is accomplished by bringing the appropriate chip enable low, HBE and LBE high. All four DAC outputs are simultaneously updated by a single LDAC command.

SO 420 TRUTH TABLE

$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{CE}$ 4	HBE	LBE	LDAC	DESCRIPTION
0	1	1	1	1	1	0	Enables 1st rank of DAC1
1	0	1	1	1	1	0	Enables 1st rank of DAC2
1	1	0	1	1	1	0	Enables 1st rank of DAC3
1	1	1	0	1	1	0	Enables 1st rank of DAC4
X	X	X	X	X	X	1	Load DACs 1-4 secondary register from primary register

CONTROL FUNCTIONS

PIN	DEFINITION	FUNCTION
$\overline{CEX}$	Chip Enable X	Enables the primary register of DACX for loading data in conjunction with the HBE and/or LBE function.
HBE	High Byte Enable	Enables the 8 MSBs to be loaded into the primary register of the DACs selected by $\overline{CEX}$.
LBE	Low Byte Enable	Enables the 4 LSBs to be loaded into the primary register of the DACs selected by $\overline{CEX}$.
LDAC	Load DAC	Loads all data in all four DACs, from the primary to secondary registers and updates all DAC outputs.

NOTE : By enabling HBE, LBE and LDAC, all latches become transparent on selected DACs.

STROBE LOGIC

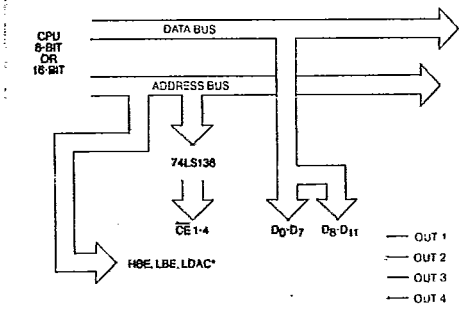
STROBE	FUNCTION
0	Data Latched (Held)
1	Data Changing (Transfer)

POWER SUPPLY CONSIDERATION

Power supplies used for the SO 420 should be selected for low noise operation. In particular, they should be free of high frequency noise. Decoupling capacitors are recommended on all power supply pins located as close to the unit as possible. Suitable decoupling capacitors are 1 µ F tantulum type in parallel with 0,1 µ F disc ceramic type.

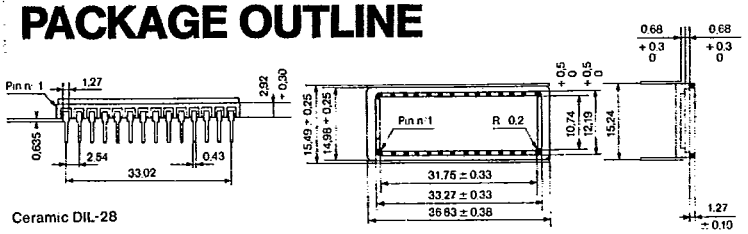
TYPICAL APPLICATION: MICROPROCESSOR INTERFACE

The SO 420 control logic is easily interfaced to most common microprocessors. Due to the 8-bit / 4-bit input architecture, no external latches are required for interface to 8- or 16-bit bus structures.



* For 8-bit Data Bus, HBE and LBE addressed separately as high byte and low byte.
For 16-bit Data Bus, HBE and LBE are tied together and addressed as one word.

PACKAGE OUTLINE



Ceramic DIL-28

PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	BIT 1	11	BIT 11	21	GND
2	BIT 2	12	BIT 12	22	REF In
3	BIT 3	13	CE 1	23	REF Out
4	BIT 4	14	CE 2	24	Vout 1
5	BIT 5	15	CE 3	25	Vout 2
6	BIT 6	16	CE 4	26	Vout 3
7	BIT 7	17	HBE	27	Vout 4
8	BIT 8	18	LBE	28	LDAC
9	BIT 9	19	+ Vs		
10	BIT 10	20	- Vs		

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PROCESS
SO 420 CC	0° C ; 70° C	Commercial
SO 420 CZ	−55° C ; +125° C	Military
SO 420 CB	−55° C ; +125° C	*

- All models packaged in ceramic DIL 28-pins.
- Metallic package available on request.