Standard Products

ACT5028 16-Bit Monolithic Tracking Rad Hard Resolver-To-Digital Converter

www.aeroflex.com/RDC

November 1, 2006

Obsolete for Future Designs, use ACT5028B Data sheet

FEATURES

- Radiation Performance
  - Total Dose: 100Krad (Si)
  - SEL Immune: > 100MeV-cm^2/mg
- +5VDC power only
- Programmable: By using a few non critical external resistors and capacitors
  - Resolution: 10, 12, 14 or 16 bit resolution
  - Bandwidth
  - Tracking rate
- Low power: +5V @ 22 mA Typ.
- 45 to 30,000 Hz carrier frequency range
- Accuracy to 5.3 Arc Minutes
- Differential instrument amplifiers resolver input
- -45° to +125°C Operating Temperature
- Digital interface logic voltage of 3.3V to 5V
- Packaging – Hermetic
  - 52 Pin Ceramic QUAD Flat Package (CQFP), .956" SQ x .10" Ht max
  - 52 Lead Ceramic Leadless Chip Carrier Package (CLCC), 0.765" SQ x 0.09" Ht max (EM's only)
- Evaluation board available for test and evaluation. See Aeroflex Application Note AN5028-1.

NOTE: Aeroflex Plainview does not currently have a DSCC certified Radiation Hardened Assurance Program

APPLICATIONS

This single chip Resolver-to-Digital Converter (RDC) is used in shaft angle control systems, and is suitable for space or other radiation environments that require >100KRad total dose tolerance. The part is latchup free in heavy ion environments (e.g., geosynchronous orbits) and is estimated to experience SEU induced errors of less than 15 minutes of arc at a rate of 1 per device per 2 years when operating dynamically.

THEORY OF OPERATION

The ACT5028 converter is a single CMOS Type II tracking resolver to digital converter monolithic chip. It is implemented using precision analog circuitry and digital logic. For flexibility, the converter bandwidth, dynamics and velocity scaling are externally set with passive components. Refer to Figure 1, ACT5028 Block Diagram.

The converter is powered from +5VDC. Analog signals are referenced to signal ground, which is nominally VCC/2. The converter consists of three main sections; the Analog Control Transformer (CT), the Analog Error Processor (EP) and the Digital Logic Interface.

The CT has two analog resolver inputs (Sin and Cos) that are buffered by high impedance input instrumentation type amplifiers and the 16 bit digital word which represents the output digital angle. The CT performs the ratiometric trigonometric computation of:

$$\mathrm{SIN}(A)\sin(wt)\,\mathrm{COS}(B) - \mathrm{COS}(A)\sin(wt)\,\mathrm{SIN}(B) = \mathrm{SIN}(A\text{-}B)\sin(wt)$$

Utilizing amplifiers, switches, logic and resistors in precision ratios. “A” represents the resolver angle, “B“ represents the digital angle and sin(wt) represents the resolver reference carrier frequency.

The Error Processor is configured as a critically damped Type II loop. The AC error, SIN (A-B) sin (wt) is full wave demodulated using the reference squared off as its drive. This DC error is integrated in an analog integrator yielding a velocity voltage which in turn drives a Voltage Controlled Oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II loop. A lead is inserted to stabilize the loop and a lag is inserted at a higher frequency to attenuate the carrier frequency ripple. The error processor drives the 16 bit digital output until it nulls out. Then angle “A” = “B”. The digital output equals angle input to the accuracy of the precision control transformer. The various error processor settings are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

The digital logic interface has a separate power line, VLI/O that sets the interface logic 1 level. It can be set anywhere from +3V to the +5V power supply.

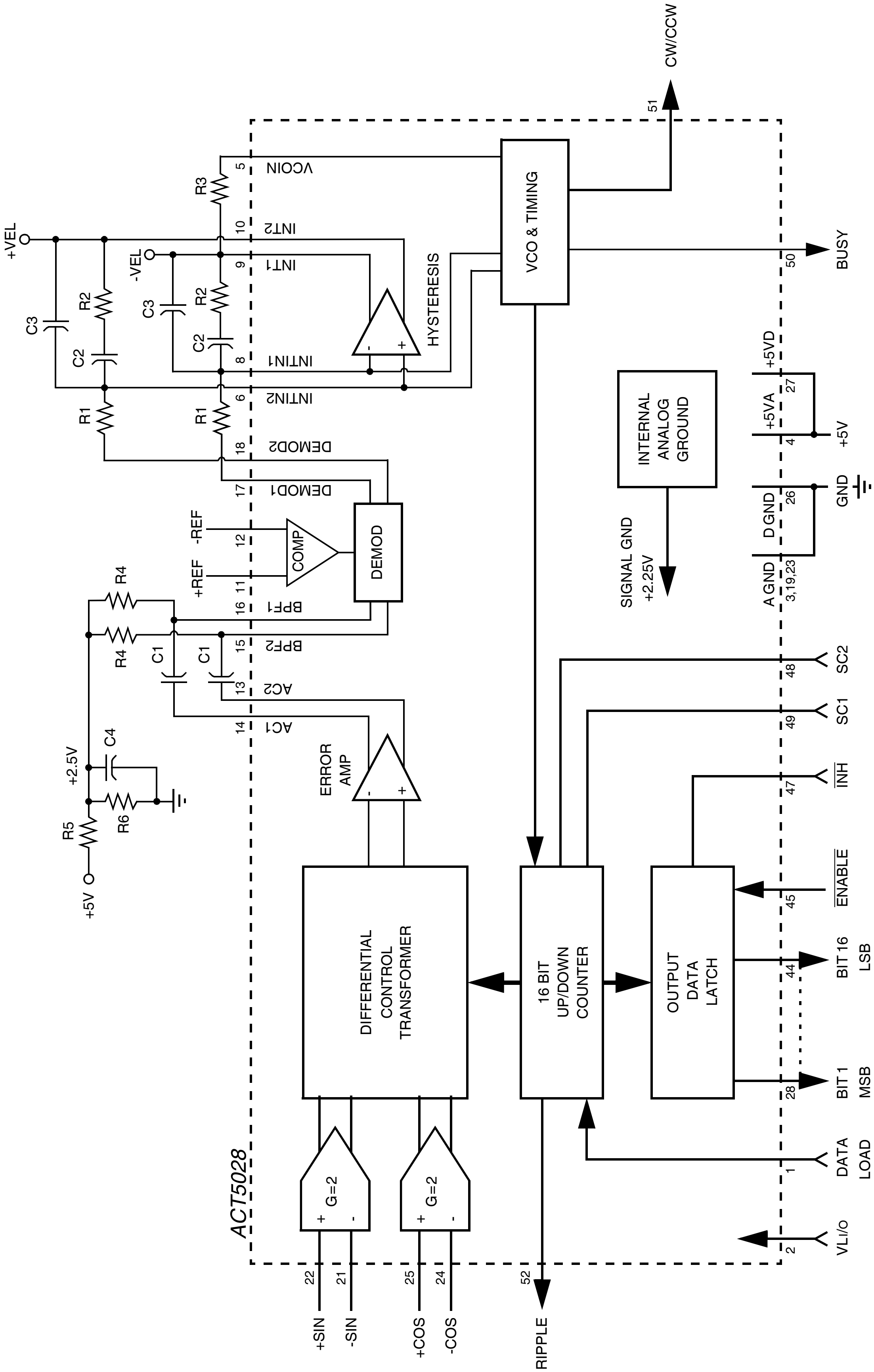


FIGURE 1 – ACT5028 BLOCK DIAGRAM

PIN DESCRIPTIONS

SIGNAL	DIRECTION	PIN	SIGNAL DESCRIPTION
+SIN -SIN	INPUT	22 21	Analog Sine input from Synchro or Resolver. 1.3Vrms nominal
+COS -COS	INPUT	25 24	Analog Cosine input from Synchro or Resolver. 1.3Vrms nominal
+REF -REF	INPUT	11 12	Analog Reference input
BIT 1 (MSB) BIT 2 BIT 3 BIT 4 BIT 5 BIT 6 BIT 7 BIT 8 BIT 9 BIT 10 BIT 11 BIT 12 BIT 13 BIT 14 BIT 15 BIT 16 (LSB)	BIDIR	28 29 30 31 32 34 35 36 38 39 40 41 42 43 44	Digital angle data. Parallel format. Natural binary positive logic. Bit 1, most significant bit = 180°, Bit 2 = 90°, Bit 3 = 45° and so on. In the 10 bit mode, Bit 10 is the LSB. Bits 11-16 are 0s. In the 12 bit mode, Bit 12 is the LSB. Bits 13-16 are 0s. In the 14 bit mode, Bit 14 is the LSB. Bits 15-16 are 0s. In the 16 bit mode, Bit 16 is the LSB.
SC1 SC2	INPUT	49 48	Digital input. Sets the resolution. SC1 SC2 Resolution 0 0 10 bit 0 1 12 bit 1 0 14 bit 1 1 16 bit
$\overline{\text{ENABLE}}$*	INPUT	45	Logic 0 enables digital angle output. Otherwise it is high impedance.
$\overline{\text{INH}}$*	INPUT	47	Logic 0 freezes the digital angle output so that it can be safely read.
DATA LOAD	INPUT	1	Logic 1 enables the digital angle lines to be inputs to preset the angle. Logic 0 is for normal digital angle output.
BUSY	OUTPUT	50	A logic 1 pulse when the digital angle changes by 1 LSB.
CW/CCW	OUTPUT	51	For turns counting. Logic 1 = counting up (CW), logic 0 = counting down (CCW).
RIPPLE	OUTPUT	52	Ripple clock for turns counting. A logic 1 pulse = a 0° transition in either direction.
AC1 AC2	OUTPUT	14 13	Differential AC error output
BPF1 BPF2	INPUT	16 15	Differential AC error input to demodulator
DEMOD1 DEMOD2	OUTPUT	17 18	Differential DC error output
INTIN1 INTIN2	INPUT	8 6	Differential DC input to differential velocity integrator
INT1 INT 2	OUTPUT	9 10	Differential velocity output
VCOIN	INPUT	5	Input to Voltage Controlled Oscillator
VCC VDD	POWER	4 27	Analog Power In Digital Power In
A GND D GND	POWER	3, 19, 23 26	Analog Power ground Digital Power ground
VL I/O	POWER	2	Digital input/output DC power supply. Sets logic 1 level. +3V to +5V

* Indicates Active Low Signal

ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUE
Operating Temperature	-45°C to +125°C
Storage Temperature	-65°C to +150°C
Positive Power Supply Voltage (V_{CC} = V_{DD})	-0.5 V to +7.0 V
Analog Output Current (Output Shorted to GND)	32 mA Max
Digital Output Current (Output Shorted to GND)	18.6 mA Max
Analog Input Voltage Range	-0.3 V to + (V_{CC} +.3 V)
Digital Input Voltage Range	-0.3 V to + (V_{DD} +.3 V)
Thermal Resistance $Ø_{JC}$ Specification	1.25°C/W
Maximum Junction Temperature	135°C

* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only; functional operation beyond these operating conditions is not recommended and extended exposure beyond these operating conditions may effect device reliability.

OPERATING CONDITIONS

(T_A = -45°C to +125°C)

POWER SUPPLY	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD} = V_{CC}	Operating Voltage	4.5	5	5.5	VDC
I_{DD} + I_{CC}	Operating Current	-	22	35	mA
$VL_{I/O}$	Interface Voltage	3	3.3, 5	5.5	VDC

ELECTRICAL CHARACTERISTICS [2,5,6]

(T_A = -45°C to +125°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy[4]	Add 1 LSB for total Error	-	±2	± 5	Minutes
Repeatability		-	-	1	LSB
Resolution per LSB	10 Bit Mode	0.35	-	-	Degrees
		21.1	-	-	Minutes
	12 Bit Mode	0.09	-	-	Degrees
		5.27	-	-	Minutes
	14 Bit Mode	0.022	-	-	Degrees
		1.32	-	-	Minutes
	16 Bit Mode	0.0055	-	-	Degrees
		0.33	-	-	Minutes
Max Tracking Rate[7]	SC1 SC2 Bits Used				
10 Bit Mode	0 0 B1 - B10	1024	-	-	RPS
12 Bit Mode	0 1 B1 - B12	256	-	-	RPS
14 Bit Mode	1 0 B1 - B14	64	-	-	RPS
16 Bit Mode	1 1 B1 - B16	16	-	-	RPS
VCO Frequency		1.05	-	-	MHz

ELECTRICAL SPECIFICATIONS[2,5,6]

(T_A = -45°C to +125°C)

ANALOG SIGNAL INPUTS	SYM	PARAMETER	MIN	TYP	MAX	UNITS
SIN, COS, REF	V_{SIN}, V_{COS}, V_{REF}	Voltage measurement made between ± inputs	1.0	1.3	1.5	V_{RMS}
	F_{REF}	Frequency[1]	45	-	30K	Hz
		Impedance[3]	100	-	-	MΩ
		Capacitance[3]	-	5	15	pF
		DC Bias on -Sin, -Cos	-	$V_{CC}/2$	-	V_{DC}
		Bias Current[3]	-	0.1	50	nA
DIGITAL INPUTS						
$\overline{ENABLE}$, $\overline{SC2}$, SC1, $\overline{INH}$ See Note 3	V_{IL}	Logic Low	-	-	0.8	V_{DC}
	V_{IH}	Logic High	2	-	-	V_{DC}
	I_{IN}	Leakage Current	-	0.2	100	nA
		Impedance	100	-	-	MΩ
		Capacitance	-	5	15	pF
DIGITAL OUTPUTS						
BUSY, RIPPLE CW/CCW	V_{OL}	Logic Low @ 1.6mA	-	-	0.3	V_{DC}
	V_{OH}	Logic High @ -1.6mA	$V_{LI/O}$ - .6	-	-	V_{DC}
DIGITAL I/O						
B1 - B16	V_{IL}	Logic Low[3]	-	-	0.8	V_{DC}
	V_{IH}	Logic High[3]	2	-	-	V_{DC}
	V_{OL}	Logic Low @ 1.6mA	-	-	0.3	V_{DC}
	V_{OH}	Logic High @ -1.6mA	$V_{LI/O}$ - .6	-	-	V_{DC}
	I_{IN}	Leakage Current[3]	-	0.2	100	nA
	I_Z	High-Z Leakage Current[3]	-	0.2	100	nA

Notes

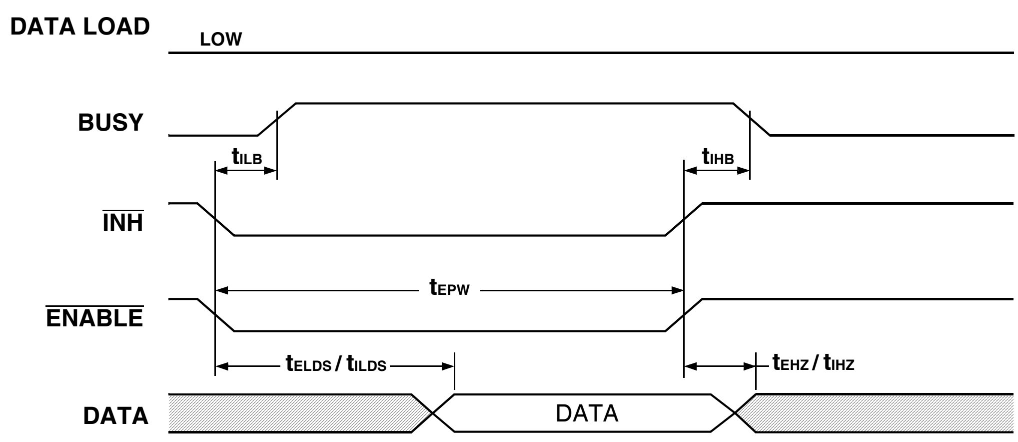
1. @ 10 Bits, F_{REF} > 4 x BW_{CL}
   @ 12 Bits, F_{REF} > 8 x BW_{CL}
   @ 14 Bits, F_{REF} > 12 x BW_{CL}
   @ 16 Bits, F_{REF} > 16 x BW_{CL}
2. All typical values are measured at +25°C.
3. Characteristics are guaranteed by design, not production tested.
4. Accuracy apply over the full operating Power Supply voltage range, Full operating Temperature range, Reference Frequency range, 10% Signal Amplitude variation and 10% Reference Harmonic distortion.
5. For ESD protection the ACT5028 features limiting resistors in series with diodes. Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation.
6. All testing at nominal voltage.
7. All used inputs shall be tied to Ground. Bit 1 is always the MSB.

TIMING SPECIFICATIONS [6]

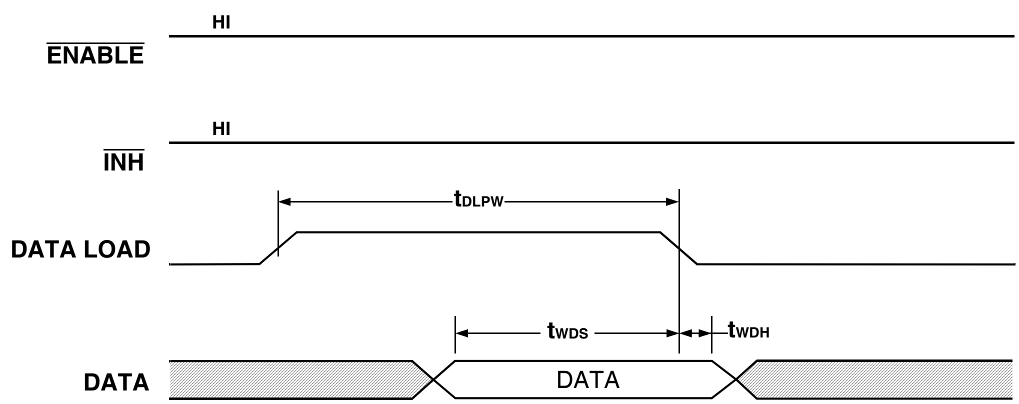
T_A = 25°C with 50pf Load

DIGITAL OUTPUT – Rise Time / Fall Time	SYM	COMMENTS	MIN	TYP	MAX	UNITS
Busy	t_{LH}	Rise Time	-	20	40	ns
	t_{HL}	Fall Time	-	20	40	ns
CW/CCW, Ripple, B1- B16	t_{LH}	Rise Time	-	45	85	ns
	t_{HL}	Fall Time	-	45	85	ns
Busy Pulse Width	t_{BPW}	JY04A silicon	10	20	40	ns
Busy to Data Stable	t_{BDS}	Enable = Low	-	-	60	ns
Ripple Pulse Width	t_{RPW}	$= 1 / (2^N \times RPS)$	1	-	-	µs
Ripple to Busy	t_{RB}	Both edges of Ripple	-	10	15	ns
$\overline{\text{INH}}$ Low to Busy	t_{ILB}		-	-	20	ns
$\overline{\text{INH}}$ High to Busy	t_{IHB}		-	-	60	ns
READ DATA – $\overline{\text{Enable}}$ & $\overline{\text{INH}}$ would normally be tied together, Data Load = Logic Low						
$\overline{\text{Enable}}$ Pulse Width	t_{EPW}		200	-	-	ns
$\overline{\text{Enable}}$ Low to Data Stable	t_{ELDS}		-	-	70	ns
$\overline{\text{Enable}}$ High to Data Hi-Z	t_{EHZ}		-	-	20	ns
$\overline{\text{INH}}$ Low to Data Stable	t_{ILDS}		-	-	70	ns
$\overline{\text{INH}}$ High to Data Change	t_{IHZ}		-	-	20	ns
WRITING DATA – $\overline{\text{Enable}}$ & $\overline{\text{INH}}$ = Logic Hi						
Data Load Pulse Width	t_{DLPW}	Transparent Trailing Edge Latch	200	-	-	ns
Data Setup to Data Load	t_{WDS}		60	-	-	ns
Data Hold	t_{WDH}		10	-	-	ns

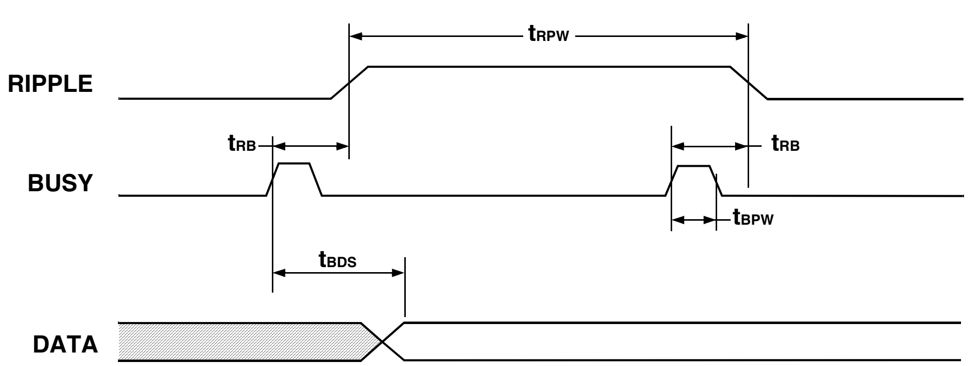
READ CYCLE



WRITE CYCLE



BUSY TIMING



ACT5028 TIMING DIAGRAMS

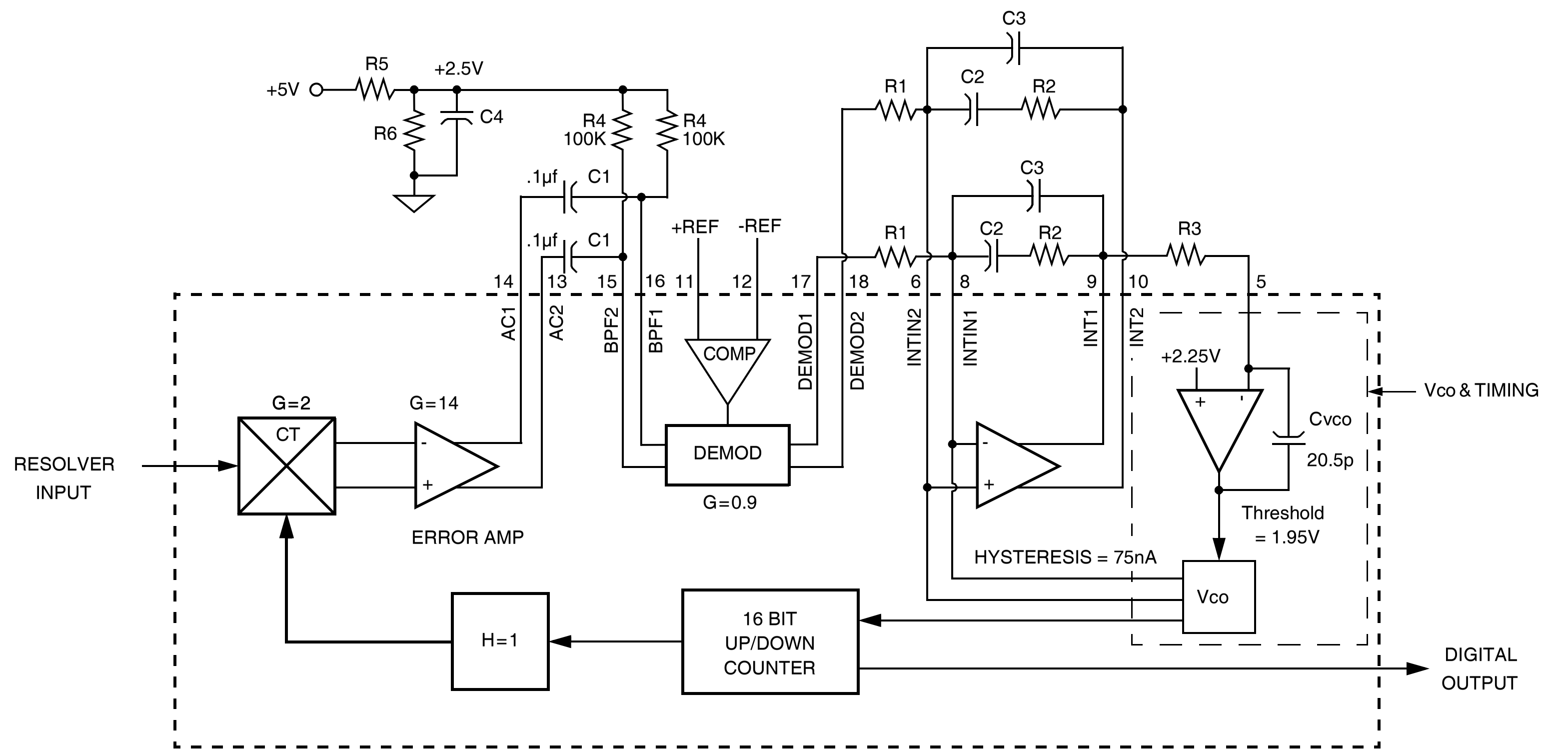


FIGURE 2 – ACT5028 FUNCTIONAL BLOCK DIAGRAM

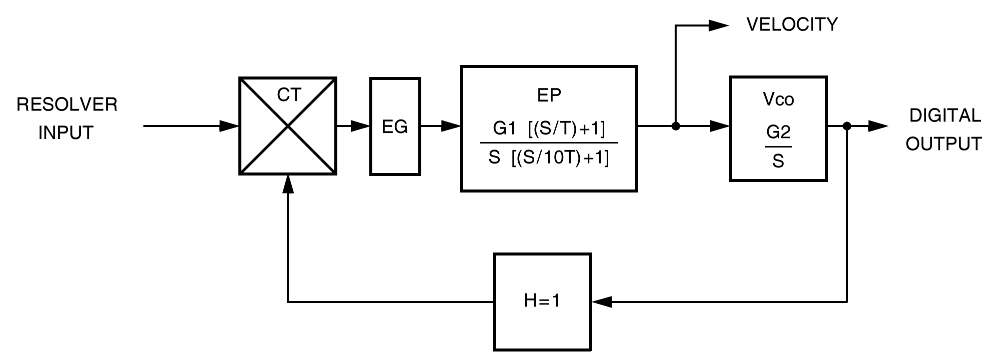


FIGURE 3 – ACT5028 TRANSFER FUNCTION DIAGRAM

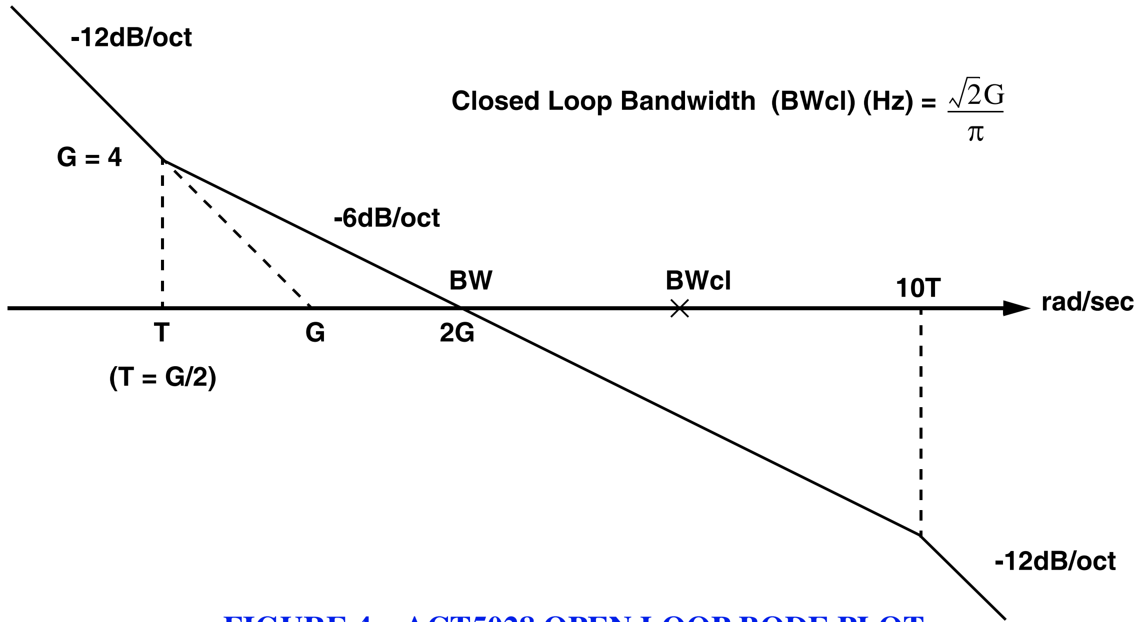


FIGURE 4 – ACT5028 OPEN LOOP BODE PLOT

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram, Transfer Function Diagram and Bode plots, as shown in Figures 2, 3 and 4.

PROCEDURE FOR SELECTING RDC BANDWIDTH COMPONENTS *

Input: Carrier Frequency (Fc) in Hz [47 to 30,000 Hz]
Input: Nominal Resolver Input Level in Vrms [1Vrms min. to 1.5Vrms max.]
Input: Resolution in bits; 10, 12, 14 or 16 bits
Input: Closed Loop Bandwidth (BWcl) in Hz [10 bit; BWcl = Fc/4 max.]
[12 bit; BWcl = Fc/8 max.]
[14 bit; BWcl = Fc/12 max.]
[16 bit; BWcl = Fc/16 max.]

Input: Maximum Tracking Rate in RPS [16 bit; 16 RPS max.]
(RPS = rotations per second) [14 bit, 64 RPS max.]
[12 bit; 256 RPS max.]
[10 bit, 1024 RPS max.]

Input: Hysteresis in LSBs. Recommended is 1 LSB for 16 & 14 bits and 0.7 LSBs for 12 & 10 bits.

EG = Nominal Resolver Input Level • .0027 [16 bit] or
EG = Nominal Resolver Input Level • .011 [14 bit] or
EG = Nominal Resolver Input Level • .043 [12 bit] or
EG = Nominal Resolver Input Level • .17 [10 bit]

G = 2.22 • BWcl

$G^2 = EG \bullet 0.45 \bullet G1 \bullet G2$

Hysteresis recommended values
HYS = 0.7 [10 & 12 bit] or
HYS = 1 [14 & 16 bit] or

$R1_{(ohms)} = 6 \bullet 10^6 \bullet EG \bullet HYS$

G2 = Maximum Tracking Rate • 2^{15} [16 bit] or
G2 = Maximum Tracking Rate • 2^{13} [14 bit] or
G2 = Maximum Tracking Rate • 2^{11} [12 bit] or
G2 = Maximum Tracking Rate • 2^{9} [10 bit]

$R3_{(ohms)} = (25 \bullet 10^9)/G2$

$G1 = G^2/(EG \bullet .45 \bullet G2)$

$C2_{(farads)} = 1/(G1 \bullet R1)$

$C3_{(farads)} = C2/10$

$R2_{(ohms)} = 2/(G \bullet C2)$

ACT5028 EXAMPLE CALCULATIONS

Carrier Frequency = 800 Hz
Nominal Resolver Input Level = 1.3Vrms
Resolution = 14 bits
Closed Loop Bandwidth (BWcl) = 20 Hz
Maximum Tracking Rate in RPS = 1
Hysteresis = 1 LSB

EG = Nominal Resolver Input Level • .011 [14 bit] = 1.3 • .011 = .014
G = 2.22 • BWcl = 2.22 • 20 = 44.4
HYS = 1 [14 bit]

$R1_{(ohms)} = 6 \bullet 10^6 \bullet EG \bullet HYS = 6 \bullet 10^6 \bullet .014 \bullet 1 = 84K$. Use closest standard resistor = 84.5K 1%

$G2$ = Maximum Tracking Rate $\bullet\ 2^{13} = 8192$ [2^{13} for 14 bits]

$R3_{(ohms)} = (25 \bullet 10^9)/G2 = (25 \bullet 10^9)/8192 = 3{,}050K$. Use closest standard resistor = 3.01M 1% or 3M 5%

$G^2 = EG \bullet 0.45 \bullet G1 \bullet G2$

$G1 = G^2/(EG \bullet .45 \bullet G2) = 44.4^2/(.014 \bullet .45 \bullet 8192) = 38.2$

$C2_{(farads)} = 1/(G1 \bullet R1) = 1/(38.2 \bullet 84.5K) = .31\mu F$. Use closest standard capacitor = .33µF 10%

$C3 = C2/10_{(farads)} = C2/10 = .33\mu/10 = .033\mu F$

$R2_{(ohms)} = 2/(G \bullet C2) = 2/(44.4 \bullet .33\mu) = 136.5K$. Use closest standard resistor = 137K 1%

SIGNAL AND REFERENCE INPUT CONDITIONING

Inputs to the converter should be 1.3 Vrms nominal, resolver format referenced to $V_{CC}/2$ nominal Figure 5 shows various input configurations.

REFERENCE CONDITIONING

Most resolvers have a LEADING input to output phase shift. A simple C-R leading phase shift network (Figure 5 – Reference Conditioning) from the resolver reference to the RDC's reference input will provide the compensating phase shift required to bring the signals in phase. If the resolver has a LAGGING input to output phase shift an R-C lagging phase shift network (low pass network) would be required.

Note the C-R phase lead circuit on the input to the Demodulator (BPF1 and BPF2) in Figure 2 should be considered when calculating the total system phase compensation.

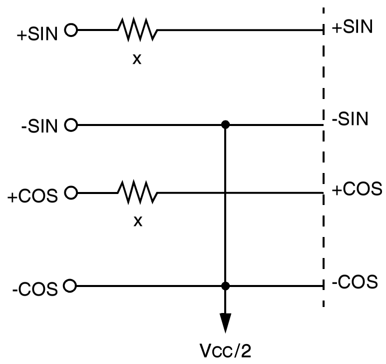
The formula for calculating the phase shift network is as follows:

$$\text{Phase angle} = \text{ArcTan}\ \frac{\dfrac{1}{6.28 \times (R7 + R8) \times C}}{F_{REF}}$$

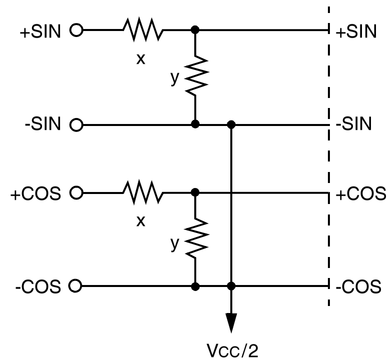
Select a convenient capacitor value and perform the following calculation to determine the proper resistor value.

$$R = \frac{1}{(\text{Tan (Phase Angle)}) \times F_{REF} \times 6.28 \times C}$$

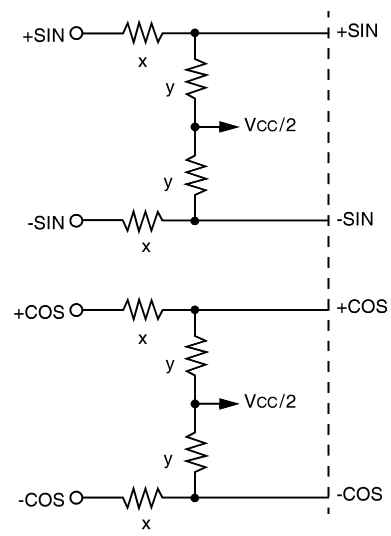
**** Software Program SW5028-2 available at Aeroflex WEB site.***



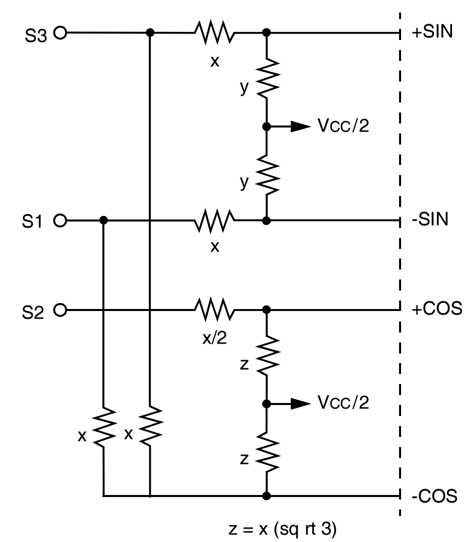
DIRECT RESOLVER



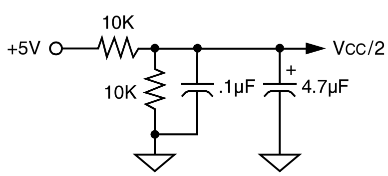
SINGLE ENDED RESOLVER CONDITIONING



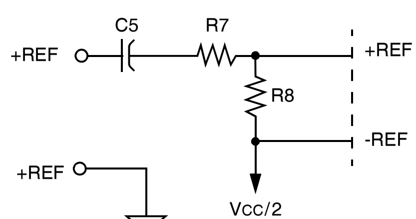
DIFFERENTIAL RESOLVER CONDITIONING



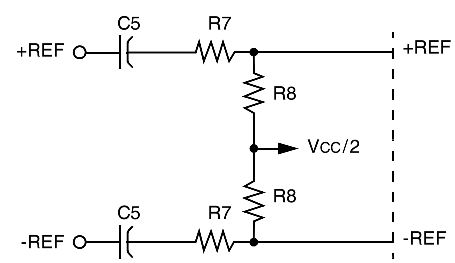
SYNCHRO CONDITIONING



2.5VDC



SINGLE ENDED REFERENCE CONDITIONING



DIFFERENTIAL REFERENCE CONDITIONING (FLOATING REFERENCE)

FIGURE 5 – ACT5028 RESOLVER, SYNCHRO AND REFERENCE INPUT CONFIGURATIONS

TABLE I – ACT5028 PIN OUT DESCRIPTIONS (CQFP OR CLCC – PACKAGE)

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	DATA LOAD *	19	A GND	37	BIT 9
2	VL I/O	20	N/C	38	BIT 10
3	A GND	21	-SIN	39	BIT 11
4	A +5V	22	+SIN	40	BIT 12
5	VCOIN	23	A GND	41	BIT 13
6	INTIN2	24	-COS	42	BIT 14
7	N/C	25	+COS	43	BIT 15
8	INTIN1	26	D GND	44	BIT 16 (LSB)
9	INT1	27	D +5V	45	$\overline{\text{ENABLE}}$
10	INT2	28	BIT 1 (MSB)	46	N/C
11	+REF	29	BIT 2	47	$\overline{\text{INH}}$
12	-REF	30	BIT 3	48	SC2
13	AC2	31	BIT 4	49	SC1
14	AC1	32	BIT 5	50	BUSY
15	BPF2	33	N/C	51	CW/CCW
16	BPF1	34	BIT 6	52	RIPPLE
17	DEMOD1	35	BIT 7		
18	DEMOD2	36	BIT 8		

* DATA LOAD is active High for Rev. A Silicon and active Low for Rev. B Silicon.

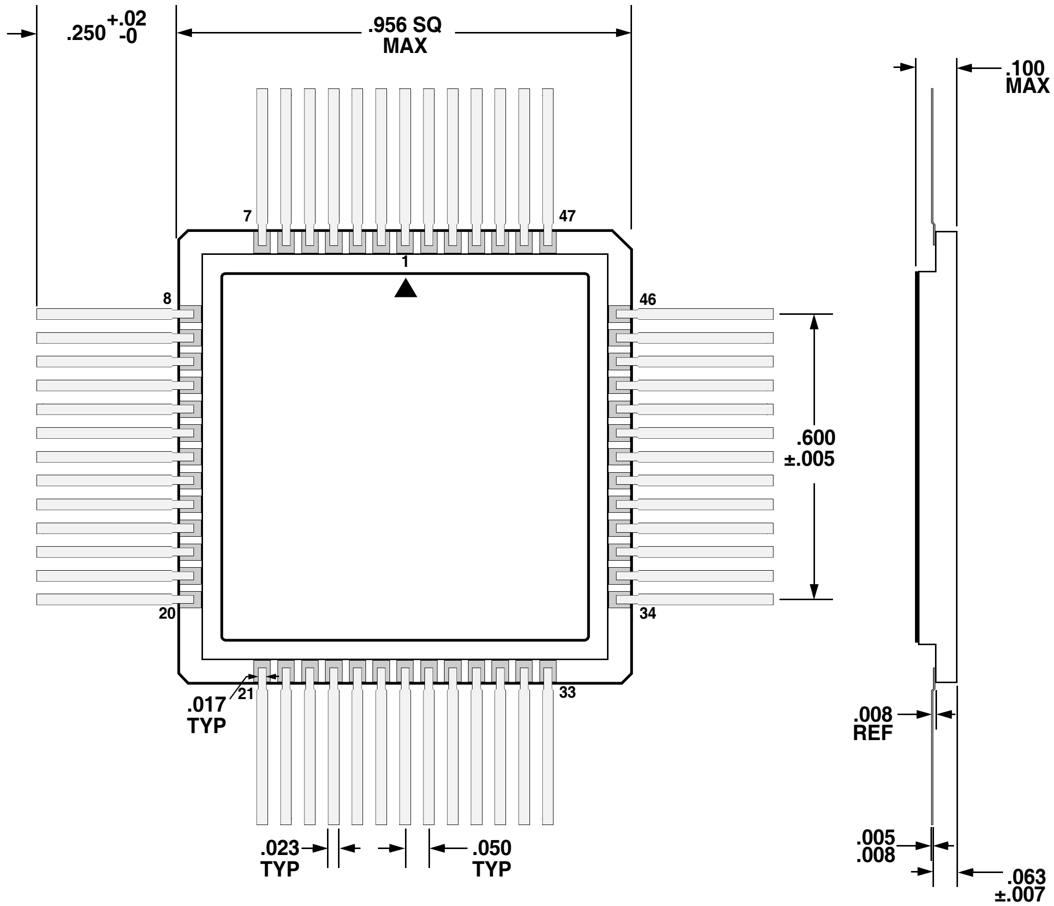


FIGURE 6 – 52 PIN CERAMIC QUAD FLAT PACKAGE (CQFP) OUTLINE

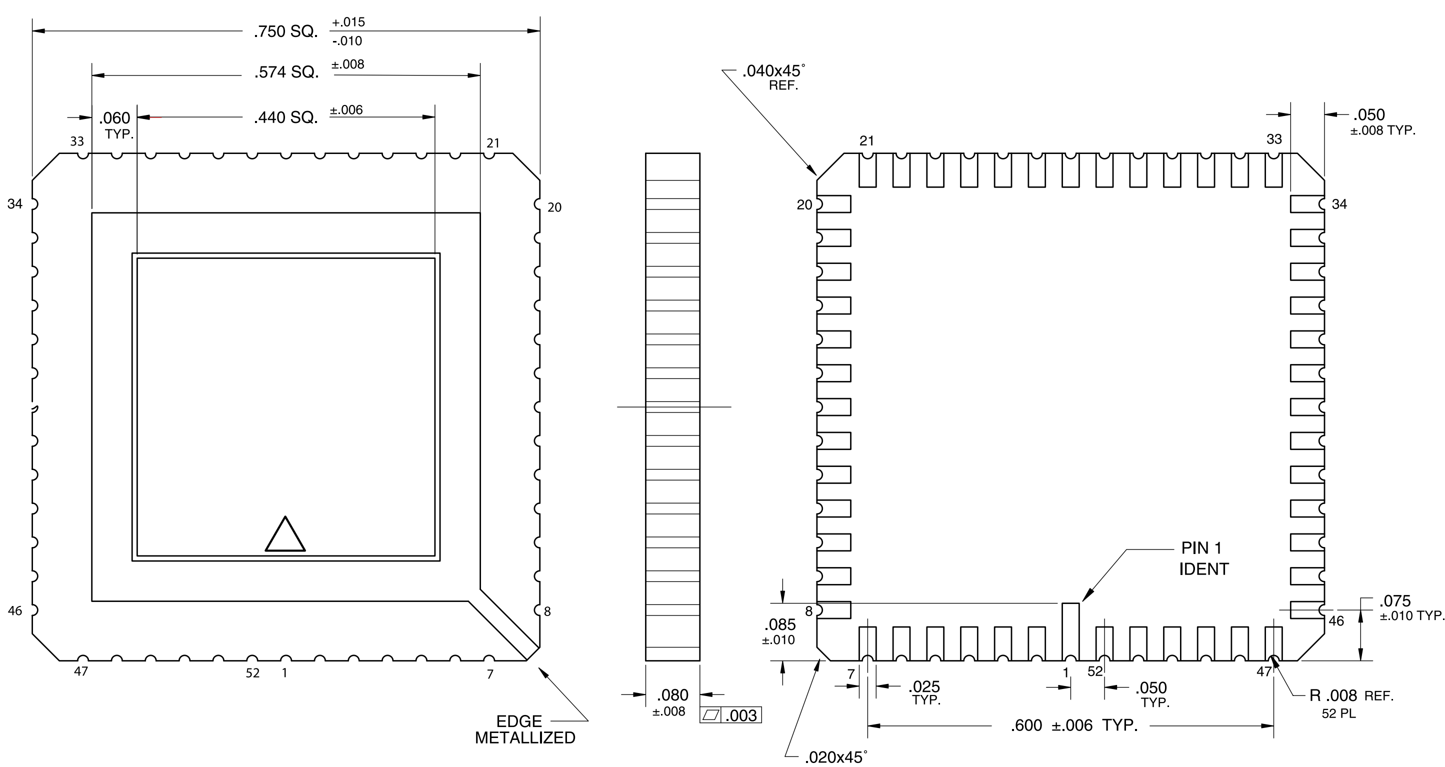


FIGURE 7 – 52 LEAD CERAMIC CHIP CARRIER (CLCC) PACKAGE OUTLINE

ERRATA INFORMATION ACT5028-2-X

This Errata information represents the known bugs, anomalies, and work-arounds for the ACT5028 Resolver to Digital Converter

DESCRIPTION OF ANOMALIES:

Anomaly #1: Instability at 360^{o} and 180^{o} Input Angles

Anomaly #2: Correcting for the Integral Nonlinearity Error found in Revision A Silicon

EFFECTED PARTS:

ACT5028-2-X (revision A silicon)

ANOMALY #1

PROBLEM DESCRIPTION:

This problem only occurs in the 16 Bit mode when rotating in the clockwise (CW) direction and has been observed on 45% of the parts tested at 25°C. The problem is temperature sensitive, parts that passed at 25°C would fail at -10°C and parts that once failed at 25°C would pass at 55°C.

At 360^{o} the problem occurs when the counter passes from FFFF to 0000 then reverse rotation (CCW) back to FFFF. Because of the nature of this problem it is possible that the problem can occur at 180° but has never been observed. The problem could occur when the counter passes from 7FFF to 1000 then reverse rotation (CCW) back to 7FFF.

Two different failure modes have been observed:

1) The output latch locks to a value with the MSB inverted giving the indication that the RDC chip is 180^{o} out of phase, the RDC chip exhibits zero error. This condition remains indefinitely until the resolver rotates in either direction by one count. At which time the RDC chip responds to the 180^{o} error which takes less than 150ms to correct.
2) The RDC chip sees an immediate error of 180^{o} and begins to correct for this error which takes less than 150ms.

In some cases it has been observed that the MSB is OK but the next bit gets inverted which provides a 90^{o} error. In this case the time required for the RDC chip to correct its self is less than 75 ms.

RECOMMENDED ACTIONS:

1) Use the 14, 12 or 10 Bit mode where this problem doesn't exist.
2) Insure a hysteresis of at least one bit to prevent this anomaly when rotating very slowly.
3) Avoid reversing direction at 360^{o} and 180^{o} when rotating in the CW direction.
4) If the resolver stops within two counts of 360^{o} or 180^{o} wait 150ms after motion resumes before reading the RDC output.

ANOMALY #2

PROBLEM DESCRIPTION AND RECOMMENDED ACTION:

This Errata information is to address the constant Integral Nonlinearity (INL) that exists at each angle of the ACT5028 Resolver to Digital Converter (RDC). This error is repeatable from chip to chip and provides a look up Table of offsets that must be added to the output of the Resolver to Digital Converter to get the correct angle.

Figure 7 shows the error in Minutes that exists at 2^o increments for the full 360^o. Note that the INL error from 0^o to 180^o is basically the same as the error between 180^o and 360^o. Table II has the angle and correction factor (in Minutes) that must be added to zero out the INL error.

A simple calculation can be performed to derive a correction factor for angles that fall between the angles listed in Table II herein.

AL = Larger Angle

AS = Smaller Angle

CL = Correction Factor associated with larger Angle

CS = Correction Factor associated with smaller Angle

NA = New Angle

NCF = New Correction Factor

Formula:

NCF = CS + (((NA - AS) / (AL - AS)) * (CL - CS))

Example:

Require the correction factor @ 15^o

NCF = 23.4009 + (((15 – 14) / (16 – 14)) * (24.0326 - 23.4009))

NCF = 23.4009 + (((1) / (2)) * .6137)

NCF = 23.4009 + (.5 * .6137)

NCF = 23.4009 + .31585

NCF = 23.71675 minutes

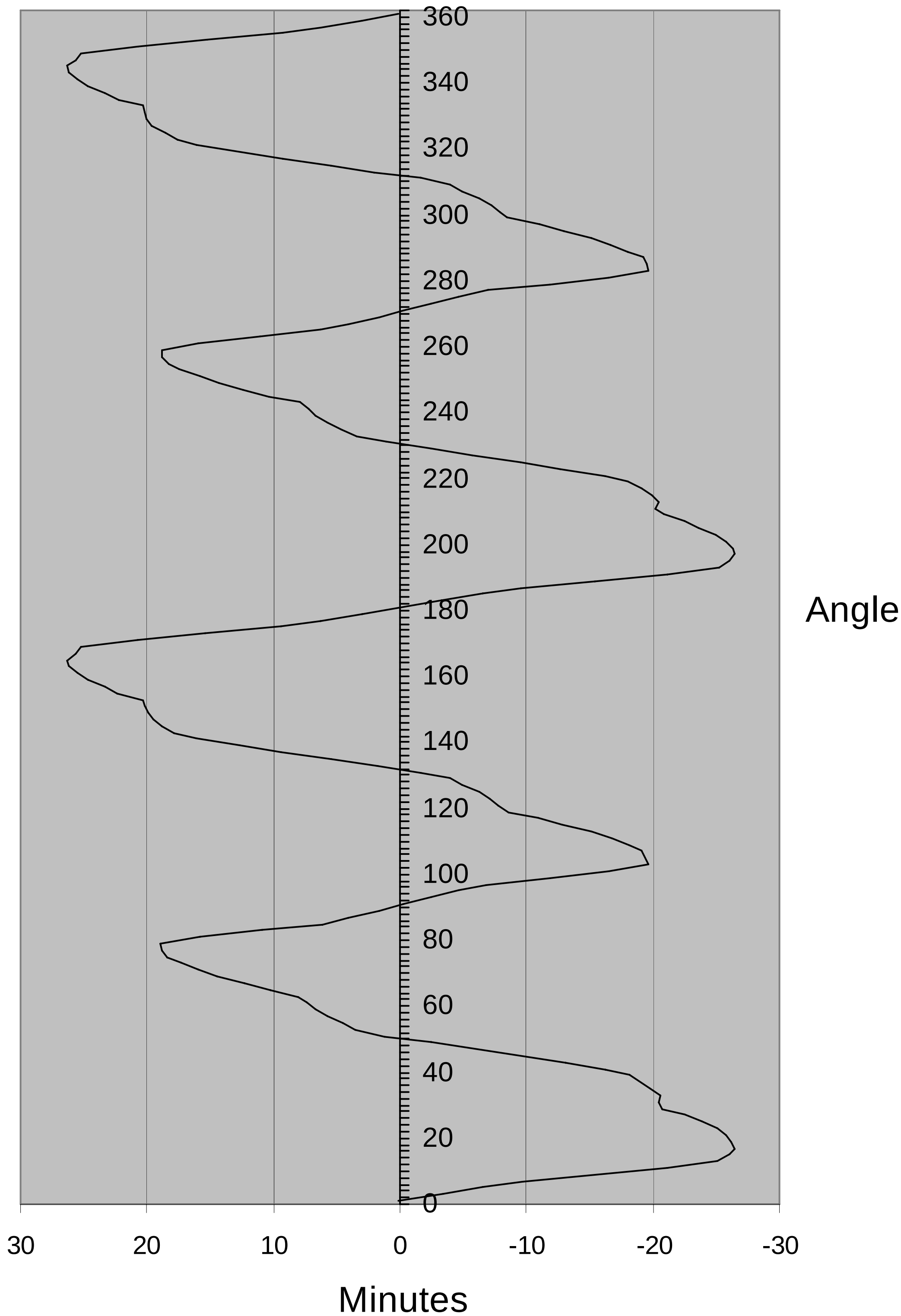


Figure 8 – Anomaly #2 Angle Error Chart

ANOMALY #3

PRECAUTIONARY NOTE:

The ACT5028 RDC converter can provide incorrect data output if a unit step of 180° (starting at any angle) is introduced to the Sin / Cos input.

This anomaly is difficult to reproduce since a Resolver will never provide a unit step function to the RDC chip.

The only time this would be a concern is during power up, if the Resolver is set to 180°. The RDC will initialize its internal counter to 0000h which simulates the unit step function mentioned above. In practice this error condition during power up is difficult to produce because of the dynamics associated with all the variables when power is first applied.

If the system designer does nothing to accommodate this potential problem the system could see an error at power on, however, this error will be self corrected once the Resolver rotates causing the RDC to correct the Resolver rotates causing the RDC to correct this error.

Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor
0	-0.07141	90	0.322266	180	0.098877	270	0.302124
2	3.418579	92	2.479248	182	3.208008	272	2.426147
4	6.520386	94	4.689331	184	6.520386	274	4.605103
6	9.633179	96	6.774902	186	9.488525	276	6.94519
8	15.41931	98	11.90369	188	15.401	278	11.87805
10	21.13037	100	16.474	190	21.07727	280	16.56555
12	25.11108	102	19.57947	192	25.22461	282	19.69482
14	26.07056	104	19.39453	194	26.03394	284	19.54285
16	26.46606	106	19.08508	196	26.39832	286	19.16931
18	26.20239	108	18.11096	198	26.26465	288	17.97913
20	25.77759	110	16.74683	200	25.83252	290	16.62048
22	25.07996	112	15.10803	202	24.99023	292	15.13
24	23.82019	114	12.87048	204	23.65173	294	12.98035
26	22.46521	116	10.87463	206	22.48718	296	10.98267
28	20.78979	118	8.602295	208	20.85937	298	8.441162
30	20.43091	120	7.72522	210	20.224	300	7.906494
32	20.52795	122	7.144775	212	20.42725	302	7.218018
34	19.7699	124	6.210937	214	19.85229	304	6.216431
36	18.95874	126	4.932861	216	19.03564	306	4.954834
38	18.13843	128	3.90564	218	18.03406	308	3.980713
40	16.23779	130	1.655273	220	16.29089	310	1.66626
42	13.06458	132	-1.84021	222	12.73315	312	-2.02881
44	9.490356	134	-5.41992	224	9.592896	314	-5.4364
46	5.974731	136	-9.4043	226	5.698242	316	-9.33105
48	2.404175	138	-12.6178	228	2.404175	318	-12.6654
50	-1.17187	140	-16.1389	230	-1.14624	320	-16.0803
52	-3.48083	142	-17.796	232	-3.46619	322	-17.6166
54	-4.52271	144	-18.8104	234	-4.61975	324	-18.5577
56	-5.70923	146	-19.4824	236	-5.70374	326	-19.6362
58	-6.61743	148	-19.9402	238	-6.66687	328	-20.0574
60	-7.38831	150	-20.1306	240	-7.23999	330	-20.1324
62	-8.08594	152	-20.2991	242	-7.89734	332	-20.2917
64	-10.2429	154	-22.326	244	-10.4224	334	-22.2601
66	-12.2662	156	-23.3386	246	-12.3468	336	-23.2654
68	-14.5001	158	-24.7339	248	-14.295	338	-24.6991
70	-16.0071	160	-25.4718	250	-15.8606	340	-25.4828
72	-17.3346	162	-26.1438	252	-17.439	342	-26.1346
74	-18.3875	164	-26.2976	254	-18.3289	344	-26.3727
76	-18.8013	166	-25.6311	256	-18.8672	346	-25.6219
78	-18.9478	168	-25.2484	258	-18.8361	348	-25.2118
80	-15.7855	170	-20.7568	260	-15.921	350	-20.7623
82	-10.946	172	-15.3589	262	-11.0815	352	-15.3351
84	-6.09558	174	-9.42993	264	-6.2439	354	-9.33838
86	-4.07043	176	-6.22375	266	-4.04297	356	-6.21277
88	-1.63879	178	-2.95349	268	-1.66626	358	-3.04504

Table II – Anomaly #2 Correction Factor (Minutes)

ORDERING INFORMATION [4]

AEROFLEX PART # [1]	SCREENING	PACKAGE
ACT5028-1-EM	Class C, Rev. A Silicon [2 3]	CLCC
ACT5028-2-S	Class K (DSCC QML Pending), Rev. A Silicon [2 3]	CQFP
ACT5028-2-7	Class C, Rev. A Silicon [2 3]	CQFP
ACT5028-2-I	Class I, Rev. A Silicon [2 3]	CQFP

Notes

1. The first dash number indicates the package style (-1 = CLCC or -2 = CQFP).
   The middle dash number indicates the die revision level, First four Part Numbers above are initial release silicon, thus no middle #.
   The last dash number indicates the testing level of the part:
   - Class C = Commercial Flow, Commercial Temp. Range, 0^oC to $+70^oC$ testing
   - Class I = Commercial Flow, Industrial Temp. Range, -40^oC to $+85^oC$ testing
   - Class K = MIL-PRF-38534 Flow, -45^oC to $+125^oC$ testing (Rev. A Silicon)
2. Rev. A silicon has an offset at each angle with different magnitudes which are repeatable from chip to chip. This offset must be substracted out from the value being read to achieve the accuracy indicated in this data sheet.
3. See Errata information Anomaly #1, 2 & 3 within this data sheet.
4. Obsolete for future designs. Use ACT5028B product.

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