

June 1989

CMOS 16 Bit Microprocessor

Features

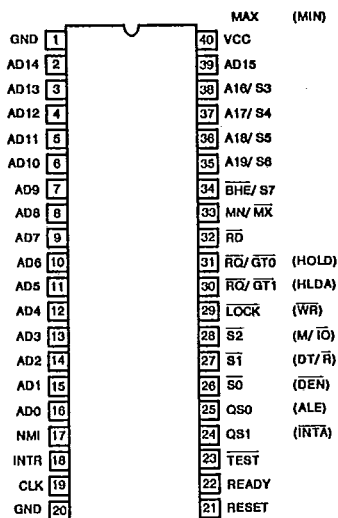
- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with NMOS 8086
- 5MHz Operation 80C86/883
- 8MHz Operation 80C86-2/883
- Low Power Operation
 - ▶ ICCSB 500µA Max
 - ▶ ICCOP 10mA/MHz Max
- 1MByte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word and Block Move Operations
- 8 Bit and 16 Bit Signed/Unsigned Arithmetic
 - ▶ Binary, or Decimal
 - ▶ Multiply and Divide
- Operating Temperature Range -55°C to +125°C

Description

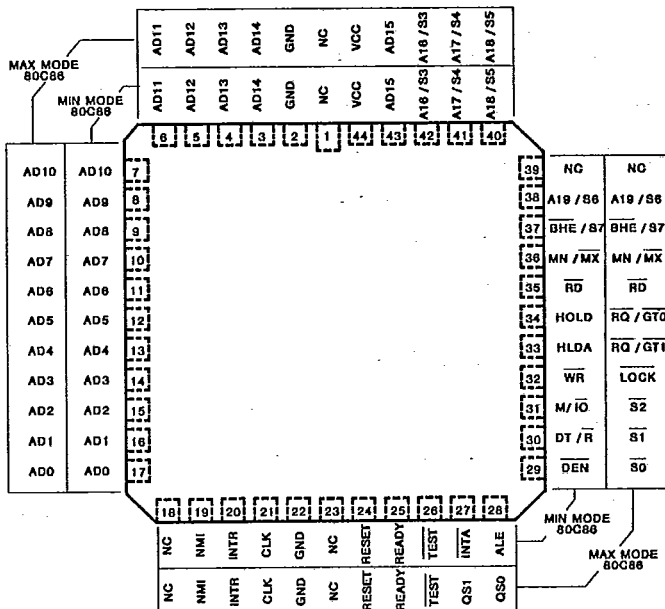
The Harris 80C86/883 high performance 16 bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Full TTL compatibility (with the exception of CLOCK) and industry standard operation allow use of existing NMOS 8086 hardware and software designs.

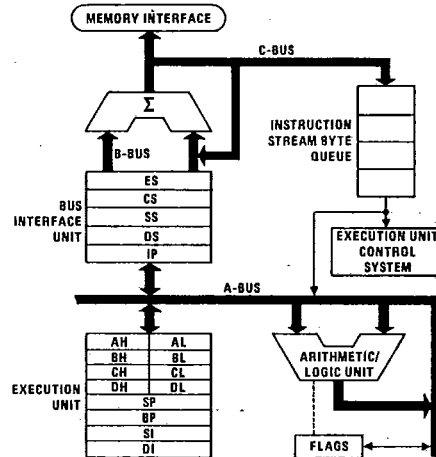
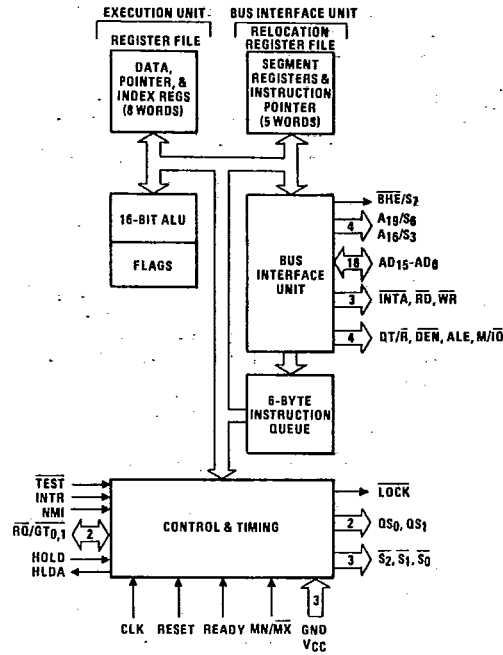
Pinouts

80C86/883 (CERAMIC DIP)
TOP VIEW



80C86/883 (CERAMIC LCC)
TOP VIEW





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CMOS
MICROPROCESSORS

Pin Description

The following pin function descriptions are for 80C86/883 interface connection to the 80C86/883 (without regard to systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus additional bus buffers).

T-49-17-15

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION | | | | | | | | | | | | | | | |
|--------------------------------------|------------|---------------------------------|---|-----|----|-----------------|---|---|----------------|---|---|--------------------------------|---|---|---------------------------------|---|---|------|
| AD15-AD0 | 2-16, 39 | I/O | <p>ADDRESS DATA BUS: These lines constitute the time multiplexed memory/I/O address (T1) and data (T2, T3, TW, T4) bus. A0 is analogous to BHE for the lower byte of the data bus, pins D7-D0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions (See BHE). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".</p> | | | | | | | | | | | | | | | |
| A19/S6 A18/S5 A17/S4 A16/S3 | 35-38 | O | <p>ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4. S6 is always LOW. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.</p> <p>This information indicates which segment register is presently being used for data accessing.</p> <p>These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>S4</th> <th>S3</th> <th>CHARACTERISTICS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Alternate Data</td> </tr> <tr> <td>0</td> <td>1</td> <td>Stack</td> </tr> <tr> <td>1</td> <td>0</td> <td>Code or None</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data</td> </tr> </tbody> </table> | S4 | S3 | CHARACTERISTICS | 0 | 0 | Alternate Data | 0 | 1 | Stack | 1 | 0 | Code or None | 1 | 1 | Data |
| S4 | S3 | CHARACTERISTICS | | | | | | | | | | | | | | | | |
| 0 | 0 | Alternate Data | | | | | | | | | | | | | | | | |
| 0 | 1 | Stack | | | | | | | | | | | | | | | | |
| 1 | 0 | Code or None | | | | | | | | | | | | | | | | |
| 1 | 1 | Data | | | | | | | | | | | | | | | | |
| BHE/S7 | 34 | O | <p>BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal (BHE) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use BHE to condition chip select functions. BHE is LOW during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3 and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T1 for the first interrupt acknowledge cycle.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BHE</th> <th>A0</th> <th>CHARACTERISTICS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Whole word</td> </tr> <tr> <td>0</td> <td>1</td> <td>Upper Byte from/to odd address</td> </tr> <tr> <td>1</td> <td>0</td> <td>Lower byte from/to even address</td> </tr> <tr> <td>1</td> <td>1</td> <td>None</td> </tr> </tbody> </table> | BHE | A0 | CHARACTERISTICS | 0 | 0 | Whole word | 0 | 1 | Upper Byte from/to odd address | 1 | 0 | Lower byte from/to even address | 1 | 1 | None |
| BHE | A0 | CHARACTERISTICS | | | | | | | | | | | | | | | | |
| 0 | 0 | Whole word | | | | | | | | | | | | | | | | |
| 0 | 1 | Upper Byte from/to odd address | | | | | | | | | | | | | | | | |
| 1 | 0 | Lower byte from/to even address | | | | | | | | | | | | | | | | |
| 1 | 1 | None | | | | | | | | | | | | | | | | |
| RD | 32 | O | <p>READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/I/O or S2 pin. This signal is used to read devices which reside on the 80C86/883 local bus. RD is active LOW during T2, T3 and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C86/883 local bus has floated.</p> <p>This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".</p> | | | | | | | | | | | | | | | |
| READY | 22 | I | <p>READY: Is the acknowledgement from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86/883 READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.</p> | | | | | | | | | | | | | | | |
| INTR | 18 | I | <p>INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</p> | | | | | | | | | | | | | | | |

Pin Description (Continued)

The following pin function descriptions are for 80C86/883 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 80C86/883 (without regard to additional bus buffers).

T-49-17-15

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION |
|--------|------------|------|--|
| TEST | 23 | I | TEST: Input is examined by the "Wait" instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK. |
| NMI | 17 | I | NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized. |
| RESET | 21 | I | RESET: causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized. |
| CLK | 19 | I | CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. |
| VCC | 40 | | VCC: +5V power supply pin. A 0.1 μF capacitor between pins 20 and 40 is recommended for decoupling. |
| GND | 1, 20 | | GND: Ground. Note: both must be connected. A 0.1 μF capacitor between pins 1 and 20 is recommended for decoupling. |
| MN/MX | 33 | I | MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections. |

The following pin function descriptions are for the 80C86/883 in minimum mode (i.e. MN/MX = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

MINIMUM MODE SYSTEM

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION |
|---------------|------------|------|---|
| M/I \bar{O} | 28 | O | STATUS LINE: logically equivalent to $\bar{S}2$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/I \bar{O} becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, IO = LOW). M/I \bar{O} is held to a high impedance logic one during local bus "hold acknowledge". |
| WR | 29 | O | WRITE: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/I \bar{O} signal. WR is active for T2, T3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge". |
| INTA | 24 | O | INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and TW of each interrupt acknowledge cycle. Note that INTA is never floated. |
| ALE | 25 | O | ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated. |
| DT/ \bar{R} | 27 | O | DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/ \bar{R} is equivalent to $\bar{S}1$ in maximum mode, and its timing is the same as for M/I \bar{O} (T = HIGH, R = LOW). DT/ \bar{R} is held to a high impedance logic one during local bus "hold acknowledge". |
| \bar{DEN} | 26 | O | DATA ENABLE: provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. \bar{DEN} is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. \bar{DEN} is held to a high impedance logic one during local bus "hold acknowledge". |

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CMOS
MICROPROCESSORS

Pin Description (Continued)

The following pin function descriptions are for the 80C86/883 in minimum mode (i.e. MN/MX = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

MINIMUM MODE SYSTEM (Continued)

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION |
|--------------|------------|--------|---|
| HOLD HLDA | 31, 30 | I O | HOLD: Indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or T1 clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. |

The following pin function descriptions are for the 80C86/883 system in maximum mode (i.e., MN/MX = GND). Only the pin functions which are unique to maximum mode are described below.

MAXIMUM MODE SYSTEM

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|-----------------|-----------------|--|-----------------|-----------------|-----------------|-----------------|---|---|---|-----------------------|---|---|---|---------------|---|---|---|----------------|---|---|---|------|---|---|---|-------------|---|---|---|-------------|---|---|---|--------------|---|---|---|---------|
| $\overline{S0}$ $\overline{S1}$ $\overline{S2}$ | 26 27 28 | O O O | STATUS: Is active during T4, T1 and T2 and is returned to the passive state (1, 1, 1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These signals are held at a high impedance logic one state during "grant sequence". <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>$\overline{S2}$</th> <th>$\overline{S1}$</th> <th>$\overline{S0}$</th> <th>CHARACTERISTICS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Interrupt Acknowledge</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Read I/O Port</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Write I/O Port</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Halt</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Code Access</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Read Memory</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Write Memory</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Passive</td> </tr> </tbody> </table> | $\overline{S2}$ | $\overline{S1}$ | $\overline{S0}$ | CHARACTERISTICS | 0 | 0 | 0 | Interrupt Acknowledge | 0 | 0 | 1 | Read I/O Port | 0 | 1 | 0 | Write I/O Port | 0 | 1 | 1 | Halt | 1 | 0 | 0 | Code Access | 1 | 0 | 1 | Read Memory | 1 | 1 | 0 | Write Memory | 1 | 1 | 1 | Passive |
| $\overline{S2}$ | $\overline{S1}$ | $\overline{S0}$ | CHARACTERISTICS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | Interrupt Acknowledge | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | Read I/O Port | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | Write I/O Port | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | Halt | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | Code Access | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | Read Memory | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | Write Memory | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | Passive | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RQ/GT0 RQ/GT1 | 31, 30 | I/O | REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with RQ/GT0 having higher priority than RQ/GT1. RQ/GT has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see RQ/GT Sequence Timing) <ol style="list-style-type: none"> 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86/883 (pulse 1). 2. During a T4 or T1 clock cycle, a pulse 1 CLK wide from the 80C86/883 to the requesting master (pulse 2) indicates that the 80C86/883 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86/883 (pulse 3) that the "hold" request is about to end and that the 80C86/883 can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending). <p>Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pin Description (Continued)

The following pin function descriptions are for the 80C86/883 system in maximum mode (i.e., MN/MX = GND). Only the pin functions which are unique to maximum mode are described below.

MAXIMUM MODE SYSTEM (Continued)

| SYMBOL | PIN NUMBER | TYPE | DESCRIPTION | | | | | | | | | | | | | | | |
|----------|------------|----------------------------------|---|-----|-----|--|---|---|--------------|---|---|----------------------------------|---|---|-----------------|---|---|----------------------------|
| | | | <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. <p>If the local bus is idle when the request is made the two possible events will follow:</p> <ol style="list-style-type: none"> 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied. | | | | | | | | | | | | | | | |
| LOCK | 29 | O | <p>LOCK: output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In MAX mode, LOCK is automatically generated during T2 of the first INTA cycle and removed during T2 of the second INTA cycle.</p> | | | | | | | | | | | | | | | |
| QS1, QS0 | 24, 25 | O | <p>QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed.</p> <p>QS1 and QS0 provide status to allow external tracking of the internal 80C86/883 instruction queue. Note that QS1, QS0 never become high impedance.</p> <table border="1" data-bbox="640 842 1020 1014"> <thead> <tr> <th>QS1</th> <th>QS0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>First byte of op code from queue</td> </tr> <tr> <td>1</td> <td>0</td> <td>Empty the Queue</td> </tr> <tr> <td>1</td> <td>1</td> <td>Subsequent byte from queue</td> </tr> </tbody> </table> | QS1 | QS0 | | 0 | 0 | No Operation | 0 | 1 | First byte of op code from queue | 1 | 0 | Empty the Queue | 1 | 1 | Subsequent byte from queue |
| QS1 | QS0 | | | | | | | | | | | | | | | | | |
| 0 | 0 | No Operation | | | | | | | | | | | | | | | | |
| 0 | 1 | First byte of op code from queue | | | | | | | | | | | | | | | | |
| 1 | 0 | Empty the Queue | | | | | | | | | | | | | | | | |
| 1 | 1 | Subsequent byte from queue | | | | | | | | | | | | | | | | |

4
 CMOS MICROPROCESSORS

Absolute Maximum Ratings

| | |
|--|----------------------|
| Supply Voltage | +8.0V |
| Input, Output or I/O Voltage Applied | GND-0.5V to VCC+0.5V |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | +175°C |
| Lead Temperature (Soldering 10 sec) | +300°C |
| ESD Classification | Class 1 |

Reliability Information

| | | |
|---|---------------|---------------|
| Thermal Resistance | θ_{ja} | θ_{jc} |
| Ceramic DIP Package | 27.5°C/W | 5.9°C/W |
| Ceramic LCC Package | 62.2°C/W | 8.6°C/W |
| Maximum Package Power Dissipation at +125°C | | |
| Ceramic DIP Package | 620mW | |
| Ceramic LCC Package | 664mW | |
| Gate Count | 9750 Gates | |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

| | | | |
|--------------------------------|------------------|-----------------------------------|-----------------|
| Operating Supply Voltage | +4.5V to +5.5V | Operating Temperature Range | -55°C to +125°C |
| 80C86-2/883 ONLY | +4.75V to +5.25V | | |

TABLE 1. 80C86/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, fmax = 5MHz;
80C86-2/883: VCCL = 4.75V, VCCH = 5.25V, fmax = 8MHz

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|--------------------------------|--------|--|----------------------|---------------------|----------------|------|--------|
| | | | | | MIN | MAX | |
| Logical One Input Voltage | VIH | VCC = VCCH, Note 2 | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | 2.2 | - | V |
| Logical Zero Input Voltage | VIL | Note 2 | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | - | 0.8 | V |
| CLK Logical One Input Voltage | VIHC | VCC = VCCH | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | VCC-0.8 | - | V |
| CLK Logical Zero Input Voltage | VILC | | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | - | 0.8 | V |
| Output HIGH Voltage | VOH | IOH = -2.5mA, Note 3 IOH = -100µA, Note 3 | 1, 2, 3 1, 2, 3 | -55°C ≤ TA ≤ +125°C | 3.0 VCC-0.4 | - | V V |
| Output LOW Voltage | VOL | IOL = +2.5mA, Note 3 | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | - | 0.4 | V |
| Input Leakage Current | II | VCC = VCCH, VIN = GND or VCC DIP Pins: 17-19, 21-23, 33 | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | -1.0 | +1.0 | µA |
| Input Current Bus Hold High | IBHH | VIN = 3.0V, Note 4 VCC = VCCL & VCCH | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | -40 | -400 | µA |
| Input Current Bus Hold Low | IBHL | VIN = 0.8V, Note 5 VCC = VCCL & VCCH | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | 40 | 400 | µA |
| Output Leakage Current | IO | VCC = VCCH, VOUT = 0V, Note 6 | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | - | -10 | µA |
| Standby Power Supply Current | ICCSB | VCC = VCCH, Note 7 | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | - | 500 | µA |
| Operating Power Supply Current | ICCOP | VCC = VCCH, f = fmax, VIN = VCC or GND, Outputs Open | 1, 2, 3 | -55°C ≤ TA ≤ +125°C | - | 10 | mA/MHz |

- NOTES: 1. All voltages referenced to device GND, VCC = VCCL unless otherwise specified.
2. MN/MX is a strap option and should be held to VCC or GND.
3. Interchanging of force and sense conditions is permitted.
4. IBHH should be measured after raising VIN to VCC and then lowering to valid input high level of 3.0V on the following pins: 2-16, 28-32, 34-39.
5. IBHL should be measured after lowering VIN to GND and then raising to valid input low level of 0.8V on the following pins: 2-16, 34-39.
6. IO should be measured by putting the pin in a high impedance state and then driving VOUT to GND on the following pins: 28-29, 32.
7. ICCSB tested during clock high time after HALT instruction execution. VIN = VCC or GND, VCC = VCCH, outputs unloaded.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Specifications 80C86/883

HARRIS SEMICOND SECTOR 16E D 4302271 0014799 5

TABLE 2. 80C86/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUB-GROUPS | TEMPERATURE | 80C86-2/883 | | 80C86/883 | | UNITS |
|------------------------------------|------------|---------------------|--------------------|---------------------------------|-------------------|-----|-------------------|-----|-------|
| | | | | | MIN | MAX | MIN | MAX | |
| MINIMUM COMPLEXITY SYSTEM TIMING | | | | | | | | | |
| CLK Cycle Period | (1)TCLCL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 125 | - | 200 | - | ns |
| CLK Low Time | (2)TCLCH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 68 | - | 118 | - | ns |
| CLK High Time | (3)TCHCL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 44 | - | 69 | - | ns |
| Data In Setup Time | (6)TDVCL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 20 | - | 30 | - | ns |
| Data In Hold Time | (7)TCLDX1 | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | - | 10 | - | ns |
| READY Setup Time into 80C86/883 | (10)TRYHCH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 68 | - | 118 | - | ns |
| READY Hold Time into 80C86/883 | (11)TCHRYX | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 20 | - | 30 | - | ns |
| READY Inactive to CLK | (12)TRYLCL | Note 2 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | -8 | - | -8 | - | ns |
| HOLD Setup Time | (13)THVCH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 20 | - | 35 | - | ns |
| INTR, NMI, TEST Setup Time | (14)TINVCH | Note 3 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 15 | - | 30 | - | ns |
| Address Valid Delay | (17)TCLAV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 60 | 10 | 110 | ns |
| Address Hold Time | (18)TCLAX | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | - | 10 | - | ns |
| ALE Width | (22)TLHLL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | TCLCH -10 | - | TCLCH -20 | - | ns |
| ALE Active Delay | (23)TCLLH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | - | 50 | - | 80 | ns |
| ALE Inactive Delay | (24)TCHLL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | - | 55 | - | 85 | ns |
| Address Hold Time to ALE Inactive | (25)TLLAX | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | TCHCL -10 | - | TCHCL -10 | - | ns |
| Data Valid Delay | (26)TCLDV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 60 | 10 | 110 | ns |
| Control Active Delay 1 | (29)TCVCTV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 70 | 10 | 110 | ns |
| Control Active Delay 2 | (30)TCHCTV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 60 | 10 | 110 | ns |
| Control Inactive Delay | (31)TCVCTX | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 70 | 10 | 110 | ns |
| Address Float to RD Active | (32)TAZRL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 0 | - | 0 | - | ns |
| RD Active Delay | (33)TCLRL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 100 | 10 | 165 | ns |
| RD Inactive Delay | (34)TCLRH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 80 | 10 | 150 | ns |
| RD Inactive to Next Address Active | (35)TRHAV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | TCLCL -40 | - | TCLCL -45 | - | ns |
| HLDA Valid Delay | (36)TCLHAV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 100 | 10 | 160 | ns |
| RD Width | (37)TRLRH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 2 TCLCL -50 | - | 2 TCLCL -75 | - | ns |
| WR Width | (38)TWLWH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 2 TCLCL -40 | - | 2 TLCL -60 | - | ns |

NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
 2. Applies only to T2 state (8ns into T3)
 3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

4
CMOS
MICROPROCESSORS

TABLE 2. 80C86/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUB-GROUPS | TEMPERATURE | 80C86-2/883 | | 80C86/883 | | UNITS |
|----------------------------------|-----------|---------------------|--------------------|--|--------------|-----|--------------|-----|-------|
| | | | | | MIN | MAX | MIN | MAX | |
| MINIMUM COMPLEXITY SYSTEM TIMING | | | | | | | | | |
| Address Valid to ALE Low | (39)TAVAL | | 9, 10, 11 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | TCLCH -40 | - | TCLCH -60 | - | ns |
| Output Rise Time | (40)TOLOH | From 0.8V to 2.0V | 9, 10, 11 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 15 | - | 20 | ns |
| Output Fall Time | (41)TOHOL | From 2.0V to 0.8V | 9, 10, 11 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 15 | - | 20 | ns |

- NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
 2. Applies only to T2 state (8ns into T3)
 3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

TABLE 3. 80C86/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | NOTES | TEMPERATURE | 80C86-2/883 | | 80C86/883 | | UNITS |
|----------------------------------|-------------|--|---------|--|--------------|-----|--------------|-----|-------|
| | | | | | MIN | MAX | MIN | MAX | |
| MINIMUM COMPLEXITY SYSTEM TIMING | | | | | | | | | |
| Input Capacitance | CIN | f = 1MHz, All measurements are referenced device GND | 1 | $T_A = +25^{\circ}\text{C}$ | - | 25 | - | 25 | pF |
| Output Capacitance | COUO | | 1 | $T_A = +25^{\circ}\text{C}$ | - | 25 | - | 25 | pF |
| I/O Capacitance | C/O | | 1 | $T_A = +25^{\circ}\text{C}$ | - | 25 | - | 25 | pF |
| CLK Rise Time | TCH1CH2 (4) | From 1.0V to 3.5V | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 10 | - | 10 | ns |
| CLK Fall Time | TCL2CL1 (5) | From 3.5V to 1.0V | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 10 | - | 10 | ns |
| RDY Setup Time Into 82C84A | TR1VCL (8) | CL = 100pF, VCC = VCCL, f = 1MHz | 1, 2, 3 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | 35 | - | 35 | - | ns |
| RDY Hold Time Into 82C84A | TCLR1X (9) | CL = 100pF, VCC = VCCL, f = 1MHz | 1, 2, 3 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | 0 | - | 0 | - | ns |
| Input Rise Time (Except CLK) | TILIH (15) | From 0.8V to 2.0V | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 15 | - | 15 | ns |
| Input Fall Time (Except CLK) | TIHIL (16) | From 2.0V to 0.8V | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 15 | - | 15 | ns |
| Address Float Delay | TCLAZ (19) | CL = 100pF, VCC = VCCL, f = 1MHz | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | TCLAX | 50 | TCLAX | 80 | ns |
| Status Float Delay | TCHSZ (20) | | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | - | 50 | - | 80 | ns |
| Data Hold Time | TCLDX2 (27) | | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | 10 | - | 10 | - | ns |
| Data Hold Time After WR | TWHDX (28) | | 1 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | TCLCL -30 | - | TCLCL -30 | - | ns |

- NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
 2. Signal at 82C84A shown for reference only.
 3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. 80C86/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

| PARAMETER | SYMBOL | (NOTE 1) CONDI-TIONS | GROUP A SUB-GROUPS | TEMPERATURE | 80C86-2/883 | | 80C86/883 | | UNITS |
|---|------------|----------------------|--------------------|---------------------------------|-------------|-----------|-------------|-----------|-------|
| | | | | | MIN | MAX | MIN | MAX | |
| MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER) | | | | | | | | | |
| CLK Cycle Period | (1)TCLCL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 125 | - | 200 | - | ns |
| CLK Low Time | (2)TCLCH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 68 | - | 118 | - | ns |
| CLK High Time | (3)TCHCL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 44 | - | 69 | - | ns |
| Data In Setup Time | (6)TDVCL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 20 | - | 30 | - | ns |
| Data In Hold Time | (7)TCLDX1 | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | - | 10 | - | ns |
| READY Setup Time Into 80C86/883 | (10)TRYHCH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 68 | - | 118 | - | ns |
| READY Hold Time Into 80C86/883 | (11)TCHRYX | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 20 | - | 30 | - | ns |
| READY Inactive to CLK | (12)TRYLCL | Note 2 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | -8 | - | -8 | - | ns |
| Setup Time For Recognition (INTR, NMI, TEST) | (13)TINVCH | Note 3 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 15 | - | 30 | - | ns |
| RQ/GT Setup Delay | (14)TGVCH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 15 | - | 30 | - | ns |
| RQ Hold Time Into 80C86/883 | (15)TCHGX | Note 4 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 30 | TCHCL +10 | 40 | TCHCL +10 | ns |
| READY Active to Status Passive | (20)TRYHSH | Notes 2, 5 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | - | 65 | - | 110 | ns |
| Status Active Delay | (21)TCHSV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 60 | 10 | 110 | ns |
| Status Inactive Delay | (22)TCLSH | Note 5 | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 70 | 10 | 130 | ns |
| Address Valid Delay | (23)TCLAV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 60 | 10 | 110 | ns |
| Address Hold Time | (24)TCLAX | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | - | 10 | - | ns |
| Data Valid Delay | (33)TCLDV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 60 | 10 | 110 | ns |
| Address Float to Read Active | (37)TAZRL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 0 | - | 0 | - | ns |
| RD Active Delay | (38)TCLRL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 100 | 10 | 165 | ns |
| RD Inactive Delay | (39)TCLRHH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 10 | 80 | 10 | 150 | ns |
| RD Inactive to Next Address Active | (40)TRHAV | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | TCLCL -40 | - | TCLCL -45 | - | ns |
| GT Active Delay | (43)TCLGL | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 0 | 50 | 10 | 85 | ns |
| GT Inactive Delay | (44)TCLGH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 0 | 50 | 10 | 85 | ns |
| RD Width | (45)TRLRH | | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | 2 TCLCL -50 | - | 2 TCLCL -75 | - | ns |
| Output Rise Time | (46)TOLOH | From 0.8V to 2.0V | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | - | 15 | - | 20 | ns |
| Output Fall Time | (47)TOHOL | From 2.0V to 0.8V | 9, 10, 11 | -55°C ≤ T _A ≤ +125°C | - | 15 | - | 20 | ns |

- NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
 2. Applies only to T2 state (8ns Into T3)
 3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.
 4. The 80C86/883 actively pulls the RQ/GT pin to a logic one on the following clock low time.
 5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

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CMOS MICROPROCESSORS

Specifications 80C86/883

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TABLE 3. 80C86/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

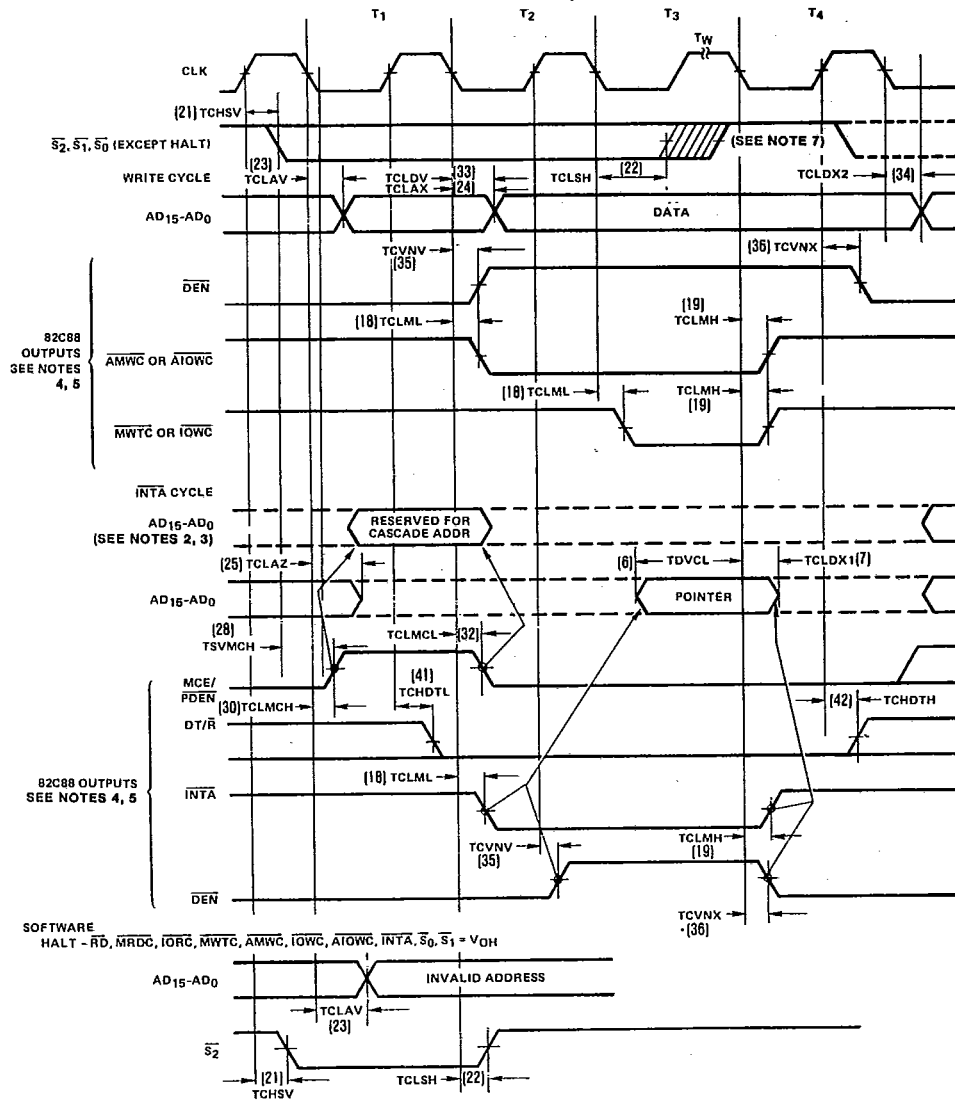
| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | NOTES | TEMPERATURE | 80C86-2/883 | | 80C86/883 | | UNITS |
|---|-------------|--|---------|---------------------------------|-------------|-----|-----------|-----|-------|
| | | | | | MIN | MAX | MIN | MAX | |
| MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER) | | | | | | | | | |
| Input Capacitance | CIN | f = 1MHz, All measurements are referenced device GND | 1 | T _A = +25°C | - | 25 | - | 25 | pF |
| Output Capacitance | COOUT | | 1 | T _A = +25°C | - | 25 | - | 25 | pF |
| I/O Capacitance | CIO | | 1 | T _A = +25°C | - | 25 | - | 25 | pF |
| CLK Rise Time | TCH1CH2 (4) | From 1.0V to 3.5V | 1 | -55°C ≤ T _A ≤ +125°C | - | 10 | - | 10 | ns |
| CLK Fall Time | TCL2CL1 (5) | From 3.5V to 1.0V | 1 | -55°C ≤ T _A ≤ +125°C | - | 10 | - | 10 | ns |
| RDY Setup Time Into 82C84A | TR1VCL (8) | CL = 100pF, VCC = VCCL, f = 1MHz | 1, 2, 3 | -55°C ≤ T _A ≤ +125°C | 35 | - | 35 | - | ns |
| RDY Hold Time Into 82C84A | TCLR1X (9) | CL = 100pF, VCC = VCCL, f = 1MHz | 1, 2, 3 | -55°C ≤ T _A ≤ +125°C | 0 | - | 0 | - | ns |
| Input Rise Time (Except CLK) | TIUH (16) | From 0.8V to 2.0V | 1 | -55°C ≤ T _A ≤ +125°C | - | 15 | - | 15 | ns |
| Input Fall Time (Except CLK) | TIHL (17) | From 2.0V to 0.8V | 1 | -55°C ≤ T _A ≤ +125°C | - | 15 | - | 15 | ns |
| Command Active Delay | TCLML (18) | CL = 100pF, VCC = VCCL, f = 1MHz | 1, 2 | -55°C ≤ T _A ≤ +125°C | 5 | 35 | 5 | 35 | ns |
| Command Inactive Delay | TCLMH (19) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | 5 | 35 | 5 | 35 | ns |
| Address Float Delay | TCLAZ (25) | | 1 | -55°C ≤ T _A ≤ +125°C | TCLAX | 50 | TCLAX | 80 | ns |
| Status Float Delay | (26)TCHSZ | | 1 | -55°C ≤ T _A ≤ +125°C | - | 50 | - | 80 | ns |
| Status Valid To ALE High | TSVLH (27) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 20 | - | 20 | ns |
| Status Valid To MCE High | TSVMCH (28) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 30 | - | 30 | ns |
| CLK Low To ALE Valid | TCLLH (29) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 20 | - | 20 | ns |
| CLK Low To MCE High | TCLMCH (30) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 25 | - | 25 | ns |
| ALE Inactive Delay | (31)TCHLL | | 1, 2 | -55°C ≤ T _A ≤ +125°C | 4 | 18 | 4 | 18 | ns |
| MCE Inactive Delay | (32)TCLMCL | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 15 | - | 15 | ns |
| Data Hold Time | (34)TCLDX2 | | 1 | -55°C ≤ T _A ≤ +125°C | 10 | - | 10 | - | ns |
| Control Active Delay | TCVNV (35) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | 5 | 45 | 5 | 45 | ns |
| Control Inactive Delay | TCVNX (36) | | 1, 2 | -55°C ≤ T _A ≤ +125°C | 10 | 45 | 10 | 45 | ns |
| Direction Control Active Delay | (41)TCHDTL | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 50 | - | 50 | ns |
| Direction Control Inactive Delay | (42)TCHDTH | | 1, 2 | -55°C ≤ T _A ≤ +125°C | - | 30 | - | 30 | ns |

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
 2. Signal at 82C84A or 82C88 shown for reference only.
 3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Wavetorms (Continued)

BUS TIMING - MAXIMUM MODE (USING 82C88) (Continued)

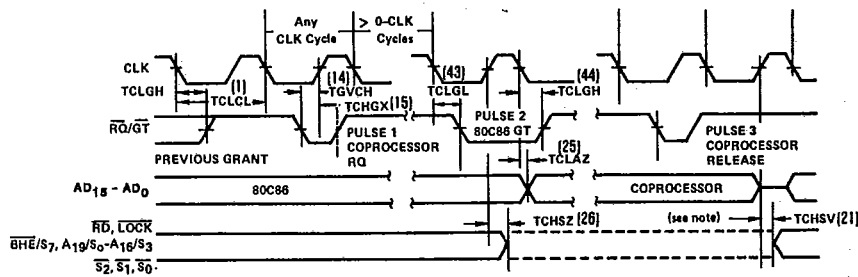


- NOTES: 1. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
 2. Cascade address is valid between first and second INTA cycles.
 3. Two INTA cycles run back-to-back. The 80C86/883 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
 4. Signals at 82C84A or 82C88 are shown for reference only.
 5. The issuance of the 82C88 command and control signals (MRDC, MWTC, AMWC, IOWC, AIOWC, INTA and DEN) lags the active high 82C88 CEN.
 6. All timing measurements are made at 1.5V unless otherwise noted.
 7. Status inactive in state just prior to T4.

Waveforms (Continued)

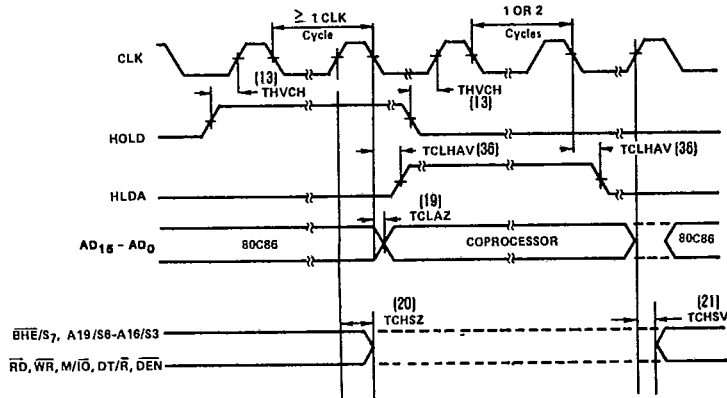
REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

T-49-17-15



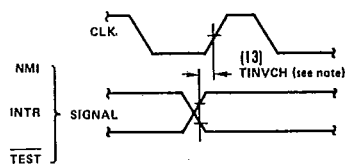
NOTE: The coprocessor may not drive the buses outside the region shown without risking contention

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



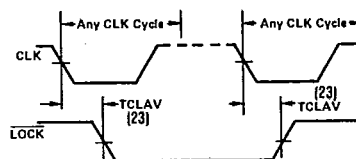
4
CMDS
MICROPROCESSORS

ASYNCHRONOUS SIGNAL RECOGNITION



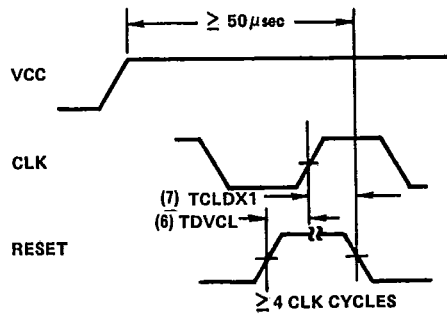
NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

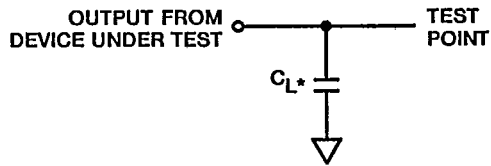


waveforms (Continued)

RESET TIMING

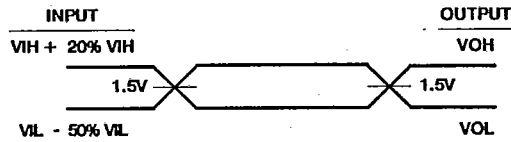


A.C. Test Circuit



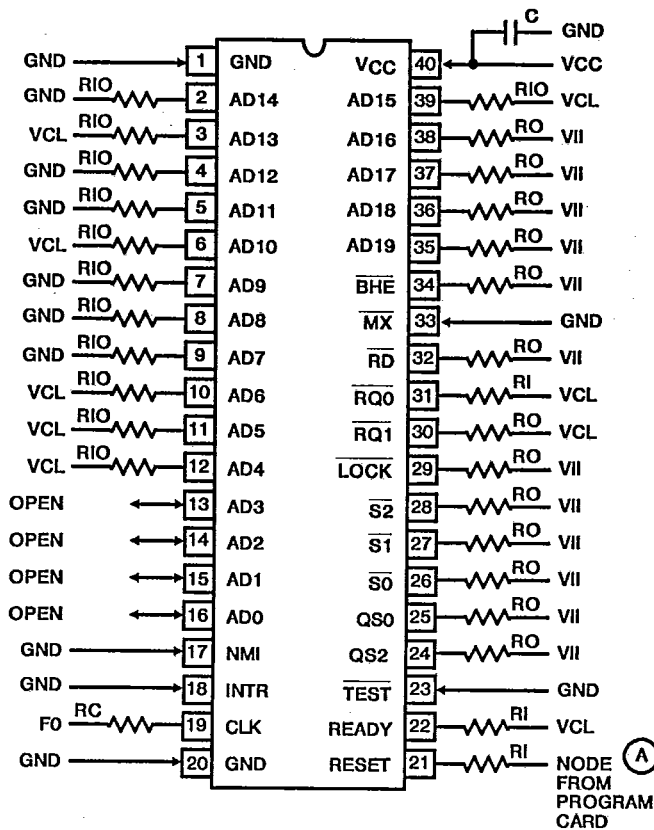
*Includes stray and jig capacitance

A.C. Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between $V_{ILmax} - 50\% V_{IL}$ and $V_{IHmin} + 20\% V_{IH}$. CLK must switch between 0.4V and $V_{CC} - 0.4$. Input rise and fall times are driven at 1ns/V.

80C86/883 CERAMIC DIP



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CMOS
MICROPROCESSORS

NOTES:

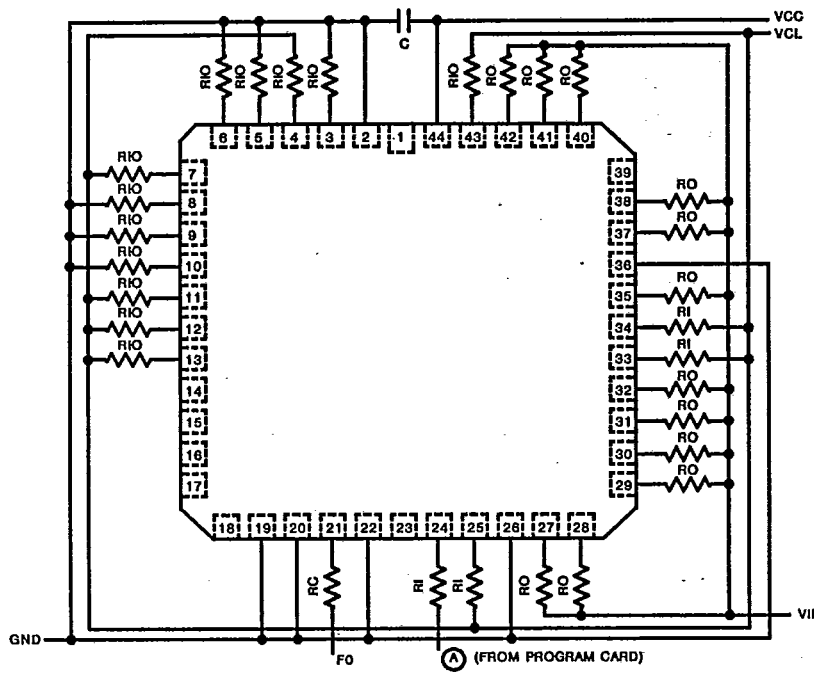
1. VCC = 5.5V ± 0.5V, GND = 0V
2. Input Voltage Limits:
VIL (Maximum) = 0.4V
VIH (Minimum) = 2.6V
3. VII is external supply set to 2.7V
4. VCL is generated on program card (VCC - 1.2V)
5. Pins 13 - 16 Input sequenced instructions from internal hold devices.

COMPONENTS: (Per Card)

1. RI = 10kΩ ± 5%, 1/4W (4)
2. RO = 1.2kΩ ± 5%, 1/4W (12)
3. RIO = 2.7kΩ ± 5%, 1/4W (16)
4. RC = 1kΩ ± 5%, 1/4W (1)
5. C = 0.01μF (Minimum) (1)

Burn-In Circuits (Continued)

80C86/883 CERAMIC LCC



NOTES:

1. VCC = 5.5V ± 0.5V, GND = 0V
2. Input Voltage Limits:
 VIL (Maximum) = 0.4V
 VIH (Minimum) = 2.6V
3. VII is external supply set to 2.7V
4. VCL is generated on program card (VCC - 1.2V)

COMPONENTS: (Per Card)

1. R1 = 10kΩ ± 5%, 1/4W (4)
2. R0 = 1.2kΩ ± 5%, 1/4W (12)
3. R10 = 2.7kΩ ± 5%, 1/4W (16)
4. RC = 1kΩ ± 5%, 1/4W (1)
5. C = 0.01μF (Minimum) (1)

Metallization Topology

DIE DIMENSIONS:

249.2 x 290.9 x 19 ± 1 mls

METALLIZATION:

Type: Silicon - Aluminum
 Thickness: 11kÅ ± 2kÅ

GLASSIVATION:

Type: Nitrox
 Thickness: 10kÅ ± 2kÅ

DIE ATTACH:

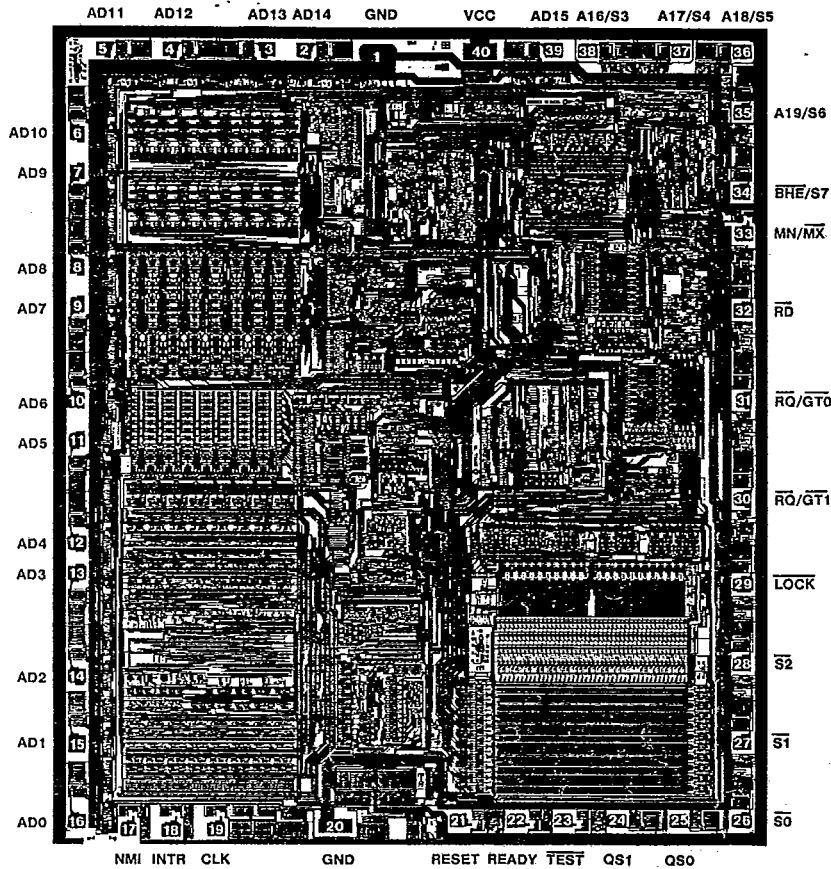
Material: Gold - Silicon Eutectic Alloy
 Temperature: Ceramic DIP — 460°C (Max)
 Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:

1.5 x 10⁵ A/cm²

Metallization Mask Layout

80C86/883



4
 CMOS
 MICROPROCESSORS

HARRIS SEMICOND SECTOR

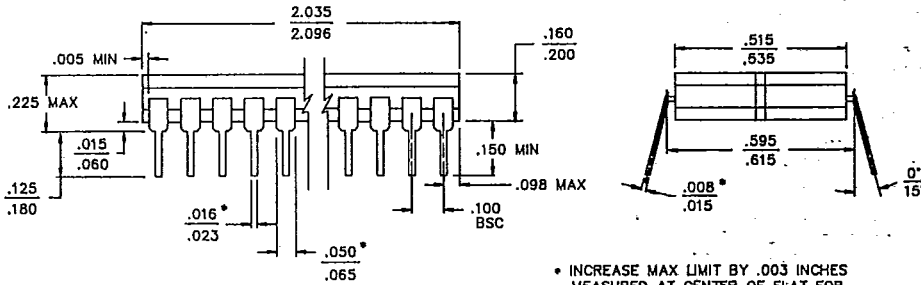
80C86/883

16E D

4302271 0014812 4

Packaging¹

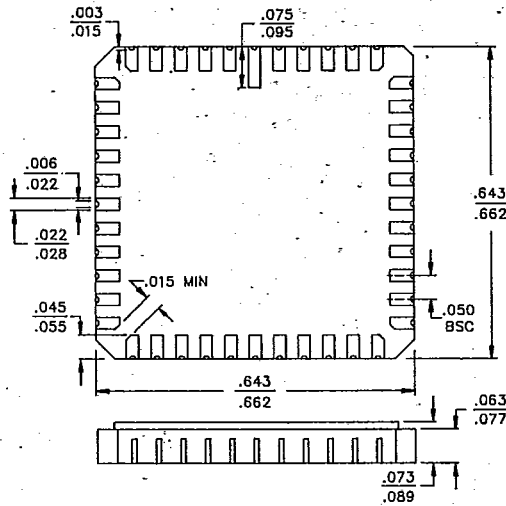
40 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
 Material: Glass Frit
 Temperature: 450°C ± 10°C
 Method: Furnace Seal

INTERNAL LEAD WIRE:
 Material: Aluminum
 Diameter: 1.25 Mil
 Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

**44 PAD CERAMIC LCC
 BOTTOM VIEW**



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
 Material: Gold/Tin (80/20)
 Temperature: 320°C ± 10°C
 Method: Furnace Braze

INTERNAL LEAD WIRE:
 Material: Aluminum
 Diameter: 1.25 Mil
 Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

[†]MIL-M-38510 Compliant Materials, Finishes, and Dimensions.



80C86

DESIGN INFORMATION

T-49-17-15

CMOS 16 Bit Microprocessor

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Functional Description

Static Operation

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system

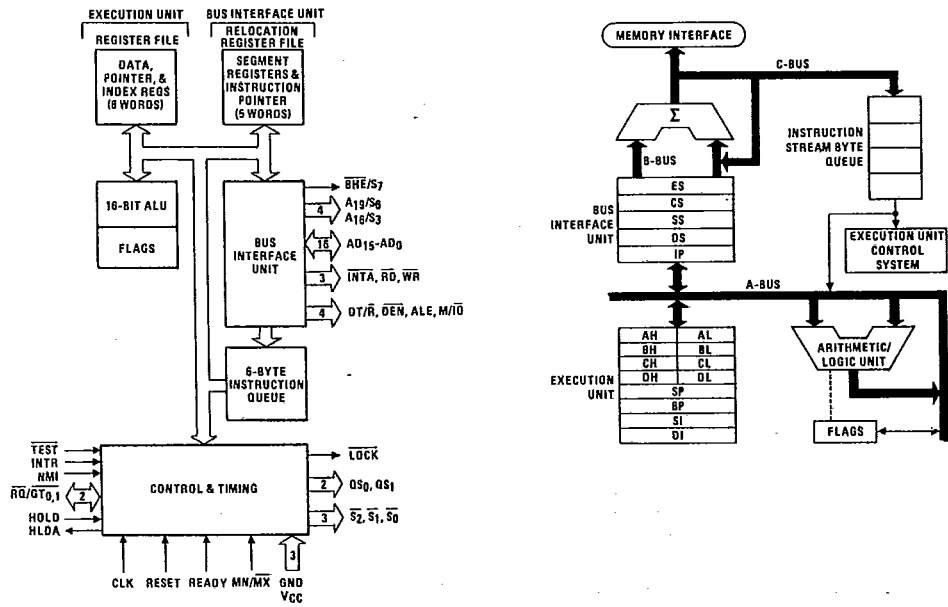
frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current, (500µA maximum).

Internal Architecture

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

Functional Diagram



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CMOS
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DESIGN INFORMATION (Continued)

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The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead-time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20 bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

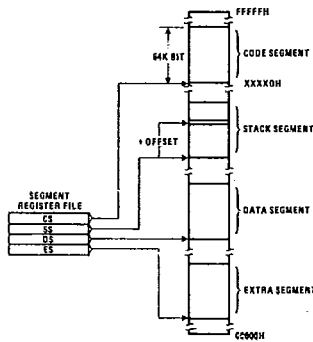


FIGURE 1. 80C86 MEMORY ORGANIZATION

TABLE A.

| TYPE OF MEMORY REFERENCE | DEFAULT SEGMENT BASE | ALTER- NATE SEGMENT BASE | OFFSET |
|-----------------------------|----------------------|--------------------------|-------------------|
| Instruction Fetch | CS | None | IP |
| Stack Operation | SS | None | SP |
| Variable (except following) | DS | CS, ES, SS | Effective Address |
| String Source | DS | CS, ES, SS | SI |
| String Destination | ES | None | DI |
| BP Used As Base Register | SS | CS, DS, ES | Effective Address |

All memory references are made relative to base addresses contained in high speed segment registers. The segment

types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table A. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table A).

Word (16 bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals, \overline{BHE} and A0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed thru its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

DESIGN INFORMATION (Continued)

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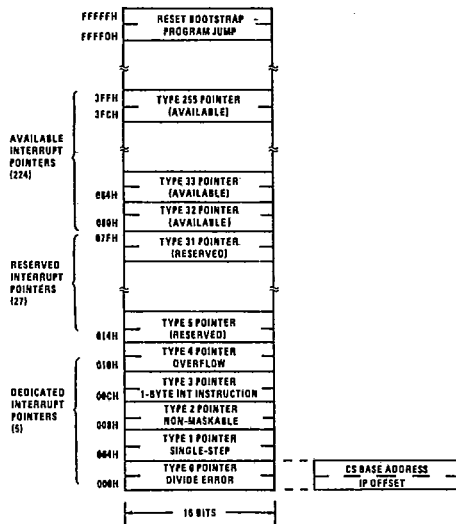


FIGURE 2. RESERVED MEMORY LOCATIONS

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum 80C86 systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/MX) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/MX pin is strapped to GND, the 80C86 defines pins 24 through 31 and 34 in maximum mode. When the MN/MX pin is strapped to VCC, the 80C86 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C86 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C86 processing power in a highly integrated form.

The demultiplexed mode requires two 82C82 latches (for 64K addressability) or three 82C82 latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See Figure 6a.) The 80C86 provides DEN and DT/R to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See Figure 6b). The 82C88 decodes status lines S0, S1 and S2, and provides the system with all bus control signals.

Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C86 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C86 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

Bus Operation

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40 lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 (see Figure 3). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T3 and T4. Each inserted wait state is the same duration as a CLK cycle. Periods can occur between 80C86 driven bus cycles. These are referred to as "idle" states (TI) or inactive CLK cycles. The processor uses these cycles for internal housekeeping and processing.

During T1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/MX strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits S0, S1 and S2 are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table B.

TABLE B.

| S2 | S1 | S0 | CHARACTERISTICS |
|----|----|----|------------------------|
| 0 | 0 | 0 | Interrupt |
| 0 | 0 | 1 | Read I/O |
| 0 | 1 | 0 | Write I/O |
| 0 | 1 | 1 | Halt |
| 1 | 0 | 0 | Instruction Fetch |
| 1 | 0 | 1 | Read Data from Memory |
| 1 | 1 | 0 | Write Data to Memory |
| 1 | 1 | 1 | Passive (no bus cycle) |

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DESIGN INFORMATION (Continued)

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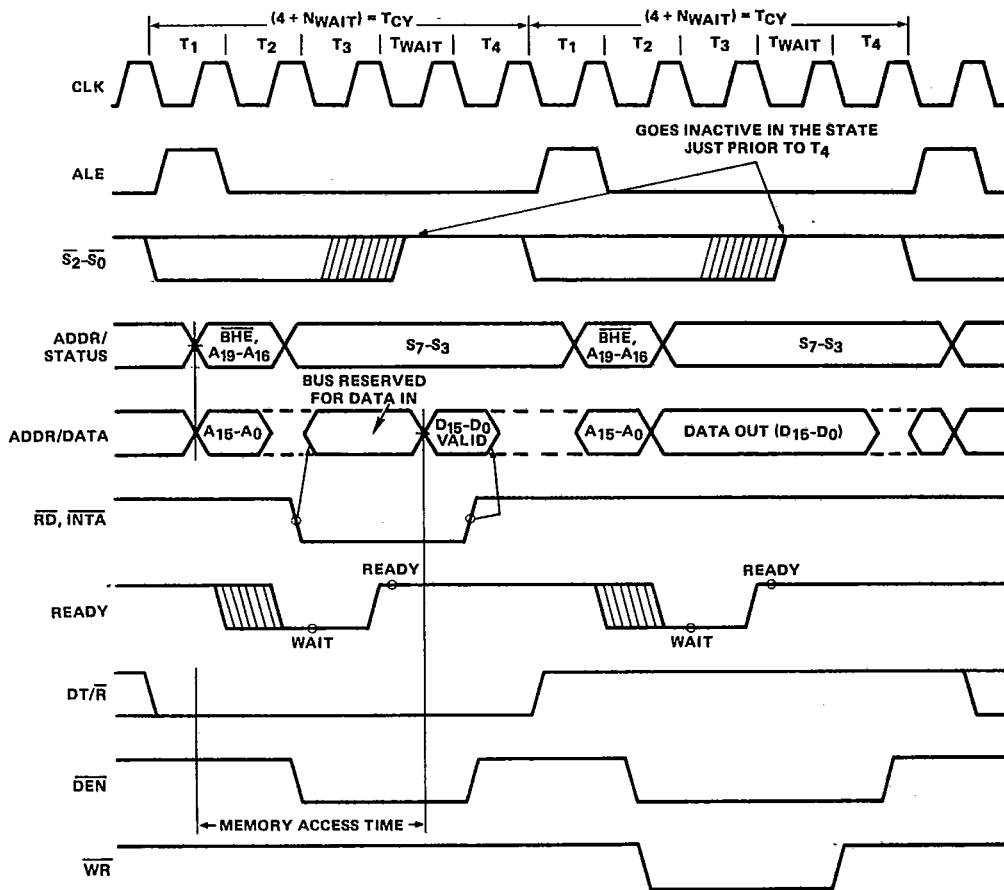


FIGURE 3. BASIC SYSTEM TIMING

DESIGN INFORMATION (Continued)

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Status bits S3 through S7 are time multiplexed with high order address bits and the BHE signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table C.

TABLE C.

| S4 | S3 | CHARACTERISTICS |
|----|----|--------------------------------|
| 0 | 0 | Alternate Data (extra segment) |
| 0 | 1 | Stack |
| 1 | 0 | Code or None |
| 1 | 1 | Data |

S5 is a reflection of the PSW interrupt enable bit. S6 is always zero and S7 is a spare status bit.

I/O Addressing

In the 80C86, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8 bit peripheral located on the lower portion of the bus be addressed as even.

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval, the 80C86 operates normally beginning with the instruction in absolute location FFFF0H. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50µs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the 80C86.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C86 pins 2-16, 26-32 and 34-39. (See Figure 4a and 4b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400µA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

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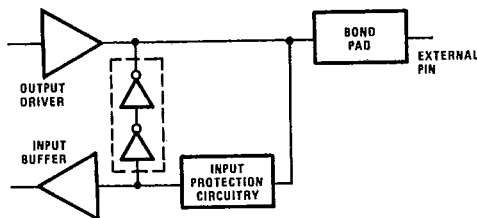


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

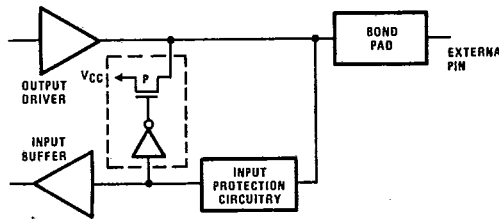


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

DESIGN INFORMATION (Continued)

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Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8 bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the INTA sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first INTA signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the LOCK signal (Max mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the 80C86 by the 82C59A Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector look-up table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

Halt

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, $\overline{S0}$

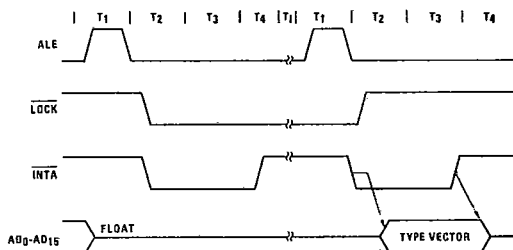


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

DESIGN INFORMATION (Continued)

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and the 82C88 bus controller issues one ALE. The 80C86 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the 80C86 out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via Lock

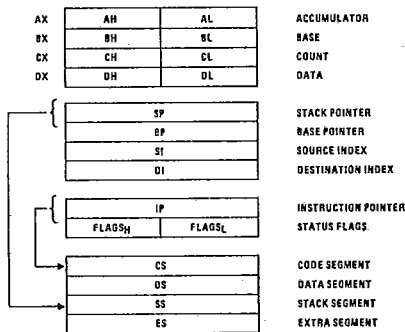
The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory Instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The LOCK signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While LOCK is active a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded and then honored at the end of the LOCK.

External Synchronization Via TEST

As an alternative to interrupts, the 80C86 provides a single software-testable input pin (\overline{TEST}). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the TEST input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C86 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C86 will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and reexecuted.

TABLE D. 80C86 REGISTER MODEL



Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/MX pin is strapped to VCC and the processor emits bus control signals (e.g. RD, WR, etc.) directly. In maximum mode, the MN/MX pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS™ compatible bus control signals. Figure 3 shows the signal timing relationships.

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82/82C83 latch. The BHE and A0 signals address the low, high or both bytes. From T1 to T4 the M/I \overline{O} signal indicates a memory or I/O operation. At T2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at T2. The read (\overline{RD}) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again three-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the 80C86 local bus, signals DT/R and \overline{DEN} are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/I \overline{O} signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3 and TW, the processor asserts the write control signal. The write (\overline{WR}) signal becomes active at the beginning of T2 as opposed to the read which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The BHE and A0 signals are used to select the proper byte(s) of the memory/I/O word to be read or written according to Table E.

TABLE E.

| BHE | A0 | CHARACTERISTICS |
|-----|----|---------------------------------|
| 0 | 0 | Whole word |
| 0 | 1 | Upper byte from/to odd address |
| 1 | 0 | Lower byte from/to even address |
| 1 | 1 | None |

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D8.

4
CMOS
MICROPROCESSORS

DESIGN INFORMATION (Continued)

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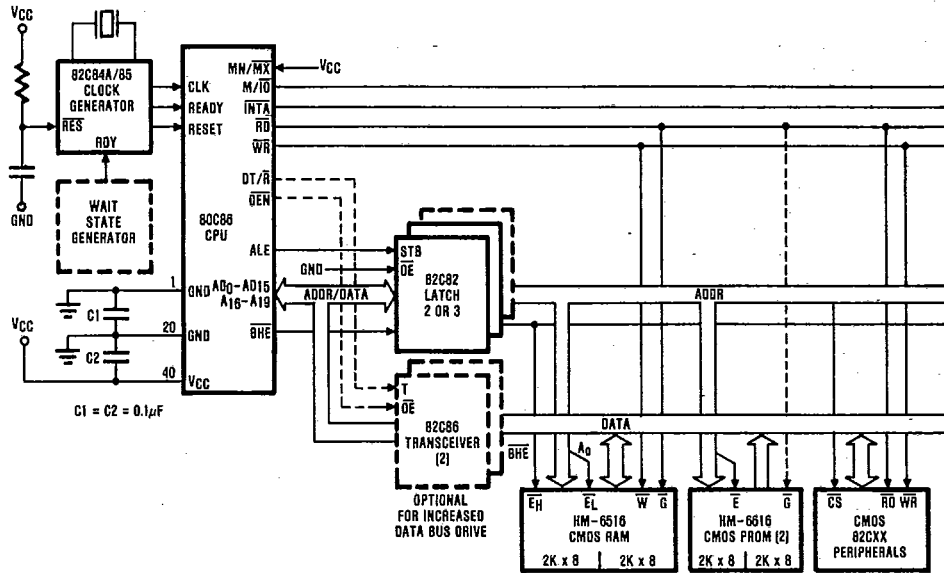


FIGURE 6A. MINIMUM MODE 80C86 TYPICAL CONFIGURATION

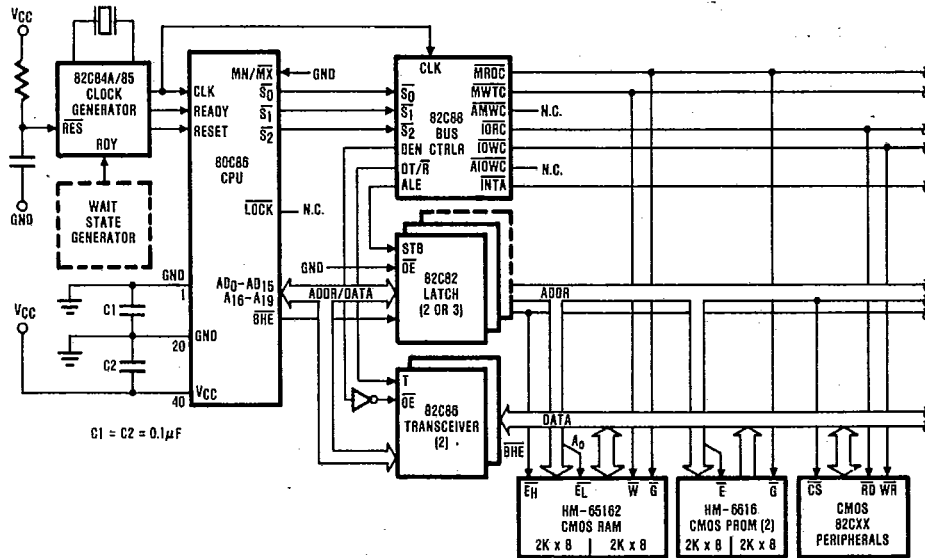


FIGURE 6B. MAXIMUM MODE 80C86 TYPICAL CONFIGURATION

DESIGN INFORMATION (Continued)

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The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal (\overline{INTA}) is asserted in place of the read (\overline{RD}) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive \overline{INTA} cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e. 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

Bus Timing - Medium Size Systems

For medium complexity systems the $\overline{MN}/\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C86 is capable of handling. Signals ALE, \overline{DEN} , and $\overline{DT}/\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C86

status outputs ($\overline{S2}$, $\overline{S1}$ and $\overline{S0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and \overline{OE} inputs from the 82C88 $\overline{DT}/\overline{R}$ and DEN signals.

The pointer into the interrupt vector table, which is passed during the second \overline{INTA} cycle, can be derived from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

DESIGN INFORMATION (Continued)

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INSTRUCTION SET SUMMARY

| Mnemonic and Description | Instruction Code | | | |
|---------------------------------------|------------------|---------------|-------------|-------------|
| DATA TRANSFER | | | | |
| MOV = Move: | 76543210 | 76543210 | 76543210 | 76543210 |
| Register/Memory to/from Register | 100010dw | mod reg r/m | | |
| Immediate to Register/Memory | 1100011w | mod 000 r/m | data | data if w 1 |
| Immediate to Register | 1011w reg | data | data if w 1 | |
| Memory to Accumulator | 1010000w | addr-low | addr-high | |
| Accumulator to Memory | 1010001w | addr-low | addr-high | |
| Register/Memory to Segment Register** | 10001110 | mod 0 reg r/m | | |
| Segment Register to Register/Memory | 10001100 | mod 0 reg r/m | | |
| PUSH = Push: | | | | |
| Register/Memory | 11111111 | mod 110 r/m | | |
| Register | 01010 reg | | | |
| Segment Register | 000 reg 110 | | | |
| POP = Pop: | | | | |
| Register/Memory | 10001111 | mod 000 r/m | | |
| Register | 01011 reg | | | |
| Segment Register | 000 reg 111 | | | |
| XCHG = Exchange: | | | | |
| Register/Memory with Register | 1000011w | mod reg r/m | | |
| Register with Accumulator | 10010 reg | | | |
| IN = Input from: | | | | |
| Fixed Port | 1110010w | port | | |
| Variable Port | 1110110w | | | |
| OUT = Output to: | | | | |
| Fixed Port | 1110011w | port | | |
| Variable Port | 1110111w | | | |
| XLAT = Translate Byte to AL | 11010111 | | | |
| LEA = Load EA to Register | 10001101 | mod reg r/m | | |
| LDS = Load Pointer to DS | 11000101 | mod reg r/m | | |
| LES = Load Pointer to ES | 11000100 | mod reg r/m | | |
| LAHF = Load AH with Flags | 10011111 | | | |
| SAHF = Store AH into Flags | 10011110 | | | |
| PUSHF = Push Flags | 10011100 | | | |
| POPF = Pop Flags | 10011101 | | | |

DESIGN INFORMATION (Continued)

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INSTRUCTION SET SUMMARY (Continued)

| Mnemonic and Description | Instruction Code | | | |
|--|------------------|-------------|---------------|------------------|
| | 76543210 | 76543210 | 76543210 | 76543210 |
| ARITHMETIC | | | | |
| ADD = Add: | | | | |
| Reg./Memory with Register to Either | 00000dw | mod reg r/m | | |
| Immediate to Register/Memory | 10000sw | mod 000 r/m | data | data if s:w = 01 |
| Immediate to Accumulator | 0000010w | data | data if w = 1 | |
| ADC = Add with Carry: | | | | |
| Reg./Memory with Register to Either | 00010dw | mod reg r/m | | |
| Immediate to Register/Memory | 10000sw | mod 010 r/m | data | data if s:w = 01 |
| Immediate to Accumulator | 0001010w | data | data if w = 1 | |
| INC = Increment: | | | | |
| Register/Memory | 1111111w | mod 000 r/m | | |
| Register | 01000reg | | | |
| AAA = ASCII Adjust for Add | 00110111 | | | |
| DAA = Decimal Adjust for Add | 00100111 | | | |
| SUB = Subtract: | | | | |
| Reg./Memory and Register to Either | 00101dw | mod reg r/m | | |
| Immediate from Register/Memory | 10000sw | mod 101 r/m | data | data if s:w = 01 |
| Immediate from Accumulator | 0010110w | data | data if w = 1 | |
| SBB = Subtract with Borrow | | | | |
| Reg./Memory and Register to Either | 00011dw | mod reg r/m | | |
| Immediate from Register/Memory | 10000sw | mod 011 r/m | data | data if s:w = 01 |
| Immediate from Accumulator | 0001110w | data | data if w = 1 | |
| DEC = Decrement: | | | | |
| Register/Memory | 1111111w | mod 001 r/m | | |
| Register | 01001reg | | | |
| NEG = Change Sign | 1111011w | mod 011 r/m | | |
| CMP = Compare: | | | | |
| Register/Memory and Register | 00111dw | mod reg r/m | | |
| Immediate with Register/Memory | 10000sw | mod 111 r/m | data | data if s:w = 01 |
| Immediate with Accumulator | 0011110w | data | data if w = 1 | |
| AAS = ASCII Adjust for Subtract | 00111111 | | | |
| DAS = Decimal Adjust for Subtract | 00101111 | | | |
| MUL = Multiply (Unsigned) | 1111011w | mod 100 r/m | | |
| IMUL = Integer Multiply (Signed) | 1111011w | mod 101 r/m | | |
| AAM = ASCII Adjust for Multiply | 11010100 | 00001010 | | |
| DIV = Divide (Unsigned) | 1111011w | mod 110 r/m | | |
| IDIV = Integer Divide (Signed) | 1111011w | mod 111 r/m | | |
| AAD = ASCII Adjust for Divide | 11010101 | 00001010 | | |
| CBW = Convert Byte to Word | 10011000 | | | |
| CWD = Convert Word to Double Word | 10011001 | | | |

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CMOS
MICROPROCESSORS

DESIGN INFORMATION (Continued)

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INSTRUCTION SET SUMMARY (Continued)

| Mnemonic and Description | Instruction Code | | | |
|---|------------------|-------------|---------------|---------------|
| | 76543210 | 76543210 | 76543210 | 76543210 |
| LOGIC | | | | |
| NOT = Invert | 1111011w | mod010r/m | | |
| SHL/SAL = Shift Logical/Arithmetic Left | 110100vw | mod100r/m | | |
| SHR = Shift Logical Right | 110100vw | mod101r/m | | |
| SAR = Shift Arithmetic Right | 110100vw | mod111r/m | | |
| ROL = Rotate Left | 110100vw | mod000r/m | | |
| ROR = Rotate Right | 110100vw | mod001r/m | | |
| RCL = Rotate Through Carry Flag Left | 110100vw | mod010r/m | | |
| RCR = Rotate Through Carry Right | 110100vw | mod011r/m | | |
| AND = And: | | | | |
| Reg./Memory and Register to Either | 001000dw | mod reg r/m | | |
| Immediate to Register/Memory | 1000000w | mod100r/m | data | data if w = 1 |
| Immediate to Accumulator | 0010010w | data | data if w = 1 | |
| TEST = And Function to Flags, No Result: | | | | |
| Register/Memory and Register | 1000010w | mod reg r/m | | |
| Immediate Data and Register/Memory | 1111011w | mod000r/m | data | data if w = 1 |
| Immediate Data and Accumulator | 1010100w | data | data if w = 1 | |
| OR = Or: | | | | |
| Reg./Memory and Register to Either | 000010dw | mod reg r/m | | |
| Immediate to Register/Memory | 1000000w | mod001r/m | data | data if w = 1 |
| Immediate to Accumulator | 0000110w | data | data if w = 1 | |
| XOR = Exclusive or: | | | | |
| Reg./Memory and Register to Either | 001100dw | mod reg r/m | | |
| Immediate to Register/Memory | 1000000w | mod110r/m | data | data if w = 1 |
| Immediate to Accumulator | 0011010w | data | data if w = 1 | |
| STRING MANIPULATION | | | | |
| REP = Repeat | 1111001z | | | |
| MOVS = Move Byte/Word | 1010010w | | | |
| CMPS = Compare Byte/Word | 1010011w | | | |
| SCAS = Scan Byte/Word | 1010111w | | | |
| LODS = Load Byte/Wd to AL/AX | 1010110w | | | |
| STOS = Stor Byte/Wd from AL/A | 1010101w | | | |
| CONTROL TRANSFER | | | | |
| CALL = Call: | | | | |
| Direct Within Segment | 11101000 | disp-low | disp-high | |
| Indirect Within Segment | 11111111 | mod010r/m | | |
| Direct Intersegment | 10011010 | offset-low | offset-high | |
| | | seg-low | seg-high | |
| Indirect Intersegment | 11111111 | mod011r/m | | |

DESIGN INFORMATION (Continued)

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INSTRUCTION SET SUMMARY (Continued)

| Mnemonic and Description | Instruction Code | | |
|--|------------------|-------------|-------------|
| | 76543210 | 76543210 | 76543210 |
| JMP = Unconditional Jump:- | | | |
| Direct Within Segment | 11101001 | disp-low | disp-high |
| Direct Within Segment-Short | 11101011 | disp | |
| Indirect Within Segment | 11111111 | mod 100 r/m | |
| Direct Intersegment | 11101010 | offset-low | offset-high |
| | | seg-low | seg-high |
| Indirect Intersegment | 11111111 | mod 101 r/m | |
| RET = Return from CALL: | | | |
| Within Segment | 11000011 | | |
| Within Seg Adding Immed to SP | 11000010 | data-low | data-high |
| Intersegment | 11001011 | | |
| Intersegment Adding Immediate to SP | 11001010 | data-low | data-high |
| JE/JZ = Jump on Equal/Zero | 01110100 | disp | |
| JL/JNGE = Jump on Less/Not Greater or Equal | 01111100 | disp | |
| JLE/JNG = Jump on Less or Equal/Not Greater | 01111110 | disp | |
| JB/JNAE = Jump on Below/Not Above or Equal | 01110010 | disp | |
| JBE/JNA = Jump on Below or Equal/Not Above | 01110110 | disp | |
| JP/JPE = Jump on Parity/Parity Even | 01111010 | disp | |
| JO = Jump on Overflow | 01110000 | disp | |
| JS = Jump on Sign | 01111000 | disp | |
| JNE/JNZ = Jump on Not Equal/Not Zero | 01110101 | disp | |
| JNL/JGE = Jump on Not Less/Greater or Equal | 01111101 | disp | |
| JNLE/JG = Jump on Not Less or Equal/Greater | 01111111 | disp | |
| JNB/JAE = Jump on Not Below/Above or Equal | 01110011 | disp | |
| JNBE/JA = Jump on Not Below or Equal/Above | 01110111 | disp | |
| JNP/JPO = Jump on Not Par/Par Odd | 01111011 | disp | |
| JNO = Jump on Not Overflow | 01110001 | disp | |
| JNS = Jump on Not Sign | 01111001 | disp | |
| LOOP = Loop CX Times | 11100010 | disp | |
| LOOPZ/LOOPE = Loop While Zero/Equal | 11100001 | disp | |
| LOOPNZ/LOOPNE = Loop While Not Zero/Equal | 11100000 | disp | |
| JCXZ = Jump on CX Zero | 11100011 | disp | |
| INT = Interrupt | | | |
| Type Specified | 11001101 | type | |
| Type 3 | 11001100 | | |
| INTO = Interrupt on Overflow | 11001110 | | |
| IRET = Interrupt Return | 11001111 | | |

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CMOS
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DESIGN INFORMATION (Continued)

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INSTRUCTION SET SUMMARY (Continued)

| Mnemonic and Description | Instruction Code | |
|-----------------------------------|------------------|------------|
| | 76543210 | 76543210 |
| PROCESSOR CONTROL | | |
| CLC = Clear Carry | 11111000 | |
| CMC = Complement Carry | 11110101 | |
| STC = Set Carry | 11111001 | |
| CLD = Clear Direction | 11111100 | |
| STD = Set Direction | 11111101 | |
| CLI = Clear Interrupt | 11111010 | |
| STI = Set Interrupt | 11111011 | |
| HLT = Halt | 11110100 | |
| WAIT = Wait | 10011011 | |
| ESC = Escape (to External Device) | 11011xxx | mod xxxr/m |
| LOCK = Bus Lock Prefix | 11110000 | |

NOTES:

- AL = 8-bit accumulator
- AX = 16-bit accumulator
- CX = Count register
- DS = Data segment
- ES = Extra segment
- Above/below refers to unsigned value.
- Greater = more positive;
- Less = less positive (more negative) signed values
- if d = 1 then "to" reg; if d = 0 then "from" reg
- if w = 1 then word instruction; if w = 0 then byte instruction
- if mod = 11 then r/m is treated as a REG field
- if mod = 00 then DISP = 0*, disp-low and disp-high are absent
- if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
- if mod = 10 then DISP = disp-high: disp-low
- if r/m = 000 then EA = (BX) + (SI) + DISP
- if r/m = 001 then EA = (BX) + (DI) + DISP
- if r/m = 010 then EA = (BP) + (SI) + DISP
- if r/m = 011 then EA = (BP) + (DI) + DISP
- if r/m = 100 then EA = (SI) + DISP
- if r/m = 101 then EA = (DI) + DISP
- if r/m = 110 then EA = (BP) + DISP*
- if r/m = 111 then EA = (BX) + DISP
- DISP follows 2nd byte of instruction (before data if required)
- *except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
- **MOV CS, REG/MEMORY not allowed.

- if s:w = 01 then 16 bits of immediate data form the operand.
- if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
- if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
- x = don't care
- z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

| 16-Bit (w = 1) | 8-Bit (w = 0) | Segment |
|----------------|---------------|---------|
| 000 AX | 000 AL | 00 ES |
| 001 CX | 001 CL | 01 CS |
| 010 DX | 010 DL | 10 SS |
| 011 BX | 011 BL | 11 DS |
| 100 SP | 100 AH | |
| 101 BP | 101 CH | |
| 110 SI | 110 DH | |
| 111 DI | 111 BH | |

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:
 FLAGS =
 X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Mnemonics © Intel, 1978

Packaging Techniques

T-90-20

Harris Semiconductor offers Leadless Chip Carriers (LCC) as a packaging option on various Digital Integrated Circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is comprised of the cavity and seal ring section of a standard DIP and offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC Packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

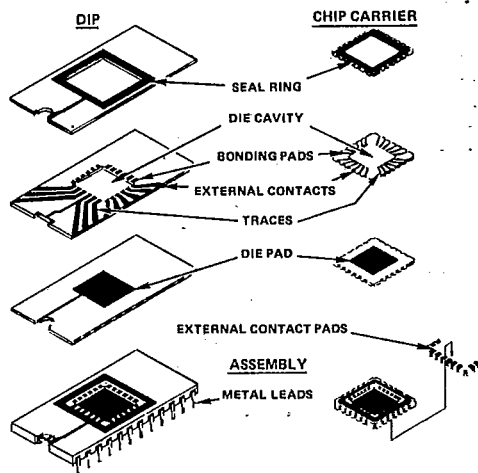


FIGURE 1. EXPLODED VIEW OF CHIP CARRIER AND DIP

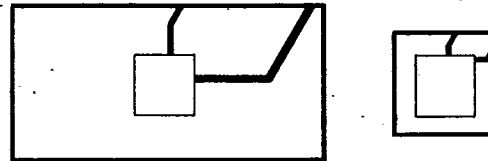
The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

TABLE 1.

| LEAD COUNT | LCC AREA | DIP AREA | DIP AREA vs. LCC AREA |
|------------|----------|----------|-----------------------|
| 18 | 0.10 | 0.22 | 220% |
| 28 | 0.20 | 0.84 | 420% |
| 48 | 0.31 | 1.68 | 542% |

(All Units in Square Inches)

The chart indicates a 220% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is a significantly smaller determinant of system performance.



| LEAD COUNT | LONGEST TRACE DIP | LONGEST TRACE SHORTEST TRACE | |
|------------|-------------------|------------------------------|-----|
| | | LCC | DIP |
| 18 | 2:1 | 1.5:1 | 6:1 |
| 24 | 4:1 | 1.5:1 | 3:1 |
| 40 | 5:1 | 1.5:1 | 6:1 |
| 54 | 6:1 | 1.5:1 | 7:1 |

FIGURE 2. ELECTRICAL PERFORMANCE (RESISTANCE AND SPEED)

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high-density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal vapor content can be carefully controlled during production.

Harris Semiconductor Leadless Chip Carriers in both Ceramic and Epoxy provide reliable, high density, high performance packaging options for today's systems.

Consult the factory or your Harris sales representative for pricing and availability.