Cyber9388

High Performance
High Integration
Flat Panel Controller

Technical Reference Manual

Revision 1.0

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Table of Contents

1. INTRODUCTION 1-1
1.1. SCOPE 1
1.2. CYBER9388 DESCRIPTION 1-1
2. FEATURES 2-1
2.1. FEATURE OVERVIEW 2-1
2.2. SYSTEM FEATURES 2-1
2.2.1 High Performance 64-bit 2D GUI 2-1
2.2.2 Highly Integrated RAMDAC & Clock Synthesizer 2-2
2.2.3 TrueVideo® Processor 2-2
2.2.4 Motion Video Capture/Overlay Support 2-2
2.2.5 Embedded SDRAM 2-3
2.2.6 Hi-Res and Hi-Ref Display Support 2-3
2.2.7 Advanced Power Management 2-3
2.2.8 CRT Power Management (VESA DPMS) 2-4
2.2.9 Standard Bus Interface with Bus Mastering Support 2-4
2.2.10 Complete Hardware Compatibility 2-4
3. ARCHITECTURAL & FUNCTIONAL DESCRIPTION 3-1
3.1. CYBER9388 COMPONENTS 3-1
3.2 2D GRAPHICS DRAWING ENGINE 3-1
3.2.1 2D GUI Functions 3-2
3.3. HOST INTERFACE 3-3
3.3.1 Command Queue 3-3
3.4. TRUEVIDEO® PROCESSOR 3-3
3.4.1 Minifier™ 3-4
3.4.2 Bilinear H/V Interpolated Scaling 3-4
3.4.3 Zoom Block 3-4
3.4.4 Edge Recovery 3-4
3.4.5 Anti-Tearing 3-4
3.4.6 DirectDraw™ 3-4
3.4.7 Horizontal Filter 3-5
3.4.8 Video H/V Scale and Color Space Conversion 3-5
3.4.9 Dual-Aperture 3-5
3.4.10 Dual Video Window for Video Conference 3-5
3.4.11 Dual-view and Simultaneous Display 3-5
3.5. SEQUENCER 3-5
3.6. TRIPLE CLOCK SYNTHESIZER 3-5
3.7. VGA CONTROLLER 3-9
3.7.1 Display Controller 3-9
3.7.2 VGA Graphics Controller 3-9
3.7.3 Attribute Controller 3-9
3.8. EMBEDDED SDRAM 3-9

Table of Contents (Cont'd)

3.9. DISPLAY INTERFACE 3-9
3.9.1 LUT/DAC *3-9*
3.9.2 LCD Flat Panel *3-10*
3.9.3 Flicker-free NTSC/PAL TV Output *3-10*
3.10. ADVANCED POWER MANAGEMENT 3-10
3.10.1 Power States *3-10*
3.10.2 Activating and Deactivating Power Modes *3-11*
3.10.3 Chip Power Sequence *3-11*
3.10.4 Panel Power Sequencing *3-12*
3.10.5 CRT Power Sequencing *3-12*
3.11. POWER-UP CONFIGURATION 3-13
3.12. TIMER MODES 3-13
3.13. TESTABILITY 3-13
3.13.1 Observation of Internal VCLK and MCLK *3-13*
3.13.2 DAC Testing *3-13*
3.13.3 Pin Scan Testing *3-13*
3.13.4 Signature Analysis *3-13*
3.14 EEPROM/DDC SUPPORT 3-14
3.15 ZV/CAPTURE/VMI PORT 3-15
3.16 CHIP BLOCK DIAGRAM 3-16
4. ELECTRICAL SPECIFICATIONS 4-1
4.1. ABSOLUTE MAXIMUM RATINGS 4-1
4.2. RECOMMENDED OPERATING CONDITIONS 4-1
4.3. DC SPECIFICATIONS 4-1
4.4. AC SPECIFICATIONS 4-2
4.4.1 Clock and Reset Timing *4-2*
4.4.2 DDC INTERFACE / EEPROM Timing *4-3*
4.4.3 PCI Bus Timing *4-4*
4.4.4 Vertical Timing *4-5*
4.4.5 Horizontal Timing *4-7*
4.4.6 PCI ROM BIOS Access Timing *4-9*
4.4.7 Panel Power Sequencing Timing *4-10*
4.4.8 Flat Panel Interface Timing *4-11*
4.4.9 VMI Host port timing *4-12*
4.4.10 TV Composite SYNC timing *4-13*
5. CONFIGURATION TABLE 5-1
5.1. VIDEO MODES 5-1
5.2. STANDARD MODES SUPPORTED FOR TV OUTPUT 5-8
5.3. EXTENDE MODES SUPPORTED FOR TV OUTPUT 5-9
6. PIN DESCRIPTION 6-1
6.1. SIGNALS 6-1

Table of Contents (Cont'd)

6.2 PIN ASSIGNMENT 6-5
6.3. PANEL SIGNAL MAPPING 6-13
6.4. CYBER9388 BGA DIAGRAM OF PIN (GRID) ASSIGNMENT OF 6-14
6.5. CYBER9388 BGA PACKAGE PHYSICAL DIMENSIONS 6-15
7. SYSTEM DESIGN 7-1
7.1. POWER UP CONFIGURATION 7-1
7.1.1 PCI Bus Interface 7-2
7.1.2 TFT Panel (Single Pixel/Clk) Interface (Direct Drive) 7-3
7.1.3 TFT Panel (Double Pixel/Clk) Interface 7-4
7.1.4 STN Panel Interface - 16 Bit Color Data 7-5
7.1.5 CRT/TV Interface 7-6
7.2. LAYOUT CONSIDERATIONS 7-7
7.2.1 Clock Synthesizer 7-7
7.2.2 Analog and Digital GND Separation 7-7
7.2.3 Trace Size and Restrictions 7-9
7.2.4 Signal Routing 7-10
7.3. FCC COMPLIANCE GUIDE 7-11
7.3.1 Layout Issues/Component Placement 7-11
7.4. SCHEMATICS EXAMPLES (PCI BUS) 7-12
7.4.1 Special Layout Considerations 7-12
7.4.2 PCI Bus Schematic Example 7-14

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1. Introduction

The information contained in this Technical Reference Manual is intended to give in-depth technical assistance to a design engineer in the development of interface boards utilizing the Trident Cyber9388 Multimedia 2D Flat Panel Controller chip.

This document includes a technically detailed, yet comprehensive reference guide to all aspects of the design specifications and considerations in the development cycle.

The Cyber9388 is described in the following sections:

- Product Information
- Architectural and functional descriptions
- Electrical Specifications
- Configuration (Mode Tables)
- Pin diagrams and descriptions
- Board level design and feature options
- Sample Schematics

1.1 Scope

This book is an excellent reference to guide the design engineer in applications development.

This document provides the user with sufficient information for:

- Designing and laying out PCI Bus interface cards for the Cyber9388
- Configuring the Cyber9388
- Detailed pin signal information and all other technical data required for success with the Cyber9388.

1.2 Cyber9388 Description

The Cyber9388 is Trident's newest release in the Cyber family of flat panel display controller chips. With 2MB embedded SDRAM, the Cyber9388 is a highly integrated display control device which incorporates a 64-bit 2D graphic engine and video accelerator with the advanced TV-output capability. It provides a flexible and high performance solution for graphics and video playback acceleration for various color depth and resolution modes.

It supports a video capture port to import a captured live video stream or MPEG 1 and MPEG 2 decompressed video streams to be overlaid with the graphics stream on mixed color depth displays. In supporting dual live videos, the Cyber9388 offers independent dual video windows that are ready for the video conferencing and are able to be scaled linearly. The Cyber9388 is able to provide different refresh rates for LCD and CRT/TV for the dual-view display mode. A sophisticated on-chip flicker reduction processor in the Cyber9388 converts a graphics image to NTSC or PAL signals for TV output. Integrating the programmable phase locked loop with high speed LUT DACs, the Cyber9388 is a true price/performance solution for modern multimedia based entertainment mobile PCs.

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2. Features

This section describes the architecture and system level features of the Cyber9388.

2.1 Feature Overview

The Cyber9388 with 2MB embedded SDRAM is a fully integrated LCD, CRT, and TV 64-bit, 2D Multimedia Flat Panel Controller for PCI systems. It is a high performance chip, offering high speed image processing in full compliance and compatibility with IBM VGA and VESA extended VGA. The Cyber9388 has a 32-bit PCI v2.1 local bus interface with Bus Mastering capability.

The Cyber9388's highly innovative design dramatically improves GUI functions and significantly promotes overall system operation. The Cyber9388, equipped with a single-cycle 2D GUI engine, pipelines video and graphics processing architecture in hardware, providing very fast 2D hardware acceleration.

Higher performance is achievable with higher bandwidths due to the high speed cycle time available with the 2MB embedded SDRAM. Integrating SDRAM with the high performance graphics engine allows the RAMDAC™ to run up to 170Mhz.

Cyber9388's LCD interface provides a flexible environment to manipulate the LCD control. It supports panel interfaces up to 1280x1024 SXGA TFT panels with 12, 18, 24, 12+12, or 18+18-bits or 1024x768 XGA DSTN panels with 16 or 24-bits. In addition to the same simultaneous display supported by the other members of the Cyber LCD controller family, the Cyber9388 is able to provide independent refresh rates for LCD+CRT or LCD+TV multi-view.

In addition to low power consumption, Cyber9388's Advanced Power Management (APM) extends power management capabilities to provide flexible power saving design solutions.

The Cyber9388 supports a 16-bit Zoom Video (ZV) Port that allows direct connection to a PC card. It permits the PC card to write video data (YUV) directly to the VGA chip and overlaid video windows with graphic data on the frame buffer without increasing the data loading on the PCI bus.

To meet the requirements of a PC97 graphics adapter and a multimedia PC, the Cyber9388 supports the planar video format for MPEG-1 and MPEG-2. Also, the dual video playback is capable of overlaying two windows for video conferencing and multimedia displays. The ClearTV™ technology performs "flicker removal" and "scaling" functions that remove the artifacts when VGA signals are transformed to a TV monitor or when the data is sent to a recording device, such as a VCR.

Additionally, the Cyber9388 has such advanced features as: Color Space Conversion (CSC), TrueVideo® scaling, dual video windows, multil-view display, Video Module Interface (VMI), interacts protocol Vertical Blanking Interleave (VBI), an 8-bit True Color DAC, and triple clock synthesizers to allow it to perform at peak levels.

2.2 System Features

The Cyber9388's main system features include:

- High Performance 64-bit GUI
- Highly Integrated RAMDAC and Triple Clock Synthesizer
- Full Feature High Performance 2D Engine
- Advanced Flat Panel Image Control
- Independent Refresh Rates for Multiple View and Simultaneous Displays of LCD+CRT or LCD+TV
- Dual Video Windows for Videoconferencing
- TrueVideo® Processor
- DirectDraw™ and DirectVideo™ Hardware Support
- Versatile Motion Video Capture/Overlay Support
- 2MB Embedded SDRAM
- ClearTV™ for Flicker-Free TV Display
- Advanced Mobile Power Management
- CRT Power Management (VESA DPMS)
- Standard Bus Interface with Bus Mastering Support
- PC97 Hardware Support

2.2.1 High Performance 64-bit 2D GUI

The 64-bit graphics engine of the Cyber9388 significantly boosts graphics performance through specialized hardware that accelerates the most frequently used GUI operations and matches the high-speed requirements of CPUs. Functions directly supported in hardware include: BitBLTs, image and text transfer, line draw, short stroke vector draw, rectangle fills, and clipping. The graphics engine supports 256 Raster Operations (ROPs) for up to 32-bit graphic modes. The ROP3 Processor in the Cyber9388 is able to perform Boolean functions, which allow many additional operations, including color expansion alignment and pattern enhancement.

The graphics engine also features linear display memory addressing (up to 4GB of memory space), accelerated color expansion modes for graphics text procession, and memory-mapped I/O registers on the graphics engine for faster access time. Graphic functions are optimized by a 64 bit internal data bus and a four-color hardware cursor/pop-up icon operation up to a 128x128x2 pixel image, which off-loads the CPU.

The hardware cursor mechanism can also be used to display patterns stored in the system memory. This pop-up icon is very useful to instantly display user friendly information through simple hot key operations. This advanced functional combination allows significant performance increases over standard Super VGA designs, providing outstanding graphics acceleration for GUIs such as Microsoft's Windows 95™.

2.2.2 Highly Integrated RAMDAC & Clock Synthesizer

The highly integrated design of the Cyber9388 offers a "no TTL" solution for cost-effective, high performance multimedia subsystem designs for the IBM® PC and compatible notebooks. The embedded SDRAM provides faster data transfer rates for improved system throughput. The highly integrated RAMDAC™ and Clock Synthesizer in the Cyber9388 provides an easy access to the interface and saves spaces.

The integrated triple frequency synthesizer provides a 100 MHz MCLK which supports the high-speed SDRAM and one 170 MHz VCLK, which support refresh rates up to 1280x1024 at 85 Hz.

Video processor features include: on-chip hardware Color Space Conversion (CSC) for faster data conversion "on-the-fly", Horizontal/Vertical (H/V) scaling with interpolation, an edge recovery algorithm, gamma correction, and overlay control with different color depths from graphics. The Cyber9388 also includes a fully integrated GUI accelerator, read cache, and a command FIFO that optimizes memory bandwidth and maximizes graphics performance.

2.2.3 TrueVideo® Processor

The Cyber9388 can provide dual video windows, which display different images from different video sources (from the PCI bus and from the capture port) on the same screen. The video image is stored in the off-screen memory and is retrieved by the Video Display Processing block for TrueVideo® processing.

With the help of DirectDraw™ acceleration for sprites, page flipping, double buffering, and color keying, TrueVideo® processing is performed by utilizing Trident's proprietary edge recovery algorithm for sharper line visibility, de-interlacing, anti-tearing, multitap horizontal filtering, dithering, and scaling operations with bilinear interpolation in both horizontal and vertical directions. The linear scaling permits zooming in/out to any size without restrictions.

In addition, the on-chip hardware Color Space Conversion (CSC) accelerates conversion for 16 bit YUV pixels into linear, true color, 24 bit RGB pixels on the fly. The additional X and Y minifiers are capable of shrinking the video images to any linear fractions; this saves bus bandwidth and memory space. The YUV planar of the Cyber9388 supports a YUV 420 format that can remove redundant video stream decoding procedures. The load of the CPU is reduced while performing SW MPEG or SW videoconferencing. The color and luminance control provided by the Cyber9388 offers color compensations to prevent color distortion for display devices such as a CRT, LCD, or TV with a Gamma correction and hue adjustment control.

The Videoconferencing feature allows remote and local video images to be displayed simultaneously on the same screen. With the support of independent VCLKs for independent refresh rates, the video processor is able to provide multiple view and simultaneous display. This function is also capable of sending local CCD data to the PCI bus via the Bus-Mastering feature.

2.2.4 Motion Video Capture/Overlay Support

The Cyber9388 has a built-in video capture port and advanced hardware interface logic allowing it to be connected directly to many MPEG and video decoders, such as: the C-Cube CL450/480, SGS 3400/3500, Philips 7110/1, and Brooktree BT819/817. The Video Module Interface (VMI) allows for MPEG compressed data to be transferred to the MPEG decoder through the Cyber9388. The decompressed MPEG data is then transferred back to the graphics controller through the VMI port for real-time display in a window.

A new industry standard is being set for transmission of non-video data over a TV broadcast signal during the dead time called vertical blanking. This technology is also referred to as Intercast. The Cyber9388 has the ability to take the entire video stream over the video port, sending the visible video stream to the display memory for display in a window, stripping the VBI data from the stream, and then sending this data to the CPU for processing using PCI Bus Mastering.

The Cyber9388 provides a Zoom Video (ZV) port aperture, which connects directly to a PC card. This feature allows the PC card to write directly to the Cyber9388 with video data (YUV) which is overlaid in the video window onto graphic data in the frame buffer without increasing the data transfer loading on the PCI bus.

The Cyber9388 features a Dual Video Overlay. The Video inputs can come from either the PCI bus or the Video Capture Port. Device drivers can use the Cyber9388's PCI Bus Mastering capability to send graphics or decompressed video images to local display memory or to receive live video images from an external video source such as a TV tuner, VCR, or camera. The Bus Mastering

can improve the whole system's operation by off-loading CPU tasking on the data transfer to or from the Cyber9388.

2.2.5 Embedded SDRAM

With 2MB embedded SDRAM, optimized performance can be achieved using programmable timing. The display queue has been increased commensurate with the increase in available bandwidth, optimizing efficiency for the graphic controller. The SDRAM also provides abundant memory bandwidth for a high resolution display and video playback.

SDRAM minimizes chip count, which saves board space and reduces power consumption.

The Cyber9388 also supports 2 MB of external SGRAM, which expands the total display memory configuration to 4MB.

2.2.6 Hi-Res and Hi-Ref Display Support

The Cyber9388 features versatile display support in the following areas: flat panels, CRTs, TVs, and application display software drivers.

2.2.6.1 Advanced Flat Panel Image Control

The Cyber9388 supports TFT or DSTN panels without external glue logic. Full functions are ready for panel interfacing with 12/18/24/36-bit/analog TFT panels or (12+12)/(18+18) double pixel/clk TFTs panels up to 1280x1024-64K color or 16/24-bit DSTN panels up to 1024x768-16M colors with a frame buffer size up to 4M (SDRAM).

The Cyber9388 supports expansion of VGA data for all supported types and resolutions. The Cyber9388 utilizes external LVDS or PanelLink™ technology that enables low voltage, high-speed, low EMI, serial, DC-balanced, differential data transmission. The Cyber9388 employs leading-edge techniques to reduce EMI and to provide scalability and support for notebook LCD displays.

2.2.6.2 Multiple view/Simultaneous Display and Dual Video Windows for Videoconferencing

The Cyber9388 is capable of providing multiple view and simultaneous displays in 24-bit color with mixed video/graphics on a flat panel and a CRT or on a flat panel and a TV. This feature is an optimal solution for users requiring different images on both displays. The Cyber9388 allows the displays shown on a panel and a CRT or TV at different refresh rates, different resolutions, and different color depth. Therefore, the display on a CRT will not be degraded to accommodate the lower refresh rate of a LCD panel.

The Cyber9388 display enhancements dramatically improve CRT resolution, providing sharp images. These enhancements include support of non-interlaced 1280x1024x64K, 1024x768x16M, 800x600x16M, and 640x480x16M colors for "full spectrum" color. Extended text modes of 80 or 132 columns by 25, 30, 43, or 60 rows provide an extended graphics area frequently used in many spreadsheet and database applications. In addition, extended graphics and text modes are supported by software drivers that provide a "ready-to-go" solution, minimizing the need for additional driver developments.

For videoconferencing, the Cyber9388 supports two independent scalers and CSCs for separate local and remote video window control.

A virtual screen can be created with the Cyber9388. When this function is enabled, a selected portion of a large image can be shown on a smaller display. The image can also be moved either up or down across the whole screen.

The Cyber9388 is able to automatically detect DDC monitors with I²C signaling.

2.2.6.3 ClearTV™ Output

The Cyber9388 supports a high quality, flicker-free TV display to either the NTSC or PAL standard. To convert the non-interlaced VGA data to an interlaced TV display, the Cyber9388 employs a 3-line flicker-free TV buffer for flicker reduction by smoothing adjacent lines. This produces a very stable view on a TV screen. ClearTV™ provides the best TV quality in the industry. Composite synchronization (Csync), sub-carrier, and I²C signals are provided for connection to standard off-the-shelf TV encoder parts, such as the AD722/4™ and Sony CXA™ series for standard home TV applications.
In order to match different display modes between VGA and TV standards, the Cyber9388 provides overscan, underscan, and automatic aspect adjustment functions or utilities to allow for identical data to be shown on a TV and a LCD panel simultaneously or individually

2.2.7 Advanced Power Management

The Cyber9388 provides flexible and extensive mobile power management capabilities. The Cyber9388 employs 3.3V voltage operation with independent power planes for Core and Analog, Host, Memory, CRT, and Panel interface. The on-chip LUT/DAC, video clock (VCLK) and memory clock (MCLK), and external crystal input can be powered down through register controls or pins. Power down states include ready, standby, and suspend. Each power state can be activated by hardware pins, hardware timers, or software control bits. Clocks to major functional blocks, such as GE, video, TV-out, etc., can be turned on/off independently.

2.2.8 CRT Power Management (VESA DPMS)

The Cyber9388 conforms to the standard power management schemes defined by VESA for CRT. The Cyber9388 supports four states of VESA Display Power Management Signaling (DPMS), which decreases monitor power consumption after timeout periods. VESA DPMS power down states (ready, standby, suspend, and off) specify HSYNC and VSYNC signals to control the monitor power down state.

2.2.9 Standard Bus Interface with Bus Mastering Support

A simple Bus Interface Unit (BIU) provides a low cost, single chip solution for IBM® PC or compatibles on PCI 2.1 Bus systems speeds up to 66 MHz with Bus Mastering capability. The capability of Bus Mastering gives the Cyber9388 access to the PCI bus, allowing the transfer of data from the Cyber chip to the other devices on the same PCI bus. For instance, the local CCD captured data can be sent to the PCI bus for compression and delivery to a remote site. The glueless logic for both the system bus and display memory interface, and a two wire communication interface allows direct support of VESA DDC, DPMS, VAFC standards for up to 8 GPIO for DDC, I²C. The Video Module Interface (VMI) is also supported for video devices such as MPEG1 and MPEG2.

The zero-wait state host write buffer, read cache, and memory mapped I/O increase operating speeds and contribute to peak performance levels. Graphics system throughput is further enhanced by a command FIFO, allowing maximum bus transfer speed for applications, such as Windows™ or AutoCAD™ that directly access video memory.

2.2.10 Complete Hardware Compatibility

The Cyber9388 is fully compliant with the PCI 2.1 Bus specifications and also supports VESA DDC and VAFC standards. The Cyber9388 is 100% IBM® VGA compatible on the BIOS and Drivers, allowing full compatibility with virtually any VGA application software. In addition, the Cyber9388 provides an HW support to DirectDraw™, offering high speed game graphics on Windows 95™. The Cyber9388 meets the requirements of PC97 as well, supporting a unique ID for each customer and a unique ID for each model.

3. Architectural & Functional Description

This section describes the architectural & functional characteristics of the Cyber9388. The following topics are discussed:

3.1. Cyber9388 Components
3.2. 2D Graphics Drawing Engine
3.3. Host Interface
3.4. TrueVideo® Processor
3.5. Sequencer
3.6. Triple Clock Synthesizer
3.7. VGA Controller
3.8. Embedded SDRAM
3.9. Display Interface
3.10. Advanced Power Management
3.11. Power-Up Configuration
3.12. Timer Modes
3.13. Testability
3.14. EEPROM/DDC Support
3.15. ZV/Capture/VMI Port

This section describes the architectural & functional characteristics of the Cyber9388.

3.1 Cyber9388 Components

The Cyber9388 is composed of the major components illustrated in the block diagram (see Figure 3-1). These components generate video output and timing for video memory and the monitor. This chapter provides a summary of each component.

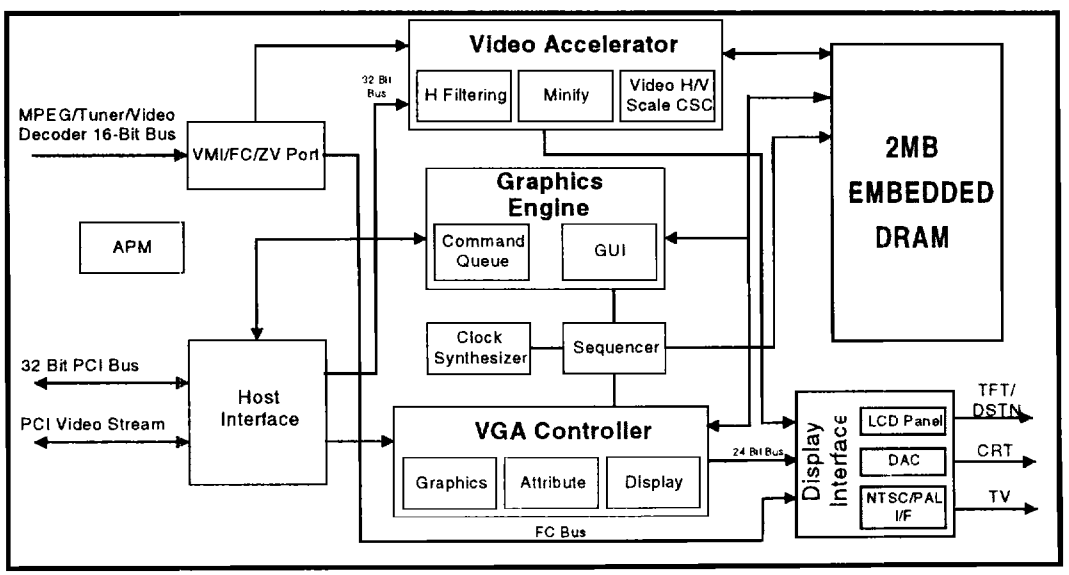

Figure 3-1. Cyber9388 Block Diagram

3.2 2D Graphics Drawing Engine

The Cyber9388 contains a revolutionary single-cycle, integrated 2D graphics drawing engine (GDE) for accelerating popular GUI environments, such as Microsoft Windows 95™ and Windows NT™ 4.0, for highly interactive entertainment applications. This enhanced graphics engine is the key to high performance. All important functions, which dramatically increase 2D device driver graphics performance, are integrated in it. The following are its key elements:

Higher memory bandwidth: This is achieved with the embedded DRAM due to a high speed cycle time and a wider data bus. The effective page cycle can be even faster in SDRAM because the memory clock can run at a higher frequency. The GDE is designed such that the data generation rate is balanced with the memory data transfer rate.

Concurrence between hardware and software: Deep FIFOs are provided to buffer data so that the controller can handle the next batch of data as quickly as the CPU transfers data to it.

3.2.1 2D GUI Functions

Although the graphics engine is thoroughly unified, for convenience the Cyber9388's functions may be divided into GUI, DirectDraw™, and Multimedia categories:

- BitBLTs
- Solid Area Fills
- Patterned Area Fills
- Text Transfers
- 256 RasterOPs
- Mono->Color Expansion
- Polygon Fill, solid or patterned
- Line Drawing
- Hardware Clipping
- Hardware Cursor
- Hardware Pup-up Icon

3.2.1.1 BitBLT's

The BitBLT is the single most important acceleration function for windowed GUI environments. A BitBLT is simply the movement of a block of data from one place to another, taking into account the special requirements and arrangements of the graphics memory. This function is utilized every time, e.g., a window is moved, in which case the BitBLT is a simple Pixel Block Transfer. More complicated cases may occur where some transformation of the source data is to occur, such as in a Color Expanded Block Transfer, where each monochromatic bit in the source is expanded to the color in the foreground or background register before being written to the display. Various operations and functions may also be used during and combined with BLTs, such as RasterOPs and Patterns (see below). Also, the source can simply be ignored and replaced with a value from the foreground (or background) register or expanded from the pattern register to the foreground (or background) color to cover a large area.

3.2.1.2 Text Transfer

Text Transfers are a special case of Color Expanded BLTs specifically tuned for high-speed transfers of 8-bit wide monochromatic data (i.e. text) from system memory or the frame buffer to the display. For this special case, the alignment is to the byte boundaries, ensuring that no separate bits locate in a different byte. Each bit of the source is then expanded to the foreground or background color.

3.2.1.3 Solid Area Fills

When a solid rectangular background is required, such as the white area in a window, the Cyber9388 can fill it with a color from the foreground color register.

3.2.1.4 Patterned Area Fills

The Cyber9388 is also able to fill a rectangular area with a repeated pattern from the pattern register for patterned desktops or window backgrounds.

3.2.1.5 256 RasterOPs

Raster Operations are logical bitwise operations involving a source, a destination, and a pattern. The source and destination are normally the source and destination rectangles for a BitBLT, while the pattern is held in a register. The Cyber9388 has a large 64x32 pattern register to avoid excessive repeated loading of the pattern register.

3.2.1.6 Polygon Fills

When areas can be described conveniently as polygons (objects with multiple sides), the Cyber9388's graphics engine can fill them with a solid color or a pattern.

3.2.1.7 Line Draws

When an application needs to draw a line between two points, the Cyber9388 will accelerate this function. The line can be solid or patterned and can have RasterOPs applied to it while it is being drawn. Aside from graphical drafting applications, line drawing is also important to GUI elements, such as fine window borders, menu dividers, etc.

3.2.1.8 Hardware Clipping

It is sometimes very computationally expensive for an application to determine whether or not an object to be drawn will be entirely inside a rectangular area. The clipping functions are useful to prevent the computer from calculating portions of the image that extends outside the viewable window. When an image is panned or moved in a window, the display controller is able to generate the lines or images that come into view and delete or clip those that move out of view. Therefore, the clipping functions are very efficient to provide fast updates by the display controller.

3.2.1.9 Hardware Cursor

The 32x32 or 64x64 hardware cursor exists on a bit-plane independent of the graphics display. This allows the cursor to be used without regard to the action going on the screen and eliminates the flickering caused by the alternating erasure and redrawing of a software cursor on the same plane as the graphics data. The cursor is stored in a 2bpp format in the off-screen area, allowing pixels of four

different values to comprise the cursor: white, black, screen color, and inverted screen color.

3.2.1.10 Hardware Pop-up Icon

A four-color pop-up icon supports a user defined pattern of 128x128x2, 64x64x2 or 32x32x2 pixel image with simple hot-key operations. The hardware pop-up icon pattern is stored in a non-visible portion of display memory and its area is separated from hardware cursor area without driver conflict.

3.3 Host Interface

The Cyber9388 can interface with the 33/66 MHz PCI local bus. The host interface handles the PCI 2.1 compliant interface protocol, performs proper signal synchronization from the CPU clock domain to the MCLK domain and provides post write data buffering. Because of this data buffering, the Cyber9388 can realize true burst mode operation in the PCI configuration, i.e., every 32 bit data transfer per CPU clock cycle at its peak transfer rate. It also translates either linear addressing or bank addressing to internal DRAM addressing. In addition, it decodes memory mapped I/O or I/O space into its internal locations. Through I/O, the HI can also communicate with video or other devices that support I²C protocol. When the BIOS is enabled in the PCI configuration, the HI will deal with the ROM timing. The Cyber9388 fully supports the PCI configuration space within the HI block.

The Cyber9388 can translate either linear or bank addressing to the internal DRAM addressing. The HI is able to communicate with video or other devices that support I²C protocol. It supports the scatter and gather mechanism. This feature will be useful for video conferencing applications, which require two live video windows. Dual read/write apertures allow simultaneous access to display memory graphics and video areas that improve the data transfer flow dramatically.

With the bus master capabilities in the Cyber9388, device drivers can use bus master function to send graphics or decompressed video images to the local display memory or to receive live video images from an external video source such as a TV-tuner, VCR, or camera.

Linear addressing can go up to 4MB of display memory. The base address for the linear addressing windows may be set anywhere up to 4 GB of linear memory space. The Cyber9388 allows a linear addressing window and the standard VGA memory space to be active at the same time. This allows greater flexibility in adapting non-linear addressed drivers to the linear addressing environment.

The Cyber9388 supports a dual linear PCI aperture feature. One aperture is normally for graphics and the other one is for Video or DirectDraw™. By separating graphics from video, graphics and video streams from the PCI bus can be simultaneously be sent to or obtained from the frame buffer.

Using the PCI Bus Mastering capability in the Cyber9388, a device driver can send graphics or decompressed video images to local display memory or receive live video images from external video sources such as a TV-tuner, VCR, or camera. The Bus Mastering improves the whole system operation parallelism by off-loading the CPU on the data transfer to or from the Cyber9388 subsystem, letting the CPU do other tasks, such as video compression or decompression, and PC game logic. PCI palette snooping is handled within HI. Two possible snooping mechanisms are supported. One is due to a PCI retry mechanism and the other is due to a bridge master abort mechanism. Which mechanism to select from is automatically determined by the video BIOS during power up.

The Cyber9388 also supports the VMI interface. Via this interface, some popular commercial MPEG decoders can communicate directly with the Cyber9388 without any glue logic. This is an important feature when the MPEG device is integrated with the Cyber9388 on the same PCI card. According to PCI specifications, there will be only one interface per card. The MPEG decoder will communicate with the host via the Cyber9388 for compressed video data and register setup.

3.3.1 Command Queue

The Command Queue enhances memory write performance. The CPU write data can be loaded into the Command Queue, eliminating the CPU's need to wait while the memory is busy with other tasks. When the memory bus is available, data is written into the memory from the Command Queue.

3.4 TrueVideo® Processor

The TrueVideo® Processor is the essential part of the Cyber9388. It accepts the data stream with YUV 4:2:2/4:1:1 or RGB formats. The block fetches the data from the off-screen memory and performs bilinearly interpolated scaling in both horizontal and vertical directions with arbitrary scaling. In addition, it converts the YUV pixels into linear RGB pixels on-the-fly. Video overlay with different graphic data color depths is supported seamlessly. This allows the highest quality overlay of graphics data on top of video data, such as in pull-down menus. The DirectDraw™ acceleration increases the performance of the software playback.

3.4.1 Minifier™

With the integration of a programmable luminance interpolating filter and an independent linear X and Y

minifier, the Cyber9388 accepts YUV 4:2:2 or YUV 4:1:1. The video image can be smoothed through a programmable multi-tap filter to reduce the jig-jag effect after minification. The video data can be minified to any linear fraction to save the bus bandwidth or memory space and is written into the off-screen memory. Video information can also be minified before sending it to the frame buffer. Minify can be performed in both horizontal and vertical directions. The horizontal and vertical minify factor, HMF and VMF, are defined as follows:

HMF = Hf/Hs x 1024 - 1

VMF = Vf/Vs x 1024 - 1

HMF and VMF are described by registers 3X5.[B3:B0]. In order to perform minify, the frame buffer horizontal and vertical destination count needs to be defined by the registers. Filtering is used in conjunction with minify. When minify is disabled, filtering is not recommended (It can still be enabled, but it will generate a fuzzy video image.). During the minify process, some pixels or lines will be dropped. In this case, filtering is needed to send the dropped information to the undropped pixels to preserve a better video image.

3.4.2 Bilinear H/V Interpolated Scaling

Three types of vertical scaling, duplication, interpolation, and edge recovery interpolation, can be performed by programming the register 3X5.8F[5:4]. When bit 4 is 1, lines are duplicated. When bit 4 is 0, vertical interpolation using the averaging method is enabled. When both bits 5 and 4 are enabled, the Trident's proprietary edge recovery interpolation can be enabled. In this case, when bit 5 is 0, edge recovery is disabled. When bit 5 is 1, edge recovery is enabled. Similarly, the method of horizontal interpolation can be determined by 3X5.8F.3. When bit 3 is 0, the pixel is duplicated. When bit 3 is 1, the pixel is interpolated by averaging adjacent pixels.

3.4.3 Zoom Block

Zooming is performed on the display path to save memory bandwidth, as compared with other methods, which perform zooming before the data is sent to memory. Zooming can be performed in both horizontal and vertical directions. The horizontal and vertical zoom factor, HZF and VZF, are described as follows:

HZF = Hd/Hf; VZF = Vd/Vf

HZF and HZF are defined in registers 3X5.81-80 and 3X5.83-82, respectively. These two factors are 14 bits long. The lower 10 bits define the fraction part multiplied by 1024 and the upper 4 bits define the integer part minus one. The maximum number of zooming in each direction is 16. Interpolation can only be performed for zooming factors less than or equal to 4. Zooming factors greater than four can only be duplicated.

3.4.4 Edge Recovery

The hardware edge recovery mechanism reduces the zigzag effect due to the scaling up of oblique lines. For each pixel, the mechanism analyzes which interpolation pixel pairs to sharpen, thereby smoothing those edges.

3.4.5 Anti-tearing

The hardware anti-tear mechanism prevents the tearing effect due to the frame buffer update and eases the burden of the software to flip the page. It is accomplished by removing the visual artifact, which occurs when the display (read) data line and the capture (write) data line cross. The display would then show data from frame "N" on one part and from "N+1" on the next. To prevent this, the Cyber9388 allocates two capture surfaces (off-screen memory areas). While frame "N+1" is being written to one surface, it reads frame "N" from the other surface.

3.4.6 DirectDraw™

The Cyber9388 supports DirectDraw™, an interface for the Microsoft Windows® operating system, which provides direct access to display devices while maintaining compatibility with Windows GDI and enables world class graphics on a Windows 95-class PC. It provides access to the following display device-dependent benefits:

- Support for double-buffered and page flipping graphics
- Access to and control of the video cards BLTer
- Improved video playback quality through access to YUV color formats
- Improved graphics and video quality through access to image-stretching hardware
- Simultaneous access to standard and enhanced display device memory areas

The following sections describe the Cyber9388 featured functions:

3.4.6.1 Source/Destination Color-keying

Both source and destination color keying are used to mask out pixels that will not be overwritten. Envision, for example, that a destination is an onscreen background scene (onscreen area in the frame buffer) which is being displayed, and a source, which is a graphics figure being stored in the off-screen buffer area, is to be overlaid on this background scene. First of all, the source or graphics figure is stored inside a rectangular area using a background color key (the color of all the rectangular area except for the graphics figure itself). During the BLT process, the

graphics figure (including the color keyed rectangle) is retrieved from the off-screen buffer area by the graphics engine and then sent to the onscreen buffer area (background scene). The color key register is programmed to be the background scene color. Any onscreen pixel that matches the color key register will not be overwritten, except for the graphics figure area itself. Thus, after the BLT process, only the graphics figure area is overlaid on the background scene.

3.4.6.2 Flipping Surfaces

DirectDraw™ has extended flipping surfaces to encompass more than page flipping and more than visible surface flipping. Any surface can now be constructed as a flipping surface. This has many advantages over the traditional, limited scope of page flipping.

3.4.7 Horizontal Filter

Video pixel data, after being converted to the internal format, is sent to the horizontal filtering block. The horizontal filtering can be one of several formats: bypass, 2, 3, 5, and 9 taps. The combined effect of the video pixel is to weigh that particular pixel data according to the adjacent video pixel data.

3.4.8 Video H/V Scale and Color Space Conversion

The Video Display Engine fetches the YUV 4:2:2 or RGB8 data from the off-screen memory and scales up with bi-linear interpolation in both horizontal and vertical directions. In addition, the on-chip hardware Color Space Conversion (CSC) accelerates conversions for the 16-bit YUV 4:2:2 data stream into the true color RGB24 data stream and muxed with the graphic data. The graphic data and video data can be handled smoothly in different color depths with the color key support.

Color Space Conversion hardware can be placed after VAFC input or before Graphics Engine. It accepts YUV422 or YUV411 as input and converts them to RGB888 for further processing. The input range of YUV data can be either CCIR601 compatible (16-235) or normalized (0-255), depending on the source format. For normalized YUV input, the conversion equation is:

$$R = Y + 1.402 * U$$
$$G = Y - 0.71414 * U - 0.34414 * V$$
$$B = Y + 1.772 * V$$

3.4.9 Dual-Aperture

The Cyber9388 supports dual PCI apertures. In the configuration space, there are two separate PCI memory base registers pointing to different logic starting addresses. Video data will be mapped to the same physical address space. Providing dual apertures in the PCI bus configuration allows concurrent processing for graphics and video data streams. Each will have a different logic address and each will be sent to its own write buffer. The video aperture is provided via a separate PCI memory base register which is used to generate DEVSEL# to claim the PCI bus cycle. The PCI offset address is simply discarded. The physical memory address is determined by the internal register.

3.4.10 Dual Video Window for Videoconferencing

The Cyber9388 allows remote and local video images to be displayed simultaneously on the same screen. The different video sources can be accepted through the PCI Bus and the capture port at the same time. Performing YUV Planar, the Cyber9388 supports YUV 420 which removes the redundant video stream decoding procedures and reduces the loads for the CPU while processing SW MPEGs or SW videoconferencing.

3.4.11 Multiple View and Simultaneous Display

The Cyber9388 supports multiple view and simultaneous display in 24-bit color depth with mixed video/graphics on a flat panel and CRT or on a flat panel and TV. The independent refresh rates are able to fully utilize the flat panel, CRT, and TV display qualities.

3.5 Sequencer

The Sequencer controls access to the display memory and provides basic memory timing for the SDRAM interface and a character clock for the CRTC to control the regenerative memory fetch. The Sequencer controls and coordinates overall Cyber9388 operation. The Sequencer prioritizes access for memory refresh, display refresh, Graphics Drawing Engine (GDE), and CPU accesses. The available display memory bandwidth of the embedded SDRAM is as twice as that of an EDO DRAM at the same clock rate. Data is output to the video screen that simultaneously allows other accesses to the video memory. The sequencer also controls the SDRAM timing for enhanced graphics performance.

3.6 Triple Clock Synthesizer

Within the controller there are three clock synthesizers. The master clock is dedicated to the display memory (MCLK). Its rate can be varied up to 100 MHz (recommended maximum), depending upon the grade of DRAM being used. The first video clock synthesizer is the pixel output clock (VCLK) which can run up to 170 MHz (recommended maximum). The second video clock is used to support the

dual video display image with independent resolution and color depth. All of the clocks are fully programmable. VCLK also has three preset frequencies for VGA compatibility.

Both the Digital-to-Analog Converter (DAC) and Triple Clock Synthesizers are analog circuits fabricated on the Cyber9388 die. Power for the two functional circuits should be supplied from an isolated external +3.3V and GND on pins AVDD[3:0] and AVSS[3:0], respectively. The only external analog connection for the DAC is IREF, a resistor to adjust the DAC current and compensation. The Triple-Clock Synthesizer requires low-pass filters on MLF and VLF, and either a 14.318MHz TTL signal on XTLI or a 14.318MHz crystal on XTLI and XTLO for proper operation.

Normal operation for the Cyber9388 assumes the use of the on-chip Triple-Clock Synthesizer and the LUT/DAC.

The on-chip Triple-Clock Synthesizers are used to clock both the display Memory Clock (MCLK) and the two Pixel Clocks (VCLK). VCLK may be programmed by register 3C2 (bit3, bit 2) as 25, 28 or 36MHz clocks for VGA compatibility. The default 25 and 28 MHz VCLK rates may be modified by the clock registers for ergonomic refresh rate monitors. It may also be programmed via registers 3C5.16 and 3C5.17 with the constants N, M, and K to generate a frequency according to the following formula

$$\text{Frequency} = OSCx(N+8)/[(M+2)x2^{k}]$$

Note: Some restrictions apply as follows:

1. K = 0 to 3
2. M = 0 to 63
3. N = 0 to 255
4. $3.49<(N+8)/(M+2)<9.78$
5. In a noisy environment, M should be <31

The MCLK is normally generated from the on-chip oscillator. Its frequency is set by the same formula (above) in registers 3C5.16, 3C5.17. Refresh rates for the display memory DRAM must be set using registers 3x5.11 bit 6 and 3x5.2F bit 6 for VGA compatibility, or from register 83C6.04 bit 5 and bit 4 in power down modes.

Table 3-1. Bit Data Formats

MSB							
D7	D6	D5	D4	D3	D2	D1	D0
K1	K0	M5	M4	M3	M2	M1	M0
LSB							
D7	D6	D5	D4	D3	D2	D1	D0
N7	N6	N5	N4	N3	N2	N1	N0

Notes:

1. Invalid N values are: 0-7, 9-15, 18-23, 27-31, 36-39, 45-47, 54-55, 63.
2. D7-D0 = Data bus input from graphics controller;
   K1-K0 = Output frequency scale;
   M5-M0 = Reference frequency input divider;
   N7-N0 = VCO frequency divider
3. For detailed frequency programming values, reference Tables 3-4 & 3-5.

The LUT/DAC is similar in operation to a standard commercially available VGA true-color LUT/DAC. In 256 color mode, the indexed look-up tables are 18 bits wide. In HiColor and True Color mode, the pixel data is the displayed color. The LUT/DAC may be initialized and controlled from registers 3C6-9.

VCLK may be programmed as a 25, 28 or 36 MHz clock for VGA compatibility.

Actually, PCLK, the frequency at which pixels are sent out from the DAC to the display, is programmed. It has a recommended maximum value of 170 MHz. VCLK, the frequency at which pixel data is moved internally from the display queue, can be divided down from PCLK. It has a recommended maximum value of 135 MHz.

Tables 3-2 and 3-3 list the various settings of registers and corresponding frequencies, using a crystal or an oscillator with its characteristic frequency 14.318 MHz or 17.734 MHz, respectively.

In general, MCLK or VCLK frequency can be derived from the following equation:
Frequency = OSC x (N+8)/[(M+2) x 2^K]

Table 3-2. Clock Frequency Table

OSC=14.31818MHz

Registers Value		N	M	K	Freq Out	Freq. Exp	Error
Hi(hex)	**Low(hex)**				**MHz**	**MHz**	
88	3E	62	8	2	25.057	25.175	-0.0047
89	4F	79	9	2	28.311	28.322	-0.0004
88	5D	93	8	2	36.153	36.000	0.0043
83	30	48	3	2	40.091	40.000	0.0023
85	4A	74	5	2	41.932	42.000	-0.0016
84	42	66	4	2	44.148	44.000	0.0034
84	43	67	4	2	44.744	44.900	-0.0035
84	48	72	4	2	47.727	48.000	-0.0057
43	1B	27	3	1	50.114	50.350	-0.0047
46	33	51	6	1	52.798	52.800	0.0000
42	18	24	2	1	57.273	57.270	0.0000
43	21	33	3	1	58.705	58.800	-0.0016
43	23	35	3	1	61.568	61.600	-0.0005
4A	63	99	10	1	63.835	64.000	-0.0026
48	53	83	8	1	65.148	65.000	0.0023
46	43	67	6	1	67.116	67.200	-0.0012
44	33	51	4	1	70.398	70.400	0.0000
44	34	52	4	1	71.591	72.000	-0.0057
42	22	34	2	1	75.170	75.000	0.0023
44	39	57	4	1	77.557	77.000	0.0072
44	3B	59	4	1	79.943	80.000	-0.0007
44	42	66	4	1	88.295	88.000	0.0034
44	44	68	4	1	90.682	90.000	0.0076
44	4A	74	4	1	97.841	98.000	-0.0016
04	22	34	4	0	100.227	100.000	0.0023
07	3C	60	7	0	108.182	108.000	0.0017
02	19	25	2	0	118.125	118.000	0.0011
03	22	34	3	0	120.273	120.000	0.0023
05	3A	58	5	0	135.000	135.000	0.0000
05	4B	75	5	0	169.773	170.000	-0.0013
05	5A	90	5	0	200.455	200.000	0.0023

Table 3-3. Clock Frequency Table

OSC=17.734475 MHz

Registers Value		N	M	K	Freq. Out	Freq. Exp.	Error
Hi(hex)	Low(hex)				MHz	MHz	
88	31	49	8	2	25.272	25.175	0.0039
88	38	56	8	2	28.376	28.322	0.0019
88	49	73	8	2	35.913	36.000	-0.0024
86	40	64	6	2	39.903	40.000	-0.0024
84	31	49	4	2	42.120	42.000	0.0029
85	3D	61	5	2	43.704	44.000	-0.0067
85	3F	63	5	2	44.971	44.900	0.0016
84	39	57	4	2	48.032	48.000	0.0007
44	1A	26	4	1	50.249	50.350	-0.0020
46	28	40	6	1	53.205	52.800	0.0077
47	32	50	7	1	57.146	57.270	-0.0022
43	19	25	3	1	58.525	58.800	-0.0047
45	29	41	5	1	62.072	61.600	0.0077
48	40	64	8	1	63.846	64.000	-0.0024
47	3A	58	7	1	65.028	65.000	0.0004
46	35	53	6	1	67.614	67.200	0.0062
45	30	48	5	1	70.940	70.400	0.0077
44	29	41	4	1	72.417	72.000	0.0058
44	2B	43	4	1	75.373	75.000	0.0050
44	2C	44	4	1	76.851	77.000	-0.0019
46	40	64	6	1	79.807	80.000	-0.0024
45	3D	61	5	1	87.408	88.000	-0.0067
44	35	53	4	1	90.152	90.000	0.0017
44	3A	58	4	1	97.542	98.000	-0.0047
04	1A	26	4	0	100.498	100.000	0.0050
09	3B	59	9	0	108.022	108.000	0.0002
04	20	32	4	0	118.233	118.000	0.0020
03	1A	26	3	0	120.597	120.000	0.0050
06	35	53	6	0	135.228	135.000	0.0017
05	3B	59	5	0	169.748	170.000	-0.0015
05	47	71	5	0	200.151	200.000	0.0008

CPU can still access display memory, I/O registers, and the LUT/DAC. The standby state can be entered or exited through control pins, register programming, or auto detection of the CHNGDDET pin activity, display memory access, and/or keyboard access. When in simultaneous display mode, the chip activates DPMS off mode with Standby Mode.

3.10.1.3 Suspend Mode

This mode is the lowest power consumption state in the Cyber9388 before losing main power. During this state, the panel power off sequence will be activated and both display memory and video clock are shut off. The CPU can no longer access the display memory and the LUT/DAC is in power-down mode.

DRAM refresh timing may be provided by either the 14.3MHz clock or the REFCLK pin. The 14.3MHz clock can be divided down to provide 8 ms or 64 ms CAS before RAS refresh.

Self-refresh is also supported in suspend mode. When the REFCLK clock is selected or self-refresh DRAMs are used, the 14.3MHz crystal oscillator is automatically shut off, if shut off is enabled by the software control select bit.

Alternatively, software may take total control of shutting off the oscillator clock by software control bits.

This mode can be activated through a pin or register. When activated by register, the software will continue to have access to all internal registers. When activated by a pin, the host interface is also powered down. Only the pin can bring it out from the pin-suspend mode. Before the suspend pin can activate the suspend mode, a delay of 0 to 15 seconds must pass based on a software-programmed suspend timer register. When deactivated, the suspend pin is not delayed by the suspend timer.

When in simultaneous display mode, the chip will activate the DPMS off mode with suspend mode.

3.10.1.4 Off Mode (0V Suspend without DRAM Refresh)

Also known as zero-volt suspend mode or machine powered off mode, this mode allows maximum power savings for long periods. The system can save the complete state of the video subsystem and restore the state later during warm up. The Cyber9388 allows all registers to be read and written to support this mode.

3.10.2 Activating and Deactivating Power Modes

This section describes the major activating and deactivating power modes.

3.10.2.1 Controlling Standby Mode

Standby mode is activated by any combination of pin, register bit, and timer settings, depending upon which triggering mechanisms are enabled. Deactivating the standby mode is achieved by deactivating all sources that activate standby.

3.10.2.2 Controlling Suspend Mode

Suspend mode is activated by any combination of pin or register bit settings, depending on which triggering mechanisms are software enabled. If suspend mode was caused by the pin, a deactivated suspend pin will deactivate suspend mode, or the software can disable use of the suspend pin by registers to deactivate suspend mode. If suspend mode was caused by the suspend register bit, only clearing this bit will deactivate suspend mode.

3.10.3 Chip Power Sequence

3.10.3.1 Power-Up Sequence

1. I/O to turn on MCLK, VCLK and DAC (bit 2) and wait for at least 1 ms to stabilize the clock.
2. I/O to change MCLK source (bit 3) back to the original clock source.
3. Waiting about 1 ms (step 2 takes some time), I/O to set to DPMS on state.
4. I/O to set screen active mode during vertical retrace period.

3.10.3.2 Power-Down Sequence

1. I/O to set to screen off mode during vertical retrace period.
2. I/O to set to one of the DPMS power down mode.
3. I/O to select MCLK divider (bit[5:4]).
4. I/O to select refresh number to 1 (3X5.11 and 3X5.2F).
5. I/O to select 14.318 MHz source (bit 3).
6. About 50 ms later (step 5 takes some time), I/O to turn off DAC, VCLK and MCLK (bit[2:0]).

Composite sync and sub-carrier clock logic to drive the standard TV encoder is also incorporated in this section.

3.9.2 LCD Flat Panel

The Cyber9388 can directly drive a variety of panels, including:

Color active-matrix TFT panels (12,18, and 24 bit analog or (12+12), (18+18) double pixel/CLK interfaces up to 1280x1024x64K colors.

Color passive DSTN panels (16 and 24 bit) interfaces up to 1024x768x16-bit.

Interfaced with the transmitter of LVDS technology, the Cyber9388 provides a low voltage, high speed, low EMI, serial DC-balanced differential data to the LCD panel.

The flat panel interface provides or supports the following functions for various panels:

Generates flat panel interface signals like FLM, LP, SCLK, and DE.

Generates different video data formats to directly drive different types of panels.

Vertical and horizontal expansion of video displays to LCD panel resolution.

Vertical centering.

Panel power sequencing.

3.9.3 Flicker-free NTSC/PAL TV Output

The Cyber9388 incorporates "flicker removal" and "vertical scaling" logic for better video quality when displayed on an interlaced TV monitor. VGA data as well as PC games are often unusable on a TV monitor due to flicker effect, which is caused by the interlaced monitor. The Cyber9388 eliminates this by smoothing adjacent lines and eliminating one horizontal line every other six lines, which cause flicker. The vertical scaling is also used to provide better video quality when outputting the video to a TV, VCR, or panel. Since the TV screen does not display as many vertical lines as a VGA monitor, proprietary scaling is implemented to avoid losing information when lines are dropped. The data from the lines that are eliminated during scaling is compensated into adjacent lines, thereby avoiding loss of data.

The Cyber9388 supports a high quality ClearTV™ display in compliance with NTSC and PAL standards.

The 3-line flicker free TV buffer embedded in the Cyber9388 smoothes adjacent lines and eliminates horizontal lines to remove the flicker effect in conversion of non-interlaced VGA data to interlaced TV display data. As a result, a very stable and pleasant display can be achieved.

A composite Sync (Csync) and subcarrier signals are generated by the Cyber9388 to hook up with standard off-shelf TV encoders, such as the AD722™ or Sony CXA™ series.

With the support of the triple clock synthesizer and the versatile frame buffer interface, the dual display function is able to display two independent images simultaneously with different resolutions and color depths on an LCD panel and TV, or on a CRT and TV. In addition, an identical image can be displayed on a LCD display device and a TV or on a CRT and TV simultaneously.

The Cyber9388 can perform overscan and underscan, which are normally required in a computer and TV setting. The overscan is able to let VGA data fill beyond the edges of a visible area on a TV screen. The underscan allows VGA data to be filled inside the edges of the visible area of a TV screen. An automatic aspect ration adjustment will be carried out by the Cyber9388 to prevent the image from distortion caused by a different image ratio (Horizontal length/Vertical length) used in the VGA and TV.

3.10 Advanced Power Management

The Cyber9388 provides flexible and extensive Advanced Power Management (APM) capabilities. Power down modes may be activated by hardware pins, hardware timers, or software control bits. DPMS is provided in either software control mode or hardware timer mode. All Advanced Power Management (APM) functions are easily controlled using registers for MCLK, VCLK, Oscillator, LUT/DAC, Panel, Standby, and Suspend. The entire Cyber9388 graphics system, including controller and memory, may be shut down and restored because of the complete read/write capability of all registers.

3.10.1 Power States

The Cyber9388 provides multiple states of power management. The power states, or modes, are defined as ready, standby, suspend, and off (see Table 3-1). Through dedicated pins, register programming, and/or activity timers, power states can be set as follows:

3.10.1.1 Ready Mode

Ready mode is the state where the Cyber9388 is in normal operation. Functional blocks, such as DAC, can be disabled in this mode through register programming to save power.

3.10.1.2 Standby Mode

During this mode, the panel power off sequence is activated, the video clock is stopped and the video display is inactive. The internal memory timing sequencer responds only to DRAM refreshes and CPU accesses. The

3.7 VGA Controller

The high performance VGA Controller provides full hardware level VGA compatibility. At reset, the Cyber9388 is in hardware level VGA mode and all of the standard VGA subsections (Display Controller, VGA Graphics Controller, and Attribute Controller) are enabled.

3.7.1 Display Controller

The Display Controller generates the horizontal and vertical synchronization signals for flat panels and CRTs, and the composite synchronization signal (Csync) for TV displays. It provides the address interface between the video memory and display screen, cursor, and underline timing of the text modes and generates refresh requests for the DRAM refresh cycle. Auto-contrast, text-expansion, and auto-centering for image enhancement are part of the functions of this block.

3.7.2 VGA Graphics Controller

The Graphics Controller controls the graphic and the text modes for VGA compatibility. It is the interface between the video memory and the CPU during the video memory read/write operations. During system access of video memory, the Graphic Controller can perform logical operations on the memory data before reaching video memory or the system data bus. These logical operations are composed of four logical write modes and two logical read modes. The logical unit allows enhanced operations such as color compares in the read mode, individual bit masking during write modes, internal 32 bit writes in a single memory cycle, and writing to the display buffer on non-byte aligned boundaries. The Graphics Controller can also perform logic operations on memory data before it reaches the display memory or system data bus.

3.7.3 Attribute Controller

The Attribute Controller receives data from video memory and formats it for output on the display monitor, and also controls blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table and the attribute code is used to determine character color, blinking, bold, the non-interlaced underline, etc. In graphics mode, the Attribute Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the display DAC. It is then used as an address in the 18 or 24 bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.

For super VGA modes, the serialized data bypasses the Attribute Controller. When the video function is disabled, the Attribute Controller can also support the hardware cursor with the cursor pattern stored in the off-screen area.

3.8 Embedded SDRAM

With 2MB embedded Synchronous DRAMs, the data bus of display memory interface works more efficiently and economically. In addition to the improvement in performance achieved with the internal arrangement of the SDRAM, the space saved due to fewer parts required is an advantage for LCD notebook applications.

The embedded SDRAM is composed of two independent banks with hidden precharge and no penalty for bank switching. With the embedded SDRAM, all functions synchronized to clock edge, simplifying timing protocol. The bandwidth available can be increased to a rate of more than 600 Mbps.

The Display Memory Interface controls all access between the Display Memory and the Graphics Engine. It generates all memory timing and control signals, provides a character clock for the CRT controller, and fetches display data sent to the VGA Controller for final video output. It also processes the proper timing control for the display. The display memory features Single-Cycle memory read/write timing for the SDRAM.

The Cyber9388 also allows programmable SDRAM timing providing flexibility for the high quality display. Programmable SDRAM timing is controlled through internal MCLK registers. An additional State Machine clock may be inserted for RAS access time. Up to five additional State Machine clocks may be inserted for the RAS precharge. Display memory RAS, CAS timing can be tuned using register 3x5.23. Both RAS pre-charge and RAS-to-CAS delay can be adjusted by 1-5 clock cycles.

3.9 Display Interface

The Cyber9388 provides an interface to all modern flat panels and/or CRTs without additional glue logic. Integrated LUT/DAC supports True Color display. The standard NTSC/PAL encoder is also supported.

3.9.1 LUT/DAC

The integrated True Color LUT/DAC operates up to 170 MHz, allowing 1600x1200 non-interlaced displays at 75 Hz. For HiColor or True Color, the LUT/DAC works in a bypass mode where the pixel data is the color displayed. For other color modes, the DAC works in index mode where pixel data is the index to the color palette. The DAC module is compatible with the RS-343A and RS-170. It outputs RGB analog signals to directly drive an analog VGA or SVGA monitor with a dual terminated 75 ohm coaxial cable.

Table 3-4. Power State Summary

State	Display	I/O Access	Mem Access	DRAM Refresh	Chip VCC	VCLK	MCLK	DAC
Ready	on	on	on	on	on	on	on	on
Standby	off	on	on	on	on	off	on	off
Software Suspend	off	on	off	on from crystal, refCLK, or self-ref	on	off	off	off
Hardware Suspend	off	off	off	on from crystal, refCLK, or self-ref	on	off	off	off
Off	off	off	off	off	off	off	off	off

3.10.4 Panel Power Sequencing

The Cyber9388 starts the panel power sequencing. ENBKLT timing is included in the sequence to control either the Backlight or Panel Enable (on some panels). The active polarity of ENBKLT is controlled by a register bit. The power up and power down sequencing is as follows:

3.10.4.1 Power-Up Sequence

ENPVDD active

1. After one vertical timing period, the panel interface signal is active.
2. After 3 vertical timing periods, ENPVEE active.
3. After one vertical timing period, ENBKLT active.

3.10.4.2 Power-Down-Sequence

1. ENBKLT inactive.
2. After one vertical timing period, ENPVEE inactive.
3. After 3 vertical timing periods, panel interface signals are tri-stated.
4. After one vertical timing period, ENPVDD inactive.

3.10.5 CRT Power Sequencing

An approximate BIOS sequence is as follows:

3.10.5.1 Power-Up Sequence

1. Turn on MCLK/VCLK clock synthesizers and wait 1ms.
2. Program MCLK rate.
3. Select clock synthesizer as source of MCLK.
4. Program MCLK rate (if programmable clock selection is made).
5. Turn on HSYNC/VSYNC.
6. Turn on DAC.
7. Set screen on.

3.10.5.2 Power-Down Sequence

1. Set screen off.
2. Turn off DAC.
3. Set HSYNC/VSYNC to DPMS desired state.
4. Turn off VCLK synthesizer.
5. Set divisor of external 14.318 clock as source of MCLK.
6. Turn off internal MCLK synthesizer.

Table 3-5 DPMS State Summary with CRT Only and Hardware Timers

State	HSYNC	VSYNC	VCLK	MCLK	DAC
Ready	on	on	on	on	on
Standby	off	on	off	on	off
Suspend	on	off	off	on	off
Off	off	off	off	on	off

3.11 Power-Up Configuration

The Cyber9388 uses memory data signals (MD[39:0]) as the power up configuration input during system RESET. All MD bus data signals have a pull-up resistor on their I/O buffer. An external pull-down resistor must connect to the MD bus pin for the signals that configure as low (0) input.

3.12 Timer Modes

The Cyber9388 offers a flexible timer for use in Standby, and DPMS. The timer may be programmed to monitor a programmable inactivity period based on any combination of pin, memory accesses, and keyboard accesses.

The timer period is programmable to count ½ minute or 1 to 15 minutes in 1 minute intervals. If there is no activity on the monitored logic for the selected period, the time-out status is set and reflected on a readable bit.

The time-out state is reset in different ways, depending on the use of the timer. In all configurations, selecting no monitored activity (setting the Timer Activity Monitor select bits to 000) will reset the time-out state. In addition, if the timer is used for Standby or DPMS, activity on the monitored logic can reset the time-out state.

3.13 Testability

In order to help diagnosis of the engineering and production samples, some testing circuits are included in the Cyber9388. The whole chip can be divided into three sections for testing: clock synthesizer, DAC, and the VGA core.

3.13.1 Observation of Internal VCLK and MCLK

When the on-chip clock synthesizer is used, the internally generated VCLK and MCLK can be observed on pin VCLK, controlled by 3D5.3B, bits 6 and 5. For high frequencies, i.e., 135Mhz VCLK, the internal clock can be divided down for observation, controlled by 3D5.3B, bit 4. This is useful in the production environment.

3.13.2 DAC Testing

To test the on-chip DAC, the DAC is first set in the test mode. The pixel data bus [7:0] is used to send data in and the analog out is observed on the R, G, and B pins. At the current writing, the maximum pixel data and clock that can be generated by external testing equipment is 120Mhz. It is particularly challenging to test a 170Mhz operation in the lab and in the production environment.

3.13.3 Pin Scan Testing

Pin scan provides a mechanism to test printed circuit boards to determine whether the Cyber9388 is properly soldered into the printed circuit board or not. Any signal pins that are not connected to the circuit board or shorted to a neighboring pin or trace will be detected using a circuit board tester.

When pin scan is enabled, all pins are connected sequentially around the Cyber9388 into a single chain. The first pin in the chain must be an input pin, and the last pin is an output pin. Each input and the input side of a bi-directional pin is exclusive-ORed with the scan data from the previous neighboring input or output pin. On the output pin, data from the previous stage is inverted then sent to the next stage. The output side of a bi-directional pin must be tri-stated, and a uni-directional tri-state output pin must be enabled.

To enable pin scan testing, hold the ENTEST# pin and the ROMCS# pin low, which will force all bi-directional pins into tri-state and all uni-directional tri-stated output pins into an output enable state. Once in pin scan mode, the tester drives all the input pins to zero and checks the output pin values. After that, one input pin at a time is driven to a logical high value, and all the output pin states are observed. Typically, if an input pin's value is changed and all the higher-numbered output pins assume an incorrect value, then that input pin is either shorted or unsoldered. If an input is changed and all the higher-numbered outputs are correct except for one output, then that output pin is either shorted or unsoldered.

In the Cyber9388, the first pin of the chain is input pin PCICLK, and the last pin of the chain is output pin INTA#. The rest of the pins are connected counterclockwise into a scan chain. During final chip or circuit board testing, it is possible to connect the INTA# pin and the PCICLK pin together to from a ring oscillator. The speed grade of each chip can then be sorted. The number of inversion stages in the Cyber9388 is arranged to be an odd number. The pin scan order is shown in the pin assignment section.

3.13.4 Signature Analysis

Signature analysis is used to generate a unique value within a frame for a specific mode when the frame buffer is loaded with a specific pattern. The known good value, which is provided by Trident, is compared with the value generated within the signature generator register to determine if the controller is good or bad. This feature is useful in the mass production environment for quickly sorting the good parts/boards. There is one place checked by the signature generator within the Cyber9388 in the RAMDAC block, just before the processed pixel data is sent to the DAC. To test RAM, there is a testing bit, which

will select whether the RAMDAC is in indexed mode or by-pass mode. If the by-pass mode is correct and the indexed mode is incorrect, the RAM may have a problem. With the signature analysis, the testing time can be reduced significantly.

The signal analysis circuit is composed of a 16-bit signature generator register, clocked by the pixel clock, with some feedback circuits to ensure the minimal overlapping of signatures for different patterns. To enable the signature analysis, bit 7 of register 3C5.21 is set to 1 (busy) after the signature generator registers are reset. Signature analysis is started at the rising edge of the next VSYNC signal and stopped at the rising edge of VSYNC following the starting VSYNC signal. Between these two VSYNC signals defines the GATE condition during which the signal analysis is performed. For text modes, the blinking function should be disabled to make the signature unique. Each bit of the 24-bit pixel data, which is selected by bits [4:0] of register 3C5.21, is sent to the signature analysis circuit. Each pixel clock between two VSYNC signals will update the content of the signature register. After this process is finished, which is indicated by bit 7 of register 3C5.21 being reset to 0, the CPU can then read the content of the signature generator registers for comparison. This process is continued until all pixel data signals are analyzed. The graphics engine can be analyzed similarly before and after the hardware acceleration is performed.

Table 3-6. Fixed Sizing Vertical Expansion and Compression

Display Device Resolution	Display Mode							
	350	400	480	600	768	1024		
LCD 640x480	c,e	c,e	c,e	c,e	480	N/A	N/A	N/A
LCD 800x600	525	525	c,e	c,e	c,e	600	N/A	N/A
LCD 1024x768	700	700	600	600	720	N/A	800	N/A
LCD 1280x1024	700	700	800	800	960	N/A	N/A	1024
NTSC 534x400	top	top	full	full	c	N/A	N/A	N/A
NTSC 640x480	Same as LCD 640x480							
PAL 640x480	Same as LCD 640x480							
PAL ~800x600	Same as LCD 800x600							

Table Code: c = centered, e = expanded, full = full resolution, and N/A = not applicable.

Table 3-7. Horizontal Expansion and Compression

Display Device Resolution	Display Mode					
	640 320 C	640 320 E	640	768	1024	1280
LCD 640x480	full	full	640 ->full	N/A	N/A	N/A
LCD 800x600	c,e	c,e	640 ->c,e	800	N/A	N/A
LCD 1024x768	960	960	960	N/A	1024	N/A
LCD 1280x1024	1280	1280	640 ->1280	N/A	N/A	1280
NTSC 534x400	top	top	full	N/A	N/A	N/A
NTSC 640x480	Same as LCD 640x480					
PAL 640x480	Same as LCD 640x480					
PAL ~800x600	Same as LCD 800x600					

3.14 EEPROM/DDC Support

The Cyber9388 has eight (8) GPIO pins, any two of which may be used to interface with any two wire 3V or 5V serial interface, such as the VESA DDC standard or the AT24C01™ from Atmel. Monitors equipped with DDC or systems with this EEPROM can be used to store system information such as monitor type, timing, serial number, etc.

The DDC INTERFACE/EEPROM requires two pins to communicate with the Cyber9388 controller: SCL (serial clock) and SDA (serial data). To ensure proper operation, the timing specified by the DDC INTERFACE / EEPROM must be met, which is controlled by the programmer. The functional timing for the DDC INTERFACE/EEPROM interface is shown in Figure 3.3.

The sequence of DDC INTERFACE / EEPROM operation is as follows:

1. Send START signal
2. Send 7-bit starting address
3. Send direction signal (R/W#)
4. Monitor ACK to ensure that the DDC INTERFACE/EEPROM has received starting address
5. Send 8-bit data (terminated with receiving ACK) (W#) or receive 8-bit data (terminated with sending ACK) (R)
6. Continue step 7 until all data bytes are sent (W#) or received (R)
7. Send STOP signal

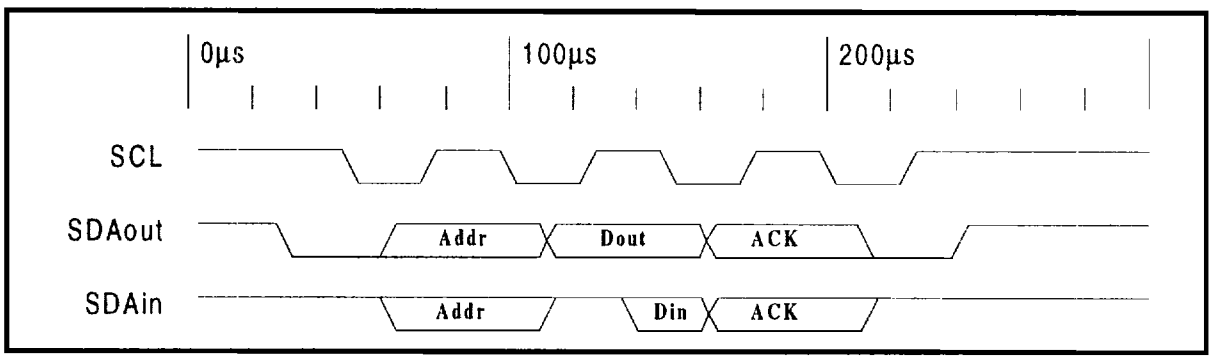

Figure 3-2. DDC INTERFACE/EEPROM Timing

3.15 ZV/Capture/VMI Port

The function of the video capture is to receive any digital video pixel data streams from other video sources, such as TV decoders, VCR, MPEG 1 and 2, etc., and store them in the frame buffer. The stored video image can be either displayed together with a graphics image or fetched by the CPU to perform further processing such as video editing or hard disk storage. For video capture, there are two possible data paths. One path is from the capture port and the other one is from the PCI host interface. They are merged together before any video data processing, buffered in the video FIFO, and then sent to the frame buffer.

The versatile capture port can be configured as a video port or the Zoom Video (ZV) port. The fourth generation of the Video processing engine in the Cyber9388 greatly improves the quality and functions of video processing. The major function blocks are the Video Capture Processing and the dual overlay window Video Display Processing. The Video inputs can either be from the PCI bus or the Video Capture Port which share the same pins with the IBM feature connector (FC). This video engine accepts 8-bit and 16-bit video data bus width of standard video source input formats (CCIR656/CCIR601), providing a glueless I/F with various decoders such as IBM MPEG 2, BT815, SAA7110/1, CL450, etc. The programmable input formatter accepts various YUV/RGB formats, integrates a programmable luminance interpolating filter and an independent linear X and Y minifier.

The Cyber9388 allows a PC card to write video data directly into the frame buffer under the graphics controller. Three different flavors of controllable sizes and shapes of images can be overlaid with a mixed color depth up to the true color through the adjustments of the window key, color key, and chroma key.

The video image is stored in the off-screen memory and the Video Display Processing block fetches the data from the off-screen memory and performs scaling operations with linear interpolation in both X and Y directions. In addition, it converts the YUV pixels into linear RGB888 pixels on the fly. The video image is overlaid with different color depths of the graphic data according to the color key. The hardware scaling and color space conversion accelerate the DirectDraw™ applications and accelerate the frame rate of the software playback.

The Cyber9388 is able to handle Intercast (VBI, Vertical Blanking Interval) supporting TV broadcasting with embedded web-site information.

3.16 Chip Block Diagram

The Cyber9388 can be divided into major blocks as shown in Figure 3-4. They are: host interface, including post write FIFO; GRAC for handling planar modes; CRT controller, which controls both graphic and video circuits including ATTRC, line buffer, VDE, graphic display queue, and hardware cursor; memory interface; GE, 64-bit graphics engine including data FIFO, clock synthesizer, DAC, Sequencer; and embedded SDRAMs with the Build-In-Self-Test (SDRAM BIST) unit. Part of the Sequencer, GRAC, part of the CRT controller, the ATTRC, and some registers for VGA compatibility constitute the VGA core.

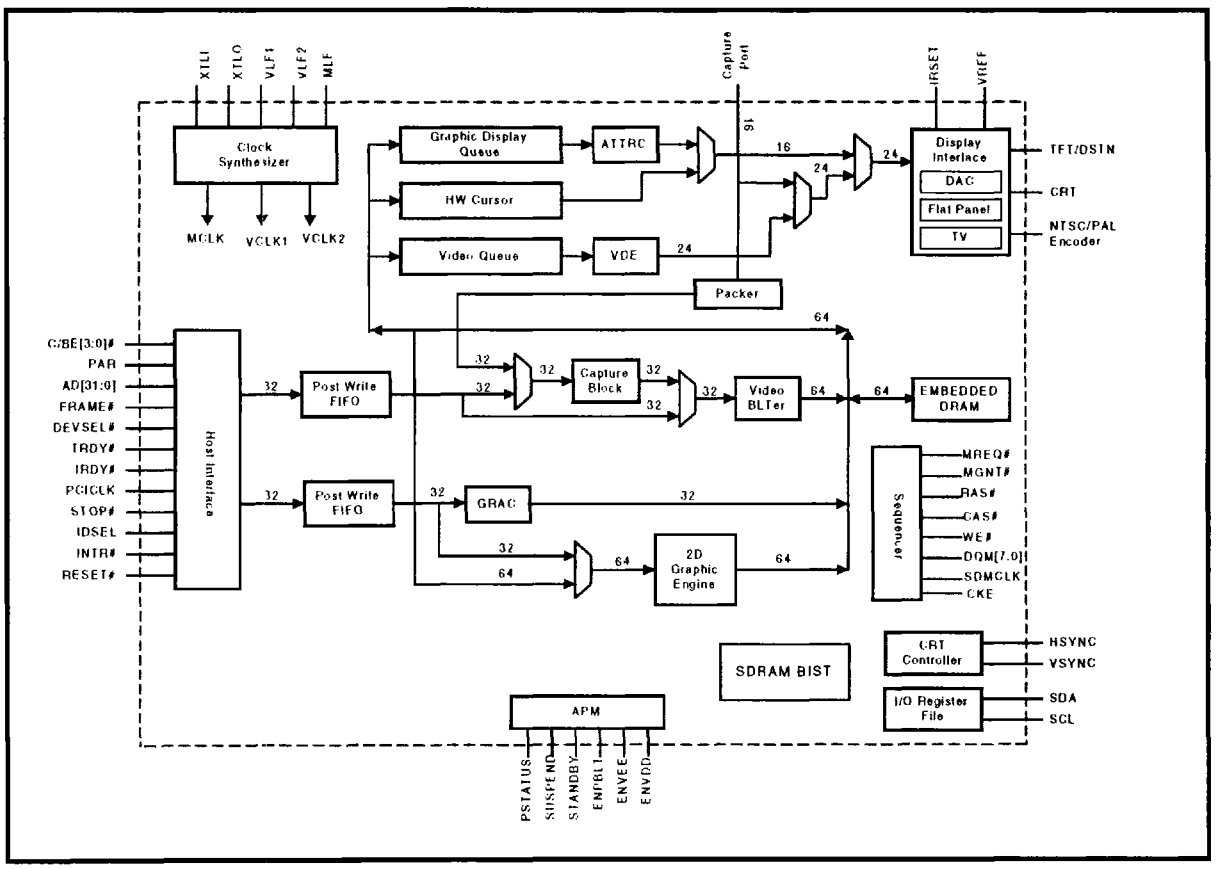

Figure 3-3. Chip Block Diagram

4. Electrical Specifications

This section describes the specifications of the Cyber9388.

4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Case Temperature	0 to 85 Celsius
Storage Temperature	-65 to 150 Celsius
DC Supply Voltage, VDD	-0.5 to 4.6 Volts
DC Input Voltage, V_{IN} (except I/O pins)	-0.5 to 4.6 Volts
DC Output Voltage, V_{out} (including I/O pins)	-0.5 to VDD + 0.5 Volts (Not exceeding 4.6 Volts)
DC Input Current, I_{IK}	± 20 mA
DC Output Current, I_{OK}	± 50 mA

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under absolute-maximum-rated conditions is not implied.

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
VDD	Supply voltage	2.7	3.6	V
V_{IN}	Input voltage		VDD	V
V_{OUT}	Output voltage		VDD	V
T_A	Operating free-air temperature	-40	85	°C
$\Delta t/\Delta V$	Input transition rise or fall rate (between 0.8 V and 2.0 V)	0	8	ns/V

4.3 DC Specifications

Table 4-3. DC Specifications

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage.		0.8	V	VCC = 3.3 V±0.3V
VIH	Input High Voltage.	2.0		V	VCC = 3.3 V±0.3V
VOL	Output Low Voltage.		VSS+0.4	V	
VOH	Output High Voltage.	2.4		V	
IIL	Input Low Current.		±5	µA	VIN = 0.0 V, except I/O ports
IIH	Input High Current.		±15	µA	VIN = VCC, I/O ports
IOH, IOL	Output Current (per pin*)	4	16	mA	VCC = 3.3 V ± 5%
IOZ	Off-state Leakage Current.		±10	µA	
CIN	Input Capacitance.		10	pF	FC = 1MHz
COUT	Output Capacitance.		10	pF	FC = 1MHz
CI/O	I/O Pin Capacitance.		10	pF	FC = 1MHz
ICC	Power Supply Current.		TBD	mA	VCC = 3.3 V±5%

***Note:** Depends on pin's function. See Section 6 for more details.

4.4 AC Specifications

This section describes the AC Specifications.

4.4.1 Clock and Reset Timing

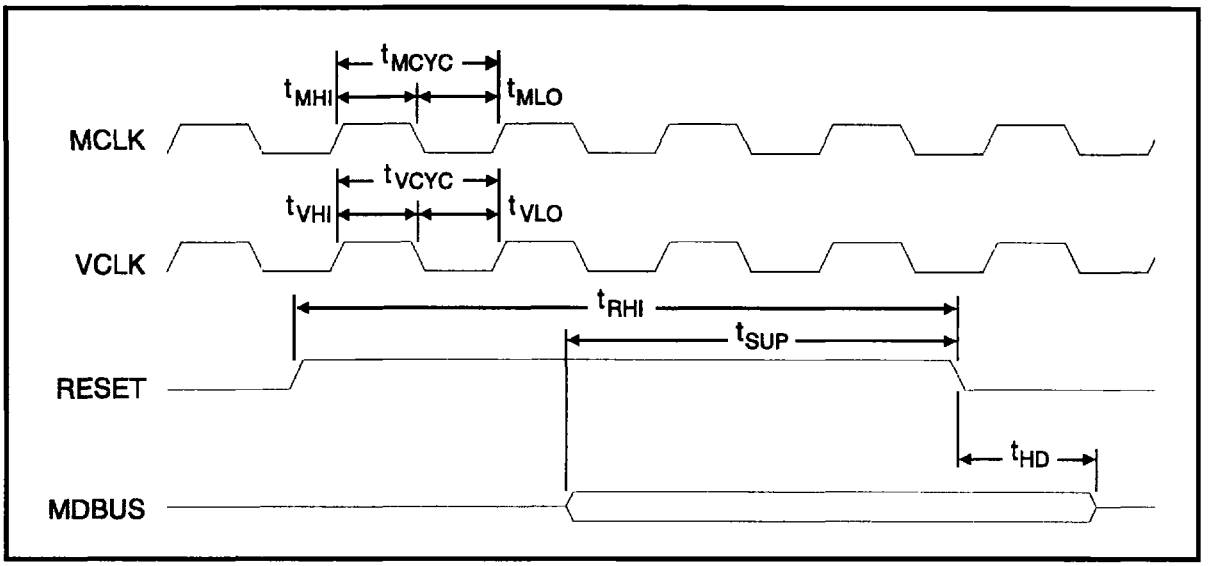

Figure 4-1. Clock and Reset Timing Diagram

Table 4-4. Clock and Reset Timing

Symbol	Min (ns)	Max (ns)	Comment
t_{MCYC}	12.5		MCLK period.
t_{MHI}	6		MCLK high time.
t_{MLO}	6		MCLK low time.
t_{VCYC}	12.5		VCLK period.
t_{VHI}	6		VCLK high time.
t_{VLO}	6		VCLK low time.
t_{RHI}	200		RESET high time.
t_{SUP}	30		Configuration setup time.
t_{HD}	10		Configuration hold time.

4.4.2 DDC INTERFACE/EEPROM Timing

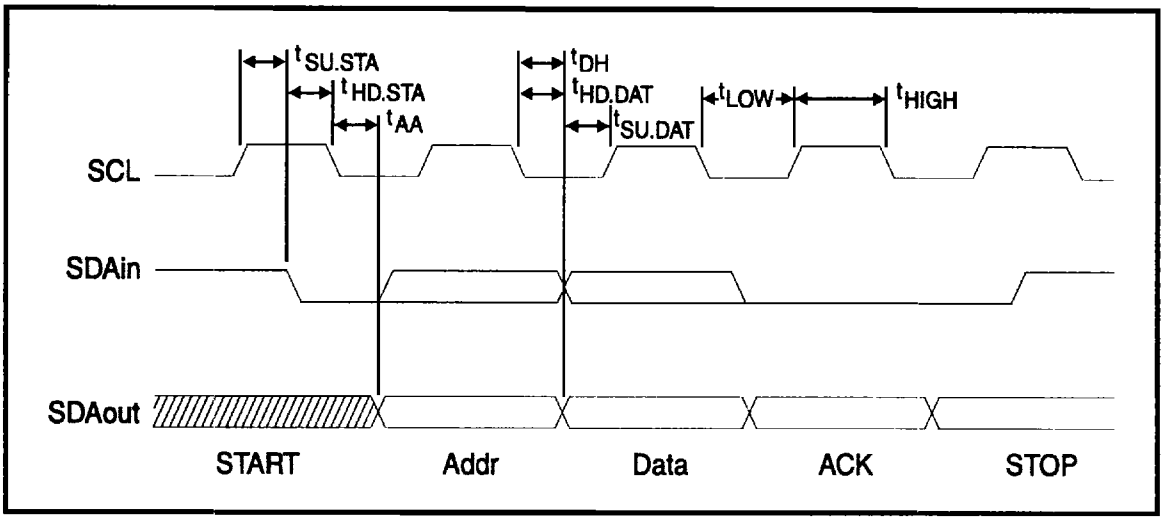

Figure 4-2. EEPROM Timing Diagram

Table 4-5. EEPROM Timing

Symbol	Min (µs)	Max (µs)	Comment
$t_{SU.STA}$	4.7		Start set-up time.
$t_{HD.STA}$	4.0		Start hold time.
t_{AA}	0.1	3.5	Clock low to data out valid.
t_{DH}	0.1		Data out hold time.
$t_{HD.DAT}$	0		Data in hold time.
$t_{SU.DAT}$	0.05		Data in set-up time.
t_{LOW}	4.7		Clock pulse width low.
t_{HIGH}	4.0		Clock pulse width high.

4.4.3 PCI Bus Timing

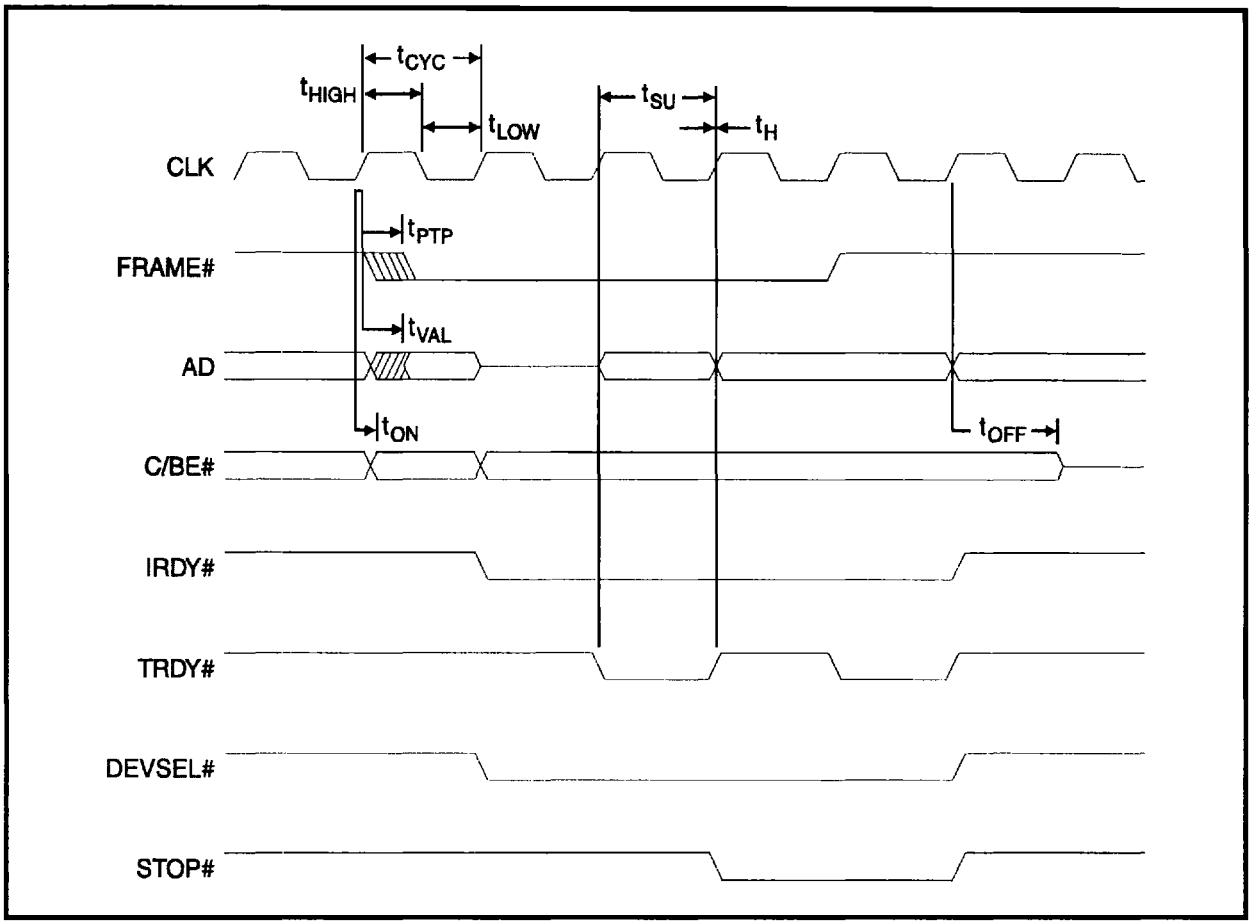

Figure 4-3. PCI Bus Timing Diagram

Table 4-6. PCI Bus Timing

	33MHz		66MHz		
Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Comment
t_{CYC}	30		15	30	CLK cycle time.
t_{HIGH}	12		6		CLK high time.
t_{LOW}	12		6		CLK low time.
t_{VAL}	2	11	2	6	CLK to signal valid delay - bus signals..
t_{PTP}	2	12	2	6	CLK to signal valid delay - point to point signals.
t_{ON}	2		2		Float to active delay.
t_{OFF}	28			14	Active to float delay.
t_{SU}	7		5		Input setup time to CLK.
t_{H}	0		0		Input hold time from CLK.

4.4.4 Vertical Timing

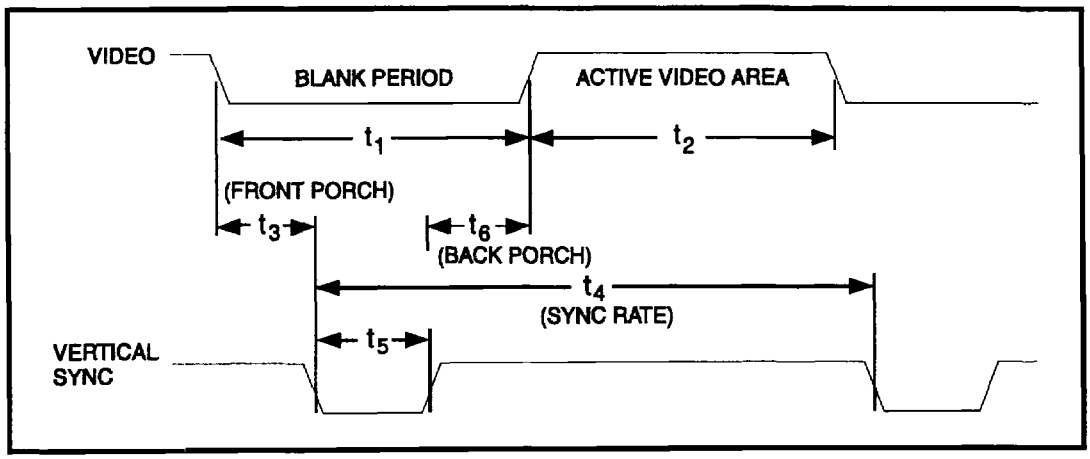

Figure 4-4. Vertical Timing Diagram

Table 4-7. Vertical Timing (ms)

Mode	CLK	Type	Display	Max Colors	t_1	t_2	t_3	t_4	t_5	t_6	Polarity
0,1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	1.87	–
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	1.87	–
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	1.08	+
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	1.08	+
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	1.87	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	1.08	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	1.08	+
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	1.08	+
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	1.87	–
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	1.87	–
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	1.02	–
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	1.02	–
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	1.08	+
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	1.02	–
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	1.05	–
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	1.02	–
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	1.86	–

Table 4-7. Vertical Timing (ms) (Cont'd)

Mode	CLK	Type	Display	Max Colors	t_1	t_2	t_3	t_4	t_5	t_6	Polarity
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	0.60	–
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	0.96	–
56	40.0	A/N	132x60	16	1.376	15.360	0.352	16.736	0.064	0.60	–
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	1.80	–
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	0.93	–
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	1.06	–
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	0.93	–
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	0.56	–
5C[1]	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	1.08	+
5C[2]	25.2	APA	640x400	256	11.02	.557	12.711	0.413	14.268	1.08	+
5D[1]	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	1.02	–
5D[2]	25.2	APA	640x480	256	1.430	12.253	0.350	16.683	0.064	1.02	–
5E[1]	72.0	APA	800x600	256	0.711	17.067	0.028	17.778	0.057	0.86	–
5E[2]	36.0	APA	800x600	256	0.711	17.067	0.028	17.778	0.057	0.56	–
5E[3]	50.3	APA	800x600	256	1.395	12.489	0.479	13.883	0.125	0.79	+
5F	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	0.66	+
5F	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	0.58	+
5F[3,4]	75.0	APA	1024X768 (HR)	16	0.673	13.599	0.053	14.272	0.106	0.51	+
60	44.9	APA	1024X768(I)	4	0.873	10.810	0.155	11.683	0.056	0.66	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	0.63	+
62	44.9	APA	1024x768 (I)	256	0.873	10.810	0.155	11.683	0.056	0.66	+
62	65.0	APA	1024x768 (NI)	256	0.945	15.785	0.329	16.731	0.041	0.58	+
62[3,4]	75.0	APA	1024x768 (HR)	256	0.673	13.599	0.053	14.272	0.106	0.51	+
63	75.0	APA	1280X1024 (I)	16	1.120	10.705	0.379	11.835	0.084	0.67	+
64	75.0	APA	1280X1024 (I)	256	1.120	10.705	0.379	11.835	0.084	0.67	+
65	162.0	APA	1600x1200 (NI)	16	0.667	16.000	0.013	16.687	0.04	0.613	+
66	175.5	APA	1600x1200 (NI)	256	0.615	14.768	0.012	15.400	0.037	0.566	+
6C	75.0	APA	640x480	16M	1.430	15.253	0.350	16.683	0.064	1.02	–
70/71[5]	77.0	APA	512x480	32/64K	1.430	15.253	0.350	16.683	0.064	1.02	–
74/75[5]	50.35	APA	640x480	32/64K	1.430	15.253	0.350	16.683	0.064	1.02	–
76/77[5]	72.0	APA	800x600	32/64K	1.430	15.253	0.350	16.683	0.064	0.56	–
7A/7B	157.5	APA	1280x1024	32/64K	0.527	11.235	0.011	11.800	0.033	0.483	+

Notes:
1. 16-bit DRAM bus version of mode.
2. 32-bit DRAM bus version of mode.
3. Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801.
4. HR=High refresh or 70Hz vertical refresh.
5. Same timing on 32K and 64K color modes.

4.4.5 Horizontal Timing

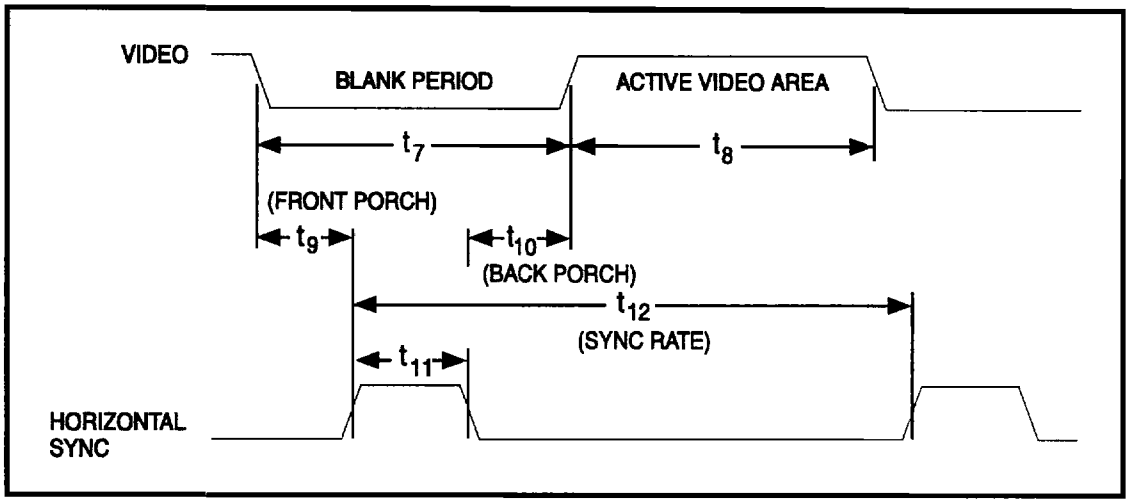

Figure 4-5. Horizontal Timing Diagram

Table 4-8. Horizontal Timing (µs)

Mode	CLK	Type	Display	Max Colors	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	Polarity
0,1	25.2	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	–
2,3	25.2	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	–
0*,1*	25.2	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	–
2+,3+	28.3	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	–
4,5	25.2	APA	320x200	4	6.356	25.422	0.636	1.907	3.813	31.778	–
6	25.2	APA	640x200	2	6.356	25.422	0.636	1.907	3.813	31.778	–
7	28.3	A/N	80x25	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	6.356	25.422	0.636	1.907	3.813	31.778	–
E	25.2	APA	640x200	16	6.356	25.422	0.636	1.907	3.813	31.778	–
F	25.2	APA	640x350	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	6.356	25.422	0.636	1.907	3.813	31.778	–
12	25.2	APA	640x480	16	6.356	25.422	0.636	1.907	3.813	31.778	–
13	25.2	APA	320x200	256	6.356	25.422	0.477	2.066	3.813	31.778	–
50	25.2	A/N	80x30	16	6.356	25.422	0.636	1.907	3.813	31.778	–
51	25.2	A/N	80x43	16	6.356	25.422	0.636	1.907	3.813	31.778	–
52	25.2	A/N	80x60	16	6.356	25.422	0.636	1.907	3.813	31.778	–

Table 4-8. Horizontal Timing (µs) (Cont'd)

Mode	CLK	Type	Display	Max Colors	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	Polarity
53	40.0	A/N	132x25	16	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	5.600	26.400	0.000	1.800	3.800	32.000	–
55	40.0	A/N	132x43	16	5.600	26.400	0.000	1.800	3.800	32.000	–
56	40.0	A/N	132x60	16	5.600	26.400	0.000	1.800	3.800	32.000	–
57	44.9	A/N	132x25	16	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	5.612	26.459	-0.200	1.804	4.009	32.071	–
59	44.9	A/N	132x43	16	5.612	26.459	-0.200	1.804	4.009	32.071	–
5A	44.9	A/N	132x60	16	5.612	26.459	-0.200	1.804	4.009	32.071	–
5B	36.0	APA	800x600	16	6.222	22.222	0.667	3.500	2.028	28.660	–
5B[1]	50.35	APA	800x600	16	4.926	15.889	0.794	2.066	2.066	20.814	+
5C[2]	50.35	APA	640x400	256	6.356	25.422	0.556	1.668	4.131	31.778	–
5C[3]	25.2	APA	640x400	256	6.356	25.422	0.636	1.907	3.813	31.778	–
5D[2]	50.35	APA	640x480	256	6.356	25.422	0.556	1.668	4.131	31.778	–
5D[3]	25.2	APA	640x480	256	6.356	25.422	0.636	1.907	3.813	31.778	–
5E[2]	72.0	APA	800x600	256	6.222	22.222	0.667	3.500	2.028	28.660	+
5E[3]	36.0	APA	800x600	256	6.222	22.222	0.667	3.500	2.028	28.660	–
5E[3]	50.3	APA	800x600	256	4.926	15.889	0.794	2.066	2.066	20.814	+
5F	44.9	APA	1024x768 (I)	16	5.345	22.806	0.204	1.260	3.956	28.151	+
5F	65.0	APA	1024x768 (NI)	16	4.800	15.754	0.615	1.108	3.077	20.554	+
5F[1,4]	75.0	APA	1024X768 (HR)	16	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024X768(I)	4	5.345	22.806	1.069	1.782	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	9.265	17.105	-1.782	4.633	4.811	26.370	+
62	44.9	APA	1024x768 (I)	256	5.345	22.806	-0.178	2.851	2.316	28.151	+
62	65.0	APA	1024x768 (NI)	256	4.800	15.754	0.615	1.108	3.077	20.544	+
62[1,4]	75.0	APA	1024x768 (HR)	256	4.053	13.653	0.320	1.920	1.813	17.707	+
63	75.0	APA	1280X1024 (I)	16	3.965	17.035	0.255	0.205	3.400	21.000	+
64	75.0	APA	1280X1024 (I)	256	3.965	17.035	0.255	0.205	3.400	21.000	+
65	162.0	APA	1600x1200 (NI)	16	3.457	9.877	0.395	1.877	1.187	13.300	+
66	175.5	APA	1600x1200 (NI)	256	3.191	9.117	0.365	1.732	1.094	12.300	+
6C	75.0	APA	640x480	16M	6.356	25.422	0.636	1.907	3.813	31.778	–
70/71[5]	77.0	APA	512x480	32/64K	6.356	25.422	0.636	1.907	3.813	31.778	–
74/75[5]	50.35	APA	640x480	32/64K	6.356	25.422	0.636	1.907	3.813	31.778	–
76/77[5]	72.0	APA	800x600	32/64K	6.222	22.222	0.667	3.500	2.028	28.660	–
7A/7B	157.5	APA	1280x1024	32/64K	2.844	8.127	0.305	1.524	1.016	11.000	+

Notes:
1. Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801.
2. 32-bit DRAM bus version of mode.
3. HR=High refresh or 70Hz vertical refresh.
4. Same timing on 32K and 64K color modes.

4.4.6 PCI ROM BIOS Access Timing

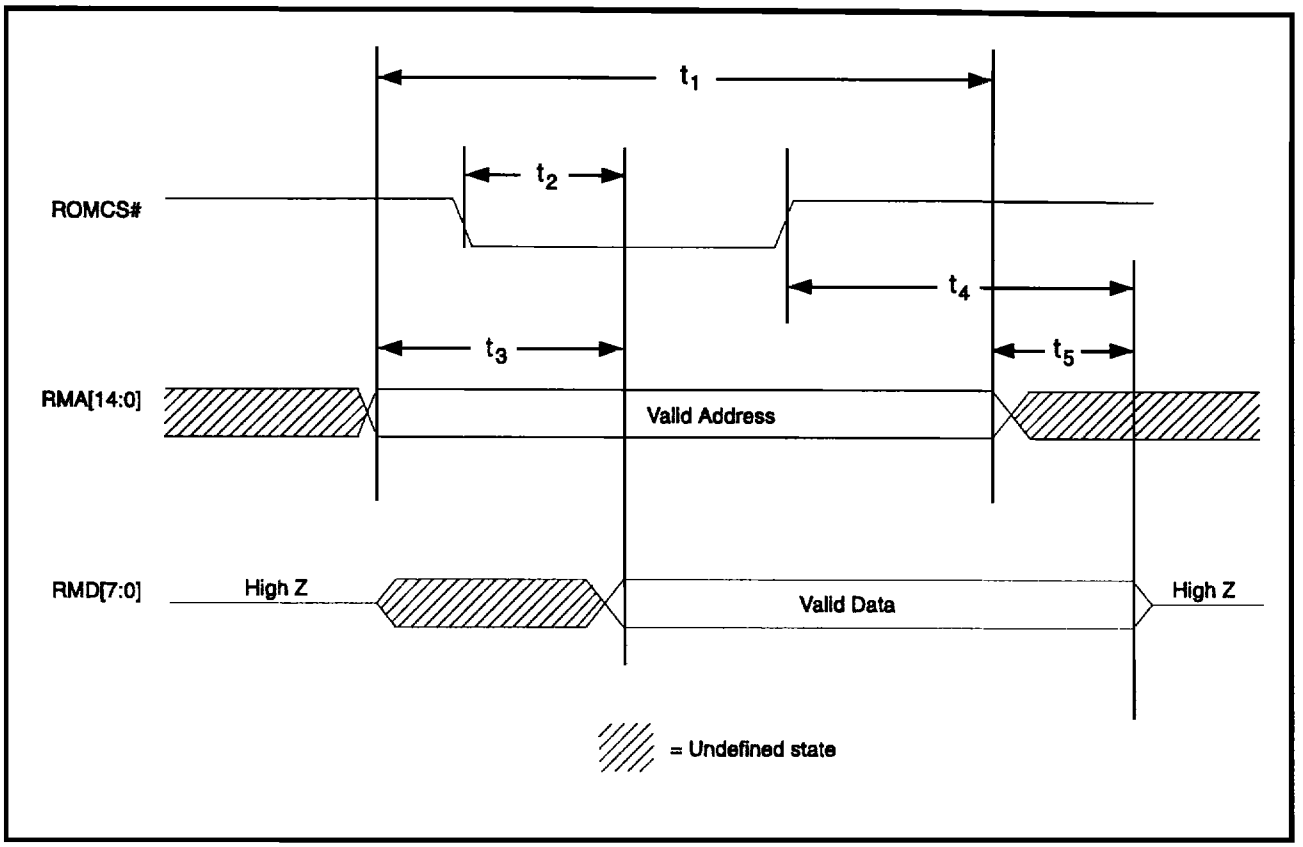

Figure 4-6. PCI ROM BIOS Access Timing Diagram

Table 4-9. PCI ROM BIOS Access Timing

Symbol	Description	Min (ns)	Typ (ns)	Max (ns)
t_1	Cycle time.		32 DMCLKs	
t_2	Chip enable access time.			150
t_3	Address access time.			150
t_4	Data to high Z delay time.			85
t_5	Valid data from invalid address hold time.	10		

4.4.7 Panel Power Sequencing Timing

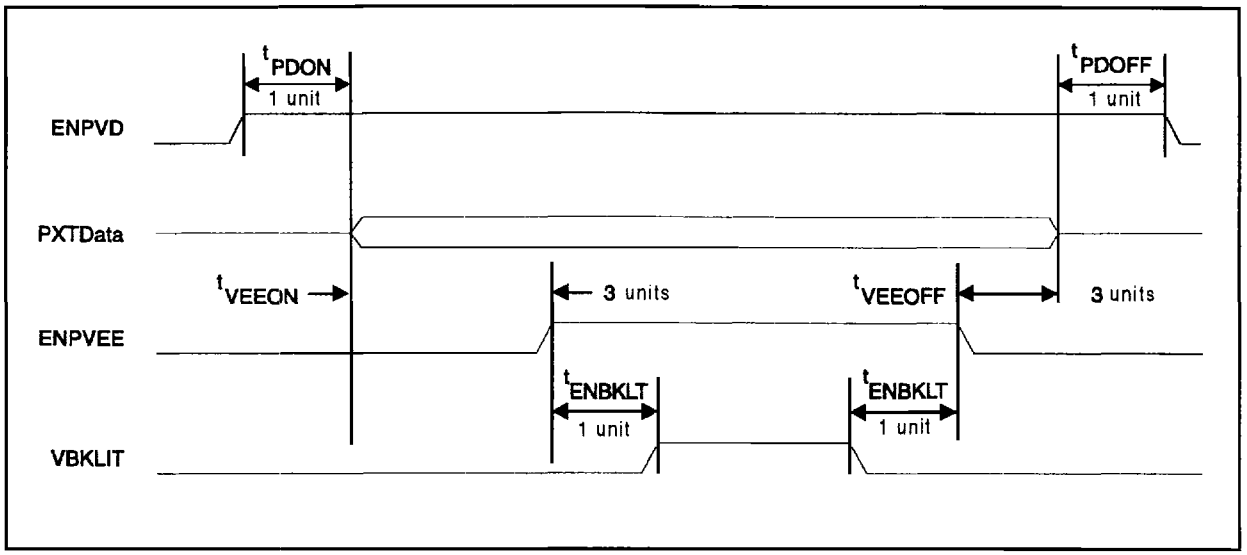

Figure 4-7. Panel Power On/Off Sequence

Table 4-10. Panel Power On/Off Sequence

Symbol	Description	Typical	Unit
t_{PDON}	Enable Panel Data	1	Frame/Programmable[1] 4ms
t_{PDOFF}	Disable Panel Data	1	Frame/Programmable[1] 4ms
t_{VEEON}	Enable Panel BIOS Volts	3	Frame/Programmable[1] 4ms
t_{VEEOFF}	Disable Back Light	3	Frame/Programmable[1] 4ms
t_{ENBKLT}	Enable Back Light	1	Frame/Programmable[1] 4ms

Note 1: The timing is software programmable. Refer to 3CF.23.3, 3CF.24[3:0] and 3CF.25[3:0].

4.4.8 Flat Panel Interface Timing

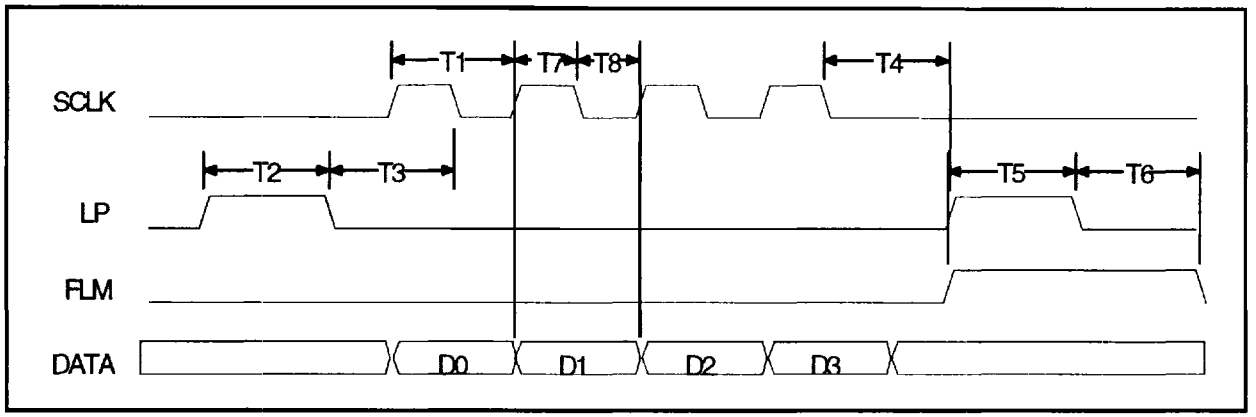

Figure 4-8. Flat Panel Interface Timing

Table 4-11. Flat Panel Interface Timing

Symbol	Name	Min (ns)	Max (ns)	Comment
T1	T1	15		SCLK cycle time
T2	T2	4T1		LP high time
T3	T3	20		LP falling edge to SCLK rising edge
T4	T4	20		SCLK falling edge to LP rising edge
T5	T5	100		FLM setup time
T6	T6	40		FLM hold time
T7	T7	5		panel DATA setup time
T8	T8	10		panel DATA hold time

4.4.9 VMI Host Port Timing

The VMI port is provided for the Cyber9388 to communicate with any other device which may not have a PCI host interface, such as an MPEG decoder (Trident's 9530). The VMI timing is shown in Figure 5-13.

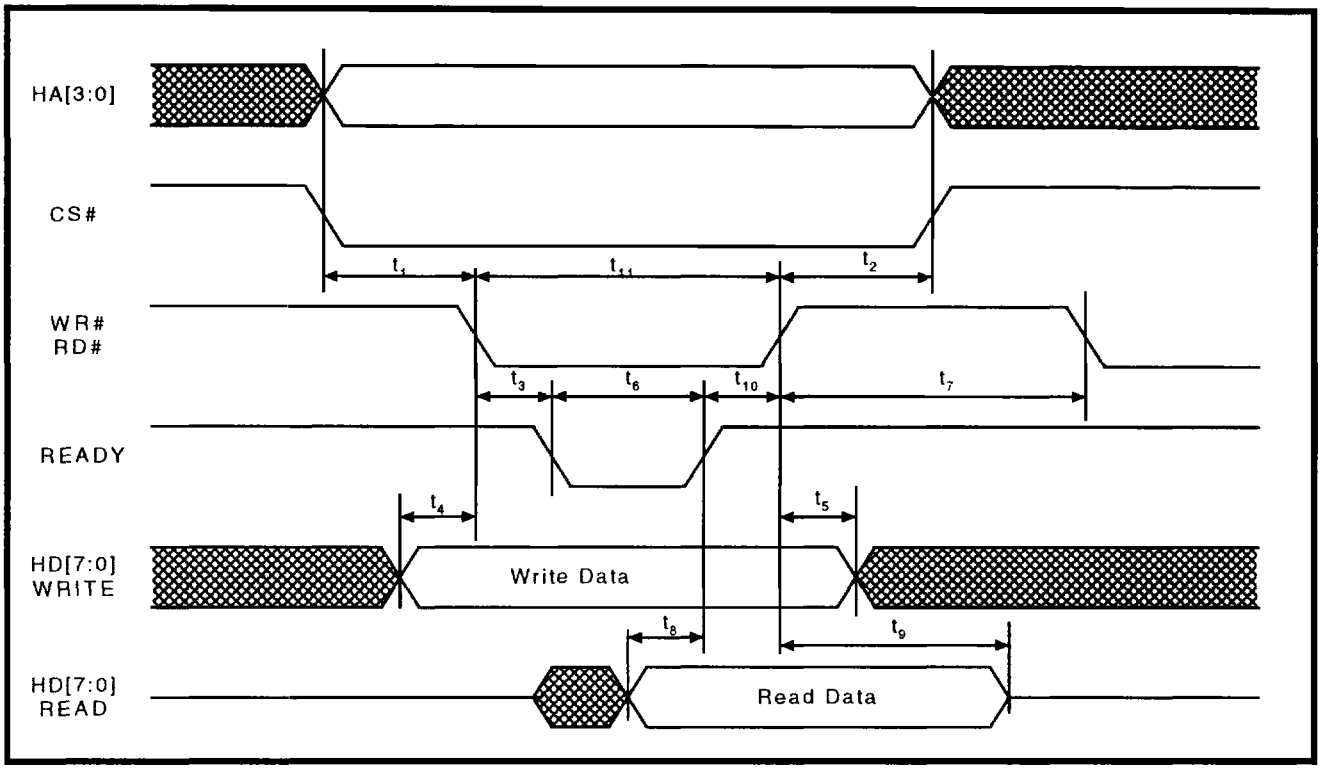

Figure 4-9. VMI Host Port Timing

Table 4-12. Video Module Interface Timing

Symbol	Min (ns)	Max (ns)	Description
t_1	10	-	HA, CS# setup until WR# or RD# LOW
t_2	0	-	HA, CS# hold after WR# or RD# HIGH
t_3	-	28	Delay READY LOW after WR# or RD# LOW
t_4	5	-	HD setup until WR# LOW
t_5	10	-	HD hold after WR# HIGH
t_6	0	-	READY pulse width
t_7	38	-	WR# HIGH until any command
t_8	0	-	(Read Cycle) HD setup until READY active
t_9	0	15	(Read Cycle) HD hold after RD# inactive
t_{10}	0	100	Delay WR# or RD# HIGH after READY HIGH
t_{11}	40	-	Read/Write command pulse width

4.4.10 TV Composite SYNC Timing

A composite sync signal is required by most TV encoder chips. The Cyber9388 provides correct composite timing that meets TV standards such as PAL or NTSC specifications.

4.4.10.1 NTSC TV Timing

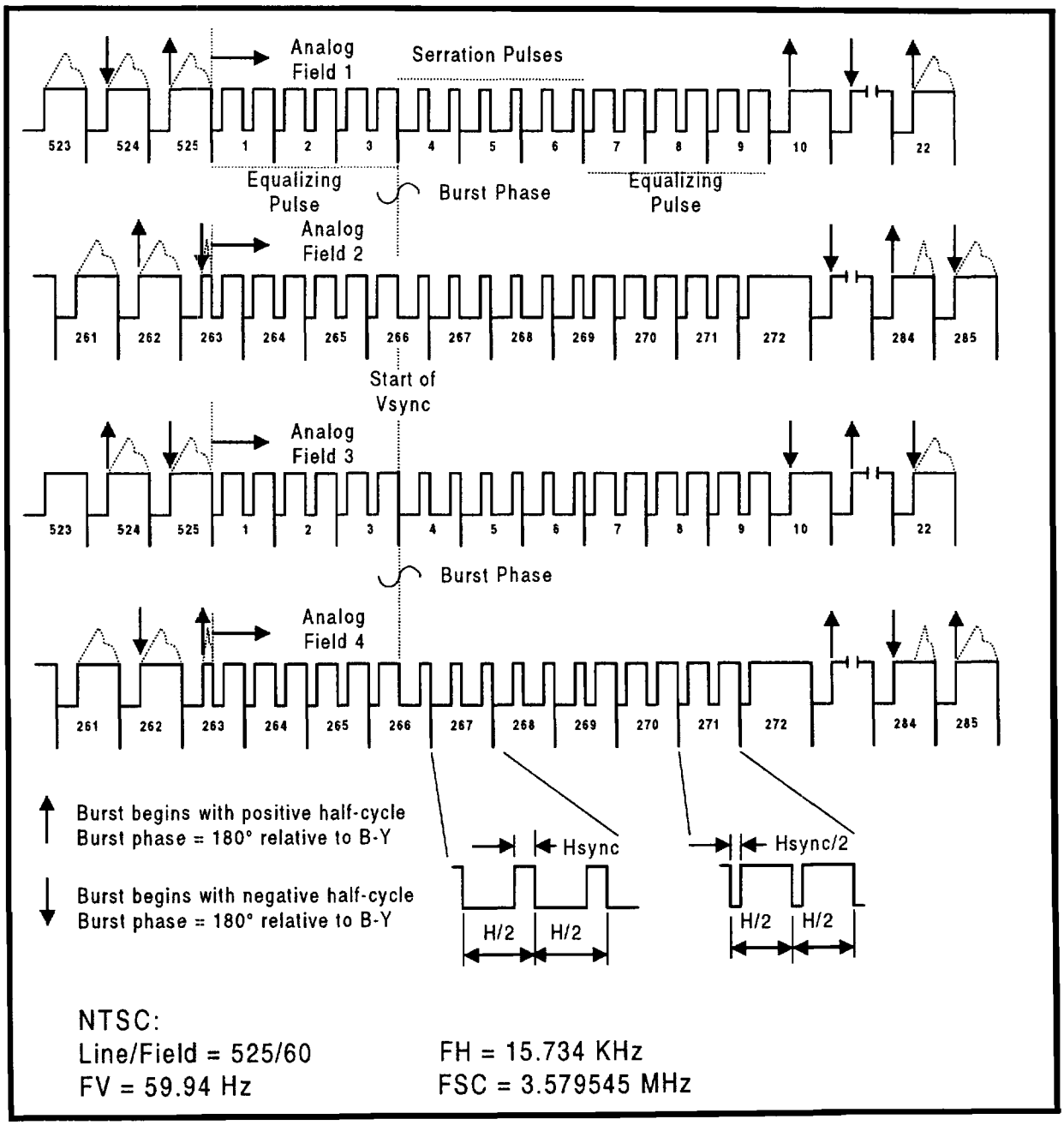

Figure 4-10. Four-field NTSC Format and Burst Blanking

4.4.10.2 PAL TV Timing

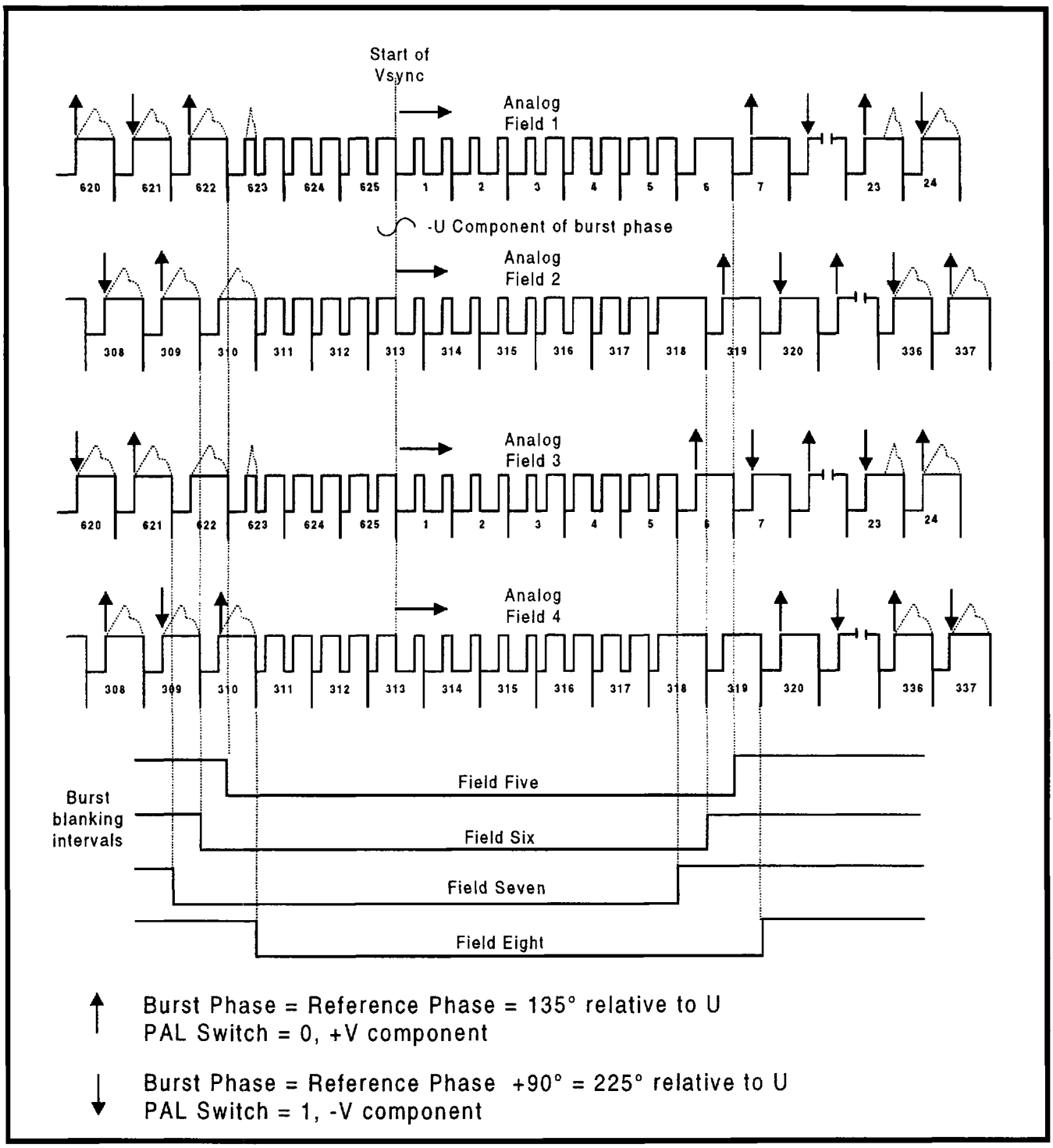

Figure 4-11. Eight-field PAL Format

5. Configuration Table

5.1. Video Modes

The following information describes various video modes which include:

- Standard Video Modes
- Extended Video Modes
- Video Mode Cross Reference

Table 5-1. Standard Mode Support

Mode #	Resolution-Colors	Pixel Freq	Hor Freq	Vert Freq	Mem	Addr	Text Res	Font	Type	Feature
0H,1H	320x200-16	28	31.4	70	All	B800	40x25	8x8	Text	NI,N,P
2H,3H	640x200-16	28	31.4	70	All	B800	80x25	8x8	Text	NI,N,P
4H, 5H	320x200-4	25	31.4	70	All	B800	40x25	8x8	Graph	NI,N,P
6H	640x200-2	25	31.4	70	All	B800	80x25	8x8	Graph	NI,N,P
7H	720x350-Mono	28	31.5	70	All	B000	80x25	9x14	Text	NI,N,P
DH	320x200-16	25	31.4	70	All	A000	40x25	8x8	Graph	NI,N,P
EH	640x200-16	25	31.4	70	All	A000	80x25	8x8	Graph	NI,N,P
FH	640x350-mono	28	31.4	70	All	B000	80x25	8x14	Graph	NI,N,P
10H	640x350-16	25	31.4	70	All	A000	80x25	8x14	Graph	NI,N,P
11H	640x480-2	25	31.4	60	All	A000	80x30	8x16	Graph	NI,N,P
12H	640x480-16	25	31.4	60	All	A000	80x30	8x16	Graph	NI,N,P
13H	320x200-256	25	31.4	70	All	A000	40x25	8x8	Graph	NI,N,P

Note: Refresh rates for Table 5-1 are located at the end of Table 5-4.

Features: NI - non-interlaced VGA display
I - interlaced VGA display
N - NTSC TV display (VGA monitor and TV display switching)
P - PAL TV display (VGA monitor and TV display switching)

Table 5-2. Extended Mode Support

Mode #	Resolution/ Colors	Pixel Freq	Hor Freq	Vert Freq	Mem	Addr	Text Res	Font	Type	Feature
50H	640x480-16	25	31.5	60	All	B800	80x30	8x16	Text	NI,N,P
51H	640x473-16	25	31.5	60	All	B800	80x43	8x8	Text	NI,N,P
52H	640x480-16	25	31.5	60	All	B800	80x60	8x8	Text	NI,N,P
53H	1056x350-16	40	31.3	70	All	B800	132x25	8x14	Text	NI
54H	1056x480-16	40	31.3	60	All	B800	132x30	8x16	Text	NI
55H	1056x473-16	40	31.3	60	All	B800	132x43	8x8	Text	NI
56H	1056x480-16	40	31.3	60	All	B800	132x60	8x8	Text	NI
57H	1188x350-16	45	31.3	70	512K	B800	132x25	9x14	Text	NI
58H	1188x480-16	45	31.3	60	512K	B800	132x30	9x16	Text	NI
59H	1188x473-16	45	31.3	60	512K	B800	132x43	8x8	Text	NI
5AH	1188x480-16	45	31.3	60	512K	B800	132x60	8x8	Text	NI
5BH_1	800x600-16	40	37.9	60	All	A000	100x75	8x8	Graph	NI,P
5BH_2	800x600-16	49.5	46.9	75	512K	A000	100x75	8x8	Graph	NI,P
5BH_3	800x600-16	56.3	53.7	85	512K	A000	100x75	8x8	Graph	NI,P
5CH	640x400-256	25	31.6	70	1M	A000	80x25	8x16	Graph	NI,N,P
5DH_1	640x480-256	25	31.5	60	512K	A000	80x30	8x16	Graph	NI,N,P
5DH_2	640x480-256	31.5	37.9	72	512K	A000	80x30	8x16	Graph	NI,N,P
5DH_3	640x480-256	31.5	37.5	75	512K	B800	80x60	8x16	Graph	NI
5DH_4	640x480-256	36	43.3	85	512K	B800	80x60	8x16	Graph	NI
5EH_1	800x600-256	40	37.9	60	512K	A000	100x37	8x16	Graph	NI,P
5EH_2	800x600-256	49.5	46.9	75	512K	A000	100x37	8x16	Graph	NI,P
5EH_3	800x600-256	56.3	53.7	85	512K	A000	100x37	8x16	Graph	NI,P
5FH_1	1024x768-16	45	35.5	87i	512K	A000	128x48	8x16	Graph	I
5FH_2	1024x768-16	65	48.5	60	512K	A000	128x48	8x16	Graph	NI
5FH_3	1024x768-16	75	56.5	70	512K	A000	128x48	8x16	Graph	NI
5FH_4	1024x768-16	78.8	60	75	512K	A000	128x48	8x16	Graph	NI
5FH_5	1024x768-16	94.5	67.9	85	512K	A000	128x48	8x16	Graph	NI
62H_1	1024x768-256	45	35.5	87i	1M	A000	128x48	8x16	Graph	I
62H_2	1024x768-256	65	48.5	60	1M	A000	128x48	8x16	Graph	NI
62H_3	1024x768-256	75	56.5	70	1M	A000	128x48	8x16	Graph	NI
62H_4	1024x768-256	80	59.5	75	1M	A000	128x48	8x16	Graph	NI
62H_5	1024x768-256	94	68.7	85	1M	A000	128x48	8x16	Graph	NI
63H_1	1280X1024-16	75	46.9	87i	1M	A000	160X64	8X16	Graph	I
63H_2	1280X1024-16	108	63.0	60	1M	A000	160X64	8X16	Graph	NI
63H_3	1280X1024-16	135	80	75	1M	A000	160X64	8X16	Graph	NI
64H_1	1280X1024-256	75	46.9	87i	2M	A000	160X64	8X16	Graph	I
64H_2	1280x1024-256	108	63.0	60	2M	A000	160x64	8x16	Graph	NI

Table 5-2. Extended Mode Support (Cont'd)

Mode #	Resolution/ Colors	Pixel Freq	Hor Freq	Vert Freq	Mem	Addr	Text Res	Char	Type	Feature
64H_3	1280x1024-256	135	80.0	75	2M	A000	160x64	8x16	Graph	NI
65H_1	1600x1200-16Ci	135	62.5	96i	1M	A000	200x75	8x16	Graph	Ni
65H_2	1600x1200-16C	162	75	60	1M	A000	200x75	8x16	Graph	NI
66H_1	1600x1200-256Ci	135	62.5	96i	2M	A000	200x75	8x16	Graph	NI
66H_2	1600x1200-256C	162	75	60	2M	A000	200x75	8x16	Graph	NI
6AH	800x600-16	40	35.2	60	All	A000	100x75	8x8	Graph	NI,P
6BH	640x400-T	25	31.6	70	1M	A000	40x25	8x8	Graph	NI,N,P
6CH_1	640x480-T	50	31.5	60	1M	A000	80x30	8x16	Graph	NI,N,P
6CH_2	640x480-T	31.5	37.9	72	1M	A000	80x30	8x16	Graph	NI,N,P
6CH_3	640x480-T	31.5	37.5	75	1M	A000	80x30	8x16	Graph	NI,N,P
6CH_4	640x480-T	36	43.3	85	1M	A000	80x30	8x16	Graph	NI
6DH_1	800x600-T	40	37.9	60	2M	A000	200x74	8x16	Graph	NI,P
6DH_2	800x600-T	49.5	46.9	75	2M	A000	200x74	8x16	Graph	NI,P
6DH_3	800x600-T	56.3	53.7	85	2M	A000	200x74	8x16	Graph	NI,P
6EH_1	1024x768-T	45	35.5	87i	4M	A000	128x48	8x16	Graph	I
6EH_2	1024x768-T	65	48.4	60	4M	A000	128x48	8x16	Graph	NI
6EH_3	1024x768-T	75	56.4	70	4M	A000	128x48	8x16	Graph	NI
6EH_4	1024x768-T	78	60	75	4M	A000	128x48	8x16	Graph	NI
6EH_5	1024x768-T	94.5	67.9	85	4M	A000	128x48	8x16	Graph	NI
72H	640x400-32k	25	31.4	70	512K	A000	64x30	8x16	Graph	NI,N,P
73H	640x400-64k	25	31.4	70	512K	A000	64x30	8x16	Graph	NI,N,P
74/5H_1	640x480-32/64K	25	31.4	60	1M	A000	80x30	8x16	Graph	NI,N,P
74/5H_2	640x480-32/64K	25	37.9	72	1M	A000	80x30	8x16	Graph	NI,N,P
74/5H_3	640x480-32/64K	31.5	37.5	75	1M	A000	80x30	8x16	Graph	NI,N,P
74/5H_4	640x480-32/64K	36	43.3	85	1M	A000	80x30	8x16	Graph	NI,N,P
76/7H_1	800x600-32/64K	40	37.9	60	1M	A000	200x37	8x16	Graph	NI,P
76/7H_2	800x600-32/64K	49.5	46.9	75	1M	A000	200x37	8x16	Graph	NI,P
76/7H_3	800x600-32/64K	56.3	53.7	85	1M	A000	200x37	8x16	Graph	NI,P
78/9H_1	1024x768-32/64K	44.9	35.5	87i	2M	A000	128x96	8x16	Graph	I
78/9H_2	1024x768-32/64K	65	48.4	60	2M	A000	128x96	8x16	Graph	I
78/9H_3	1024x768-32/64K	78	60.0	75	2M	A000	128x96	8X16	Graph	NI
78/9H_4	1024x768-32/64K	94	68.7	85	2M	A000	128x96	8X16	Graph	NI
7BH_1	1280x1024-64K	78	46.4	87i	4M	A000	160x128	8x16	Graph	I
7BH_2	1280x1024-64K	108	63.9	60	4M	A000	160x128	8x16	Graph	I
7BH_3	1280x1024-64K	135	80	75	4M	A000	160x128	8x16	Graph	I
7BH_4	1280x1024-64K	157.5	84.8	85	4M	A000	160x128	8x16	Graph	I

Note: In all of the tables showing display modes in this TRM, 32K Color mode can only be supported in a DOS environment.

Table 5-3. Extended Mode Support Yet to be Developed

Mode #	Resolution: Colors	Pixel Freq	Hor Freq	Vert Freq	Mem	Addr	Text Res	Font	Type	Feature
7EH	320x200-32K	25	31.4	70	512K	A000	40x25	8x8	Graph	NI,N,P
7FH	320x200-64K	25	31.4	70	512K	A000	40x25	8x8	Graph	NI,N,P

Table 5-4. Monitor Groups for Tables 5-1 and 5-2

Horizontal Frequency[1]	640x400	640x480	800x600	1024x768	1280x1024	1600x1200
31K	70	60	56	87i	87i	87i
35K	70	60	60	87i	87i	87i
48K	70	75	75	60	87i	87i
57K	70	85	75	70	87i	87i
65K	70	95	85	75	60	87i
72K	70	95	85	85	60	87i
82K	70	95	95	95	60	87i
100K	70	95	95	95	60	87i

Note 1: Corresponds to maximum horizontal frequency supported by Monitor Group.

Features: NI - non-interlaced VGA display
I - interlaced VGA display
N - NTSC TV display (VGA monitor and TV display switching)
P - PAL TV display (VGA monitor and TV display switching)

Table 5-5. Graphic Resolutions and Color Depth Modes Supported

MODE	2MB DRAM	4MB DRAM
640x400-256, 8 bits/pixel	✔	✔
640x400-64k, 16 bits/pixel	✔	✔
640x400-16M, 24 bits/pixel	✔	✔
640x480-256, 8 bits/pixel	✔	✔
640x480-64k, 16 bits/pixel	✔	✔
640x480-16M, 24 bits/pixel	✔	✔
800x600-16, 4 bits/pixel	●	●
800x600-256, 8 bits/pixel	✔	✔
800x600-64k, 16 bits/pixel	✔	✔
800x600-16M, 24 bits/pixel	✔	✔
1024X768-16, 4 bits/pixel	●	●
1024X768-256, 8 bits/pixel	✔	✔
1024X768-64k, 16 bits/pixel	✔	✔
1024X768-16M, 24 bits/pixel		✔
1280x1024-16, 4 bits/pixel	●	●
1280x1024-256, 8 bits/pixel	✔	✔
1280x1024-64k, 16 bits/pixel		✔
1600x1200-16, 4 bits/pixel	●	●
1600x1200-256, 8 bits/pixel	✔	✔

Note: ● means "Supported ***but not*** accelerated by the graphics engine."
✔ means "Supported ***and*** accelerated by the graphics engine."

Table 5-6. Video Modes Supported for MPEG1 or TV-PAL with a Minify Factor = 2

	Bandwidth (Mbps)			2MB Embedded SGRAM	
Res., Color, Ref. Rate	Gm	Pm	Cm	66MHz (422)	83MHz (531)
640x480, 256C, 60Hz	25	22	13.5	GPC	GPC
640x480, 256C, 75Hz	31	27	13.5	GPC	GPC
640x480, 64KC, 60Hz	50	22	13.5	GPC	GPC
640x480, 64KC, 75Hz	65	27	13.5	GPC	GPC
640x480, 16MC, 60Hz	75	22	13.5	GPC	GPC
640x480, 16MC, 75Hz	98	27	13.5	GPC	GPC
800x600, 256C, 60Hz	40	27	13.5	GPC	GPC
800x600, 256C, 75Hz	50	33	13.5	GPC	GPC
800x600, 64KC, 60Hz	80	27	13.5	GPC	GPC
800x600, 64KC, 75Hz	100	33	13.5	GPC	GPC
800x600, 16MC, 60Hz	110	27	13.5	GP	GPC
800x600, 16MC, 75Hz	150	33	13.5	GC	GPC
1024x768, 256C, 60Hz	65	34	13.5	GPC	GPC
1024x768, 256C, 75Hz	78	42	13.5	GPC	GPC
1024x768, 64KC, 60Hz	130	34	13.5	GPC	GPC
1024x768, 64KC, 75Hz	158	42	13.5	GPC	GPC
1024x768, 16MC, 60Hz	195	34	13.5	GPC	GPC
1024x768, 16MC, 75Hz	236	42	13.5	GPC	GPC
1280x1024, 256C, 60Hz	108	45	13.5	GPC	GPC
1280x1024, 256C, 75Hz	135	56	13.5	GPC	GPC

Note: G = graphics supported
P = playback supported
C = capture supported

When the video minify function is used and then the reduced video is zoomed to restore the original image, the image quality is degraded since the video pixels are discarded or artificially introduced.

Table 5-7. Video Modes Supported for MPEG2 or TV-PAL

	Bandwidth (Mbps)			2MB Embedded SGRAM	
Res, Color, Ref Rate	Gm	Pm	Cm	66MHz (422)	83MHz (531)
640x480, 256C, 60Hz	25	44	27	GPC	GPC
640x480, 256C, 75Hz	31	53	27	GPC	GPC
640x480, 64KC, 60Hz	50	44	27	GPC	GPC
640x480, 64KC, 75Hz	65	53	27	GPC	GPC
640x480, 16MC, 60Hz	75	44	27	GPC	GPC
640x480, 16MC, 75Hz	98	53	27	GPC	GPC
800x600, 256C, 60Hz	40	53	27	GPC	GPC
800x600, 256C, 75Hz	50	66	27	GPC	GPC
800x600, 64KC, 60Hz	80	53	27	GPC	GPC
800x600, 64KC, 75Hz	100	66	27	GPC	GPC
800x600, 16MC, 60Hz	110	53	27	GPC	GPC
800x600, 16MC, 75Hz	150	66	27	GPC	GPC
1024x768, 256C, 60Hz	65	65	27	GPC	GPC
1024x768, 256C, 75Hz	78	80	27	GPC	GPC
1024x768, 64KC, 60Hz	130	65	27	GPC	GPC
1024x768, 64KC, 75Hz	158	80	27	GPC	GPC
1024x768, 16MC, 60Hz	195	65	27	N/A	N/A
1024x768, 16MC, 75Hz	236	80	27	N/A	N/A
1280x1024, 256C, 60Hz	108	90	27	GPC	GPC
1280x1024, 256C, 75Hz	135	113	27	GPC	GPC

Note: G = graphics supported
P = playback supported
C = capture supported

When the video minify function is used and then the reduced video is zoomed to restore the original image, the image quality is degraded since the video pixels are discarded or artificially introduced.

5.2. Standard Modes Supported for TV Output

Table 5-8. Standard Modes for TV Output

Mode #	Resolution: Color	Pixel Freq	Hor Freq	TV Standard	Vert Freq	Mem Req	Page #	Mode Type	TV 640x480	TV 800x600
0H,1H	320x200-16	28	31.4	NTSC	60	1M	8	Text	✔	
2H,3H	640x200-16	28	31.4	NTSC	60	1M	8	Text	✔	
4H,5H	320x200-4	25	31.4	NTSC	60	1M	1	Graph	✔	
6H	640x200-2	25	31.4	NTSC	60	1M	1	Graph	✔	
7H	720x350-mono	28	31.4	NTSC	60	1M	8	Text	✔	
DH	320x200-16	25	31.4	NTSC	60	1M	8	Graph	✔	
EH	640x200-16	25	31.4	NTSC	60	1M	4	Graph	✔	
FH	640x350-mono	28	31.4	NTSC	60	1M	2	Graph	✔	
10H	640x350-16	25	31.4	NTSC	60	1M	2	Graph	✔	
11H	640x480-2	25	31.4	NTSC	60	1M	1	Graph	✔	
12H	640x480-16	25	31.4	NTSC	60	1M	2	Graph	✔	
13H	320x200-256	25	31.4	NTSC	60	1M	1	Graph	✔	
0H,1H	320x200-16	28	31.4	PAL	50	1M	8	Text	✔	✔
2H,3H	640x200-16	28	31.4	PAL	50	1M	8	Text	✔	✔
4H,5H	320x200-4	25	31.4	PAL	50	1M	1	Graph	✔	✔
6H	640x200-2	25	31.4	PAL	50	1M	1	Graph	✔	✔
7H	720x350-mono	28	31.4	PAL	50	1M	8	Text	✔	✔
DH	320x200-16	25	31.4	PAL	50	1M	8	Graph	✔	✔
EH	640x200-16	25	31.4	PAL	50	1M	4	Graph	✔	✔
FH	640x350-mono	28	31.4	PAL	50	1M	2	Graph	✔	✔
10H	640x350-16	25	31.4	PAL	50	1M	2	Graph	✔	✔
11H	640x480-2	25	31.4	PAL	50	1M	1	Graph	✔	✔
12H	640x480-16	25	31.4	PAL	50	1M	2	Graph	✔	✔
13H	320x200-256	25	31.4	PAL	50	1M	1	Graph	✔	✔

5.3. Extended Modes Supported for TV Output

Table 5-9. Extended Modes for TV Output

Mode #	Resolution-Color	Pixel Freq	Hor Freq	TV Standard	Vert Freq	Mem Req	Mode Type	TV 640x480	TV 800x600
5CH	640x400-256	25	31.6	NTSC	60	1M	Graph	✔	
5DH	640x480-256	25	31.4	NTSC	60	1M	Graph	✔	
74/5H	640x480-64k	25	31.4	NTSC	60	1M	Graph	✔	
6CH	640x480-T	50	31.4	NTSC	60	1M	Graph	✔	
5CH	640x400-256	25	31.6	PAL	50	1M	Graph	✔	✔
5DH	640x480-256	25	31.4	PAL	50	1M	Graph	✔	✔
74/5H	640x480-64k	25	31.4	PAL	50	1M	Graph	✔	✔
6CH	640x480-T	50	31.4	PAL	50	1M	Graph	✔	✔
5EH	800x600-256	40	31.4	PAL	50	1M	Graph	✔	✔
76/7H	800x600-64k	40	31.4	PAL	50	1M	Graph	✔	✔
6DH	800x600-T	80	31.4	PAL	50	2M	Graph	✔	✔

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6. Pin Description

The following listed sections describe signal references.

- PCI Bus Interface
- Memory Interface
- Clock Interface
- Flat Panel Display
- CRT and External Encoder
- Video, External Encoder, and Test
- Power Management
- Power Supply
- I/O Type Definitions

6.1 Signals

The Cyber9388 supports VESA DDC, VAFC, and a simplified DRAM interface. In order to utilize DDC, and VAFC interface or the simplified DRAM interface, OEM manufacturers must re-layout their PCB. Table 6-1 describes the pin assignments for the Cyber9388.

Table 6-1. PCI Bus Interface Signals

Pin Name	Type	Pin No	Description
C/BE[3:0]#	I/O	232, 234, 236, 237	C/BE0#: Bus Command and Byte Enable. During the address phase, C/BE#[3:0] define the bus command. During the data phase, they are used as byte enable.
AD[31:0]	I/O	16-20, 22-30, 33-40, 43-50, 52-53	AD[31:0]: Multiplexed address and data bus. During the first clock of a transaction, AD[31:0] is a physical byte address. During subsequent clock, AD[31:0] contains data. Little-endian byte ordering is used. AD[7:0] define the least significant byte and AD[31:24] define the most significant byte. When RESET# is asserted, AD[31:0] signals are not driven and tri-stated.
FRAME#	I/O	230	FRAME#: PCI cycle frame. It indicates the beginning and duration of an access.
PAR	I/O	231	PAR: Calculated Parity. PAR is the even parity bit and is calculated base on AD[31:0] and C/BE#[3:0], regardless of the byte enable signals. During reset, this signal is tri-stated.
STOP#	I/O	229	STOP#: Stop signal. It is to notify the initiator to terminate the current transaction. During reset, it is tri-stated.
IRDY#	I/O	227	IRDY#: Initiator Ready. This signal is used together with TRDY# to complete a data transaction.
DEVSEL#	I/O	226	DEVSEL#: Device Select Acknowledge. This signal responds to the host for being selected. It is tri-stated during reset.
TRDY#	I/O	228	TRDY#: Target Ready. This signal is used together with IRDY# to complete a data transaction. This signal is enabled when a transaction is asserted and remained asserted for additional a half CLK after the transaction is completed. It is tri-stated during reset. It is an input signal during DAC snooping after which the actual DAC write is performed.
INTR#	t/s	225	INTR#: CPU Interrupt. It signals the CPU that either the graphic source or the video source has an interrupt that needs to be serviced. During reset, this signal is tri-stated (low asserted, level sensitive).
PCICLK	I	224	CLK: All PCI interface signals are based on the rising edge of this system CLK.
IDSEL	I	238	Initialization Device Select. It is used as a chip select during configuration transactions.
BREQ#	t/s	239	Output request signal in bus master operation and is tri-stated during power up.
BGNT#	I	240	Input grant signal in bus master operation.
RESET#	I	235	RESET# System Reset forces the chip to a known state
ROMCS#	O	54	ROM chip select enable

Table 6-2. Memory Interface Signals

Pin Name	Type	Pin Number	Description
MA[8:0]	I/O	100-102, 106-111	SDRAM Memory Address bits [8:0]
MD[63:0]	I/O	55-59, 61-64,68-71, 74-80, 82-88, 90-94, 136-142, 144, 146-154, 156-163, 165-171	Display memory data bus. MD[31:16] are also used as BIOS address, ROMA[15:0], and MD[7:0] as ROM data.
DQM[7:0]	I/O	96-99, 122-125	SDRAM Input/Output Mask.
SDMCLK	I/O	104	SDRAM Clock
BA	t/s	112	Band Address of SDRAM
CKE	I/O	118	SDRAM Clock Enable
RAS#, CAS#, WE#	I/O	115, 116, 119	SDRAM Command Input
MTEST	I	120	Test Pin

Table 6-3. Clock Interface Signals

Pin Name	Type	Pin Number	Description
REFCLK	I	126	32KHz clock for lower power refresh during suspend.
MLF	OA	204	MCLK low pass filter for internal clock synthesizer.
VLF1	OA	206	The First VCLK low pass filter for internal clock synthesizer.
VLF2	OA	209	The Second VCLK low pass filter for internal clock synthesizer.
XTLI	IA	200	External crystal pin. If a crystal is used, it is connected across XTLI and XTLO (14.318MHz).
XTLO	OA	201	External crystal pin. If a crystal is used, it is connected across XTLI and XTLO (14.318MHz).

Table 6-4. Flat Panel Display Signals

Pin Name	Type	Pin Number	Description
P[35:0]	O	5-6, 10-13, 172-175, 177-181, 213-216, 218, 220-223, 245-246, 248-253, 259-262	Flat panel pixel data. See table for mappings to various panels.
MOD	O	14	AC modulation signal for DSTNs
SHIFT/SCLK	O	8	Shift clock for DSTN and TFT LCDs
S1	O	10	Half rate shift clock phase-1 for TFTs requiring double pixels per clock
S2	O	11	Half rate shift clock phase-2 for TFTs requiring double pixels per clock
LP	O	7	Flat panel line pulse in DSTN panels
FLM	O	15	First line marker in DSTN panels
PHS	O	7	Flat panel horizontal sync in TFT panels
PVS	O	15	Flat panel vertical sync in TFT panels
DEN	O	14	Panel display enable in TFT panels

Table 6-5. CRT and External Encoder Signals

Pin Name	Type	Pin Number	Description
CHS	I/O	198	CRT horizontal sync
CVS	I/O	199	CRT vertical sync
R	O	266	DAC red output
G	O	267	DAC green output
B	O	268	DAC blue output
IRSET	I	2	Resister to ground input to set full scale output of RGB. The value of the resistor between IRSET and VSS is on the schematic example.
DACCOMP	I	264	DAC Compensation Capacitor input.

Table 6-6. Video, External Encoder, and Test Signals

Pin Name	Type	Pin Number	Description
COMPSYNC	t/s	254	Encoder composite sync
SUBCCLK	t/s	255	Encoder subcarrier clock
BLANK#	I/O	197	This pin can be programmed as output for external DAC or video. It also can function as input for signature generation on test floor.
PCLK	I	193	Test pixel clock for test modes
DCLK	O	193	When a VAFC interface is required, this pin may be used as DCLK.
VCLK	I	195	When a VAFC interface is required, this pin may be used as input clock VCLK driven from the video system to graphics system.
VP[15:0]	I	54, 65-67, 129, 134-135, 183-188, 190-191, 256	VAFC/Capture/ZV data port in. 16 bit data may also be brought in on VP[7:0].
EVIDEO#	I/O	194	Enable video data when used in VAFC/FC.
EDCLK#/EVCLK/ OBSCLK	I/O	196	Enable video clock; or external VCLK input when external clock synthesizer is used; or VCLK/MCLK for observing internal VCLK/MCLK when testing on-chip clock synthesizer.
ESYNC#	I	195	Enable sync signal; or VCLK for advanced feature connector video clock.
SDA	I/O	243	I^2C signal
SCL	I/O	244	I^2C signal
CAPD[7:0]	I	183-188, 190-191	Video module interface data bus
VMID [7:0]	I/O	54, 65-67, 129, 134-135, 256	Video module interface data bus.
VMIRD#	O	241	VMI read strobe.
VMIWR#	O	127	VMI write strobe.
VMICS#	O	195	VMI chip select.
VMITRDY	I	194	VMI ready signal.

Table 6-7. Power Management Signals

Pin Name	Type	Pin Number	Description
STANDBY PWRDWN	I	256	STNDBY: Standby state enable (default active high). PWRDWN is same as STNDBY. The functionality may be configured to the application.
SUSPEND	I	128	SUSPEND: Suspended state enable (default active high)
PSTATUS	O	225	Power status (default active high)
ENPBLT	I/O	131	This pin can be configured as flat panel backlight enable or flat panel display ON/OFF control. (default active high)
ENPVDD	O	133	Flat panel power VDD enable (active high).
ENPVEE	O	132	Flat panel power VEE enable (active high).
GPIO[7:0]	I/O I/OT	127, 129, 131, 241-244, 263	General purpose input/output pins
BIST_ON	I/O	127	Built-In-Self-Test
PWM [2:1]	O	243, 244	Pulse width modulation signal for analog adjustment voltage on GPIOs

Table 6-8. Power Signals

Pin Name	Type	Pin Number	Description
AVDD[5:1]	PWR	1, 202, 207, 210,	Analog VDD. Same voltage level as VDDC. (No AVDD4)
AVSS[5:1]	GND	3, 203, 205, 208,265	Analog VSS.
V5SF	PWR	73	5V supply input for 5V-only or mixed-voltage environments.
VDD	PWR	9, 21, 41, 42, 155, 176, 189, 211, 217, 257, 258	Logic power supply VDD.
VCCA1/2, VCCPW1/2, VCCP1/2	PWR	72, 95, 113, 114, 130, 143	For memory interface I/O signals.
VSS	GND	4, 31, 32, 51, 60, 145, 164, 182, 192, 212, 219, 233, 247	Logic ground
VSSA1/2 VSSQ1/2 VSSP1/2	GND	81, 89, 103, 105, 117, 121	For memory interface I/O signals.
T/G (G2)	GND	269-290	Thermal ground connected to Ground Ring #2.
T/G (G1)	GND	291-292	Thermal ground connected to Ground Ring #1.

Table 6-9. I/O Type Definitions

Buffer Type	Description
A	Analog
I	Input
IU	Input with internal passive pull up
O	Output
t/s	Tri-state
PWR	Power
GND	Ground

6.2 Pin Assignments

The Cyber9388 is packaged in a 292 BGA. Starting with pin A1 at the corner of the mold gate, the pin assignment is listed in Table 6-10. Multiple function names are listed for completeness.

Buffer types are listed. Some pins can tolerate a 5V input even if the pin's power bus is at 3V. These pins are called 5V tolerant or 5V safe. They are indicated below.

The table below lists the bottom, right, top, and left sides of the package. The table also lists the VDD source for mixed voltage output signals. All input signals are powered by VDD.

Table 6-10. Cyber9388 Pin Assignments

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
1	U18	AVDD5	(vddc level)				
2	U17	IRSET			Analog	NBUFT	
3	T17	AVSS5					
4	L9	VSS	***TFT CONFIG:***				
5	Y20	P23			t/s	BT10_3V	
6	W20	P22			t/s	BT10_3V	
7	W19	LP	PHS		t/s	BT10_3V	
8	V19	SHIFT	SHIFT		t/s	BT10_3V	
9	R17	VDD					
10	V20	P18			t/s	BT10_3V	
11	U19	P19			t/s	BT10_3V	
12	U20	P20			t/s	BT10_3V	
13	T18	P21			t/s	BT10_3V	
14	T19	MOD	DEN		t/s	BT10_3V	
15	T20	FLM	PVS		t/s	BT10_3V	
16	R18	AD31			I/O	BDT10_5S	
17	R19	AD30			I/O	BDT10_5S	
18	R20	AD29			I/O	BDT10_5S	
19	P18	AD28			I/O	BDT10_5S	
20	P19	AD27			I/O	BDT10_5S	
21	P17	VDD					
22	N17	AD26			I/O	BDT10_5S	
23	P20	AD25			I/O	BDT10_5S	
24	N18	AD24			I/O	BDT10_5S	
25	N19	AD23			I/O	BDT10_5S	
26	N20	AD22			I/O	BDT10_5S	
27	M17	AD21			I/O	BDT10_5S	
28	M18	AD20			I/O	BDT10_5S	
29	M19	AD19			I/O	BDT10_5S	
30	M20	AD18			I/O	BDT10_5S	
31	N9	VSS					
32	N13	VSS					
33	L19	AD17			I/O	BDT10_5S	
34	L20	AD16			I/O	BDT10_5S	

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
35	K17	AD15			I/O	BDT10_5S	
36	K18	AD14			I/O	BDT10_5S	
37	K19	AD13			I/O	BDT10_5S	
38	K20	AD12			I/O	BDT10_5S	
39	J18	AD11			I/O	BDT10_5S	
40	J19	AD10			I/O	BDT10_5S	
41	J17	VDD					
42	H17	VDD					
43	J20	AD9			I/O	BDT10_5S	
44	H18	AD8			I/O	BDT10_5S	
45	H19	AD7			I/O	BDT10_5S	
46	H20	AD6			I/O	BDT10_5S	
47	G18	AD5			I/O	BDT10_5S	
48	G19	AD4			I/O	BDT10_5S	
49	G20	AD3			I/O	BDT10_5S	
50	G17	AD2			I/O	BDT10_5S	
51	N8	VSS					
52	F19	AD1			I/O	BDT10_5S	
53	F20	AD0		***ROM:***	I/O	BDT10_5S	
54	F18	VP9	VMID1	ROMCS#	I/O	BDT6U_5S	
55	F17	MD31		ROMA15	I/O	BDT6UMD_5S	
56	E19	MD30		ROMA14	I/O	BDT6UMD_5S	
57	E20	MD29		ROMA13	I/O	BDT6UMD_5S	
58	E18	MD28		ROMA12	I/O	BDT6UMD_5S	
59	D20	MD27		ROMA11	I/O	BDT6UMD_5S	
60	M11	VSS					
61	D19	MD26		ROMA10	I/O	BDT6UMD_5S	
62	D18	MD25		ROMA9	I/O	BDT6UMD_5S	
63	C20	MD24		ROMA8	I/O	BDT6UMD_5S	
64	C19	MD23		ROMA7	I/O	BDT6UMD_5S	
65	B20	VP10	VMID2		I/O	BDT10_5S	
66	B19	VP11	VMID3		I/O	BDT10_5S	
67	A19	VP12	VMID4		I/O	BDT10_5S	
68	D17	MD22		ROMA6	I/O	BDT6UMD_5S	
69	C18	MD21		ROMA5	I/O	BDT6UMD_5S	
70	B18	MD20		ROMA4	I/O	BDT6UMD_5S	
71	A18	MD19		ROMA3	I/O	BDT6UMD_5S	
72	E17	VCCA2					
73	A20	V5SF					
74	C17	MD18		ROMA2	I/O	BDT6UMD_5S	
75	B17	MD17		ROMA1	I/O	BDT6UMD_5S	
76	A17	MD16	***DRAM TEST:***	ROMA0	I/O	BDT6UMD_5S	

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
77	D16	MD15	MTMD7		I/O	BDT6UMD_5S	
78	C16	MD14	MTMD6		I/O	BDT6UMD_5S	
79	B16	MD13	MTMD5		I/O	BDT6UMD_5S	
80	A16	MD12	MTMD4		I/O	BDT6UMD_5S	
81	H13	VSSA2					
82	D15	MD11	MTMD3		I/O	BDT6UMD_5S	
83	C15	MD10	MTMD2		I/O	BDT6UMD_5S	
84	B15	MD9	MTMD1		I/O	BDT6UMD_5S	
85	A15	MD8	MTMD0		I/O	BDT6UMD_5S	
86	D14	MD7	ERRORB	ROMD7	I/O	BDT6UMD_5S	
87	C14	MD6	DIAG	ROMD6	I/O	BDT6UMD_5S	
88	B14	MD5		ROMD5	I/O	BDT6UMD_5S	
89	H12	VSSQ2					
90	D13	MD4	MTRAS1#	ROMD4	I/O	BDT6UMD_5S	
91	C13	MD3	MTCAS1#	ROMD3	I/O	BDT6UMD_5S	
92	B13	MD2	MTWE1#	ROMD2	I/O	BDT6UMD_5S	
93	A13	MD1		ROMD1	I/O	BDT6UMD_5S	
94	C12	MD0	MTRESET	ROMD0	I/O	BDT6UMD_5S	
95	D12	VCCPW2					
96	B12	DQM3	MTDQM3		I/O	BDT8_5S	
97	A12	DQM2	MTDQM2		I/O	BDT8_5S	
98	D11	DQM1	MTDQM1		I/O	BDT8_5S	
99	C11	DQM0	MTDQM0		I/O	BDT8_5S	
100	B11	MA0	MTMA0		I/O	BDT8_5S	
101	A11	MA1	MTMA1		I/O	BDT8_5S	
102	D10	MA2	MTMA2		I/O	BDT8_5S	
103	H10	VSSP2					
104	B10	SDMCLK	MTMCK		I/O	BDT10_5S	
105	J9	VSSP1					
106	A10	MA3	MTMA3		I/O	BDT8_5S	
107	D9	MA4	MTMA4		I/O	BDT8_5S	
108	C9	MA5	MTMA5		I/O	BDT8_5S	
109	B9	MA6	MTMA6		I/O	BDT8_5S	
110	A9	MA7	MTMA7		I/O	BDT8_5S	
111	C8	MA8	MTMA8		I/O	BDT8_5S	
112	D6	BA			I/s	BT10_5S	
113	D8	VCCP2					
114	D7	VCCP1					
115	B8	WE#	MTWE0#		I/O	BDT10_5S	VDDM
116	A8	RAS#	MTRAS0#		I/O	BDT10_5S	VDDM
117	H9	VSSQ1					VDDM
118	A7	CKE	MTCKE		I/O	BDT10_5S	VDDM

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
119	B7	CAS#	MTCAS0#		I/O	BDT10_5S	VDDM
120	C7	MTEST			IN	IBUFT_5S	VDDM
121	J8	VSSA1					
122	B6	DQM4	MTDQM4		I/O	BDT8_5S	VDDM
123	A6	DQM5	MTDQM5		I/O	BDT8_5S	VDDM
124	C6	DQM6	MTDQM6		I/O	BDT8_5S	VDDM
125	B5	DQM7	MTDQM7		I/O	BDT8_5S	VDDM
126	A5	REFCLK	MTEST2		IN	IBUFT_5S	VDDM
127	C5	GPIO7	BIST_ON		I/O	BDT6_5S	
128	B4	SUSPEND	DOUBLE		IN	IBUFT_5S	
129	A4	VP13	VMID5	GPIO5	I/O	BDT6_5S	VDDM
130	D5	VCCPW1					
131	B3	ENPBLT	MTEST1	GPIO0	I/O	BDT6_5S	VDDM
132	A3	ENPVEE			t/s	BT6_5S	VDDM
133	A2	ENPVDD			t/s	BT6_5S	VDDM
134	C4	VP14	VMID6		I/OS	BDT10_5S	
135	D3	VP15	VMID7		I/O	BDT10_5S	
136	A1	MD32			I/O	BDT6UMD_5S	
137	B2	MD33			I/O	BDT6UMD_5S	
138	B1	MD34			I/O	BDT6UMD_5S	
139	C3	MD35			I/O	BDT6UMD_5S	
140	C2	MD36			I/O	BDT6UMD_5S	
141	C1	MD37			I/O	BDT6UMD_5S	
142	D2	MD38			I/O	BDT6UMD_5S	
143	D4	VCCA1					
144	D1	MD39			I/O	BDT6UMD_5S	
145	L11	VSS					
146	E4	MD40			I/O	BDT6UMD_5S	
147	E3	MD41			I/O	BDT6UMD_5S	
148	E2	MD42			I/O	BDT6UMD_5S	
149	E1	MD43			I/O	BDT6UMD_5S	
150	F4	MD44			I/O	BDT6UMD_5S	
151	F3	MD45			I/O	BDT6UMD_5S	
152	F2	MD46			I/O	BDT6UMD_5S	
153	F1	MD47			I/O	BDT6UMD_5S	
154	G3	MD48			I/O	BDT6UMD_5S	
155	G4	VDD					
156	G2	MD49			I/O	BDT6UMD_5S	
157	G1	MD50			I/O	BDT6UMD_5S	
158	H4	MD51			I/O	BDT6UMD_5S	
159	H3	MD52			I/O	BDT6UMD_5S	
160	H2	MD53			I/O	BDT6UMD_5S	

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
161	H1	MD54			I/O	BDT6UMD_5S	
162	J4	MD55			I/O	BDT6UMD_5S	
163	J3	MD56			I/O	BDT6UMD_5S	
164	L10	VSS					
165	J1	MD57			I/O	BDT6UMD_5S	
166	K4	MD58			I/O	BDT6UMD_5S	
167	K3	MD59			I/O	BDT6UMD_5S	
168	K2	MD60			I/O	BDT6UMD_5S	
169	K1	MD61			I/O	BDT6UMD_5S	
170	L4	MD62			I/O	BDT6UMD_5S	
171	L3	MD63			I/O	BDT6UMD_5S	
172	L2	P0			t/s	BT10_3V	
173	L1	P1			t/s	BT10_3V	
174	M3	P2			t/s	BT10_3V	
175	M2	P3			t/s	BT10_3V	
176	M4	VDD					
177	M1	P4			t/s	BT10_3V	
178	N4	P5			t/s	BT10_3V	
179	N3	P6			t/s	BT10_3V	
180	N2	P7			t/s	BT10_3V	
181	N1	P8			t/s	BT10_3V	
182	L8	VSS		***VMI***			
183	P4	VP0		CAPD0	I/O	BDT6_5S	
184	P3	VP1		CAPD1	I/O	BDT6_5S	
185	P2	VP2		CAPD2	I/O	BDT6_5S	
186	P1	VP3		CAPD3	I/O	BDT6_5S	
187	R3	VP4		CAPD4	I/O	BDT6_5S	
188	R2	VP5		CAPD5	I/O	BDT6_5S	
189	R4	VDD					
190	R1	VP6		CAPD6	I/O	BDT6_5S	
191	T3	VP7		CAPD7	I/O	BDT6_5S	
192	N10	VSS	***ZV PORT***				
193	T2	PCLK	CAPCLK		I/O	BDT10_5S	
194	T1	EVIDEO#		VMIRDY#	IN	IBUFTU_5S	
195	U2	ESYNC#		VMICS#	I/O	BDT6U_5S	
196	U1	EDCLK#	CAPVS		I/O	BDT6U_5S	
197	U3	BLANK#	CAPHS		I/O	BDT6_5S	
198	V1	CHS			t/s	BT6_5S	
199	T4	CVS			t/s	BT6_5S	
200	Y1	XTLI (1)	MCLK			XOSC1	
201	Y2	XTLO (2)				XOSC2	
202	V3	AVDD1	(VDDC Level)				

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
203	V4	AVSS1					
204	U4	MLF			analog	NBUFT	
205	V5	AVSS2					
206	U5	VLF1			analog	NBUFT	
207	W3	AVDD2					
208	V2	AVSS3					
209	U6	VLF2			analog	NBUFT	
210	W2	AVDD3					
211	W4	VDD	(VDDC Level)				
212	N11	VSS					
213	Y4	P9			t/s	BT10_3V	
214	W5	P10			t/s	BT10_3V	
215	Y5	P11			t/s	BT10_3V	
216	V6	P12			t/s	BT10_3V	
217	U7	VDD					
218	W6	P13			t/s	BT10_3V	
219	K13	VSS					
220	Y6	P14			t/s	BT10_3V	
221	V7	P15			t/s	BT10_3V	
222	W7	P16			t/s	BT10_3V	
223	Y7	P17			t/s	BT10_3V	
224	U8	PCICLK	***PWR MGMT:***		IN	IBUFT_5S	
225	V8	INTR#	PSTATUS		t/s	BT8OD_5S	
226	W8	DEVSEL#			I/O	BDT10_5S	
227	Y8	IRDY#			I/O	BDT10_5S	
228	U9	TRDY#			I/O	BDT10_5S	
229	V9	STOP#			I/O	BDT10_5S	
230	W9	FRAME#			I/O	BDT10_5S	
231	Y9	PAR			I/O	BDT10_5S	
232	U10	C/BE3#			I/O	BDT10_5S	
233	M13	VSS					
234	V10	C/BE2#			I/O	BDT10_5S	
235	W10	RESET#			IN	IBUFTS_5S	
236	Y10	C/BE1#			I/O	BDT10_5S	
237	U11	C/BE0#			I/O	BDT10_5S	
238	V11	IDSEL			IN	IBUFT_5S	
239	W11	BREQ#		***PC_1***	t/s	BT8_5S	VDDH
240	Y11	BGNT#		***PC_2:***	IN	IBUFT_5S	VDDH
241	U12	GPIO6		VMIRD#	I/O	BDT6U_5S	VDDH
242	V18	GPIO3			I/O	BDT6_5S	VDDH
243	V12	GPIO2	PWM2	SDA	I/O	BDT6U_5S	VDDH
244	W12	GPIO1	PWM1	SCL	I/O	BDT6U_5S	VDDH

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
245	Y12	P24			t/s	BT10_3V	VDDH
246	V13	P25			t/s	BT10_3V	VDDH
247	M12	VSS					
248	W13	P26			t/s	BT10_3V	
249	Y13	P27			t/s	BT10_3V	
250	U13	P28			t/s	BT10_3V	
251	V14	P29			t/s	BT10_3V	
252	W14	P30			t/s	BT10_3V	
253	Y14	P31			t/s	BT10_3V	
254	U14	COMPSYNC			t/s	BT6_3V	
255	W15	SUBCCLK			t/s	BT10_3V	
256	Y15	STANDBY	VMID0	VP8	I/O	BDT6_5S	
257	V15	VDD					
258	U15	VDD					
259	V16	P32			t/s	BT10_5S	
260	W16	P33			t/s	BT10_5S	
261	Y16	P34			t/s	BT10_5S	
262	V17	P35			t/s	BT10_5S	
263	W17	GPIO4	VMIWR#		I/O	BDT10U_5S	
264*	W18	DACCOMP			analog		
265	U16	AVSS4					
266	Y17	R			analog	NBUFT	
267	Y18	G			analog	NBUFT	
268	Y19	B			analog	NBUFT	
269	K8	T/G(G2)					
270	K9	T/G(G2)					
271	K10	T/G(G2)					
272	K11	T/G(G2)					
273	K12	T/G(G2)					
274	J10	T/G(G2)					
275	J11	T/G(G2)					
276	J12	T/G(G2)					
277	J13	T/G(G2)					
278	H8	T/G(G2)					
279	H11	T/G(G2)					
280	Y3	T/G(G2)					
281	W1	T/G(G2)					
282	L12	T/G(G2)					
283	L13	T/G(G2)					
284	L17	T/G(G2)					
285	L18	T/G(G2)					
286	M8	T/G(G2)					

Table 6-10. Cyber9388 Pin Assignments (Cont'd)

Pin #	BGA NO.	Function 1	Function 2	Function 3	Pin Type	BUF	VDD
287	M9	T/G(G2)					
288	M10	T/G(G2)					
289	N12	T/G(G2)					
290	J2	T/G(G2)					
291	C10	T/G(G1)					
292	A14	T/G(G1)					

***Note:** DAC compensation capacitor pin.

6.3 Panel Signal Mapping

Table 6-11. DSTN Pins P[0:15]

Type	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15
DSTN16	LD0	LD1	LD2	LD3	LD4	LD5	LD6	LD7	UD0	UD1	UD2	UD3	UD4	UD5	UD6	UD7
DSTN24	LD0	LD1	LD2	LD3	LD4	LD5	LD6	LD7	LD8	LD9	LD10	LD11	UD0	UD1	UD2	UD3
	P16	P17	P18	P19	P20	P21	P22	P23								
DSTN24	UD4	UD5	UD6	UD7	UD8	UD9	UD10	UD11								

Notes: 1 For 16 bit color dual scan STNs, LD7 or UD7 above corresponds to red column 0 for the first data of a line.

2. For 24 bit color dual scan STNs, LD11 or UD11 above corresponds to red column 0 for the first data of a line. UD5-UD11 are on P16-P23.

Table 6-12. TFT Pins P[0:23]

Data	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
TFT	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23
3	R0				G0				B0															
9	R2	R1	R0		G2	G1	G0		B2	B1	B0													
9+9	Ro2	Ro1	Ro0		Go2	Go1	Go0		Bo2	Bo1	Bo0		Re2	Re1	Re0		Ge2	Ge1	Ge0		Be2	Be1	Be0	
12	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0												
12+12	Ro3	Ro2	Ro1	Ro0	Go3	Go2	Go1	Go0	Bo3	Bo2	Bo1	Bo0	Re3	Re2	Re1	Re0	Ge3	Ge2	Ge1	Ge0	Be3	Be2	Be1	Be0
18	R5	R4	R3	R2	G5	G4	G3	G2	B5	B4	B3	B2	R1	R0	G1	G0	B1	B0						
18+18[1]	R5	R4	R3	R2	G5	G4	G3	G2	B5	B4	B3	B2	R1	R0	G1	G0	B1	B0	S1	S2				
24	R7	R6	R5	R4	G7	G6	G5	G4	B7	B6	B5	B4	R3	R2	G3	G2	B3	B2	R1	R0	G1	G0	B1	B0

Table 6-13. TFT 18+18[2] Pins P[0:35]

TFT	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23
18+18	Ro5	Ro4	Ro3	Ro2	Go5	Go4	Go3	Go2	Bo5	Bo4	Bo3	Bo2	Re5	Re4	Re3	Re2	Ge5	Ge4	Ge3	Ge2	Be5	Be4	Be3	Be2
TFT	P24	P25	P26	P27	P28	P29	P30	P31	P32	P33	P34	P35												
18+18	Ro1	Ro0	Go1	Go0	Bo1	Bo0	Re1	Re0	Ge1	Ge0	Be1	Be0												

Notes: 1. Type 1 Of 18+18 uses external latches to capture odd and even data.

2. Type 2 of 18+18 is direct 36-bit output.

3. The most significant bits of color data are always on pins P0, P4, and P8.

Table 6-14. Panel Type Abbreviation Key

Abbreviation	Description
DSTN16	Color STN dual scan panel, 16 bit data interface
DSTN24	Color STN dual scan panel, 24 bit data interface
TFTxx	TFT panel, xx bit color data or xx/3 bit mono data interface

6.4 Cyber9388 BGA Pin (Grid) Assignments

(Top view, looking from the cap side)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
Y	5 P23	*268* *B*	*267* *G*	*266* *R*	261 P34	256 STNDBY	253 P31	249 P27	245 P24	240 BGNT#	236 C/BE1#	231 PAR	227 IRDY#	223 P17	220 P14	215 P11	213 P9	***G2*** ***VSS***	201 XTLO	200 XTLI	Y
W	6 P22	7 LP	*264* *COMP*	263 GPIO4	260 P33	255 SUBCLK	252 P30	248 P26	244 GPIO1	239 BREQ#	235 RESET#	230 FRAME#	226 DEVSEL#	222 P16	218 P13	214 P10	211 VDD	**207** **AVDD2**	**210** **AVDD3**	***G2*** ***VSS***	W
V	10 P18	8 SHIFT	242 GPIO3	262 P35	259 P32	**P2** **VDD**	251 P29	246 P25	243 GPIO2	238 IDSEL	234 C/BE2#	229 STOP#	225 INTR#	221 P15	216 P12	***205*** ***AVSS2***	***203*** ***AVSS1***	**202** **AVDD1**	***208*** ***AVSS3***	198 CHS	V
U	12 P20	11 P19	1 **AVDD5**	*2* *IRSET*	***265*** ***AVSS4***	**P2** **VDD**	254 COMPS	250 P28	241 GPIO6	237 C/BE0#	232 C/BE3#	228 TRDY#	224 PCICLK	**P2** **VDD**	*209* *VLF2*	*206* *VLF1*	*204* *MLF*	197 BLANK#	195 ESYNC#	196 EDCLK#	U
T	15 FLM	14 MOD	13 P21	*3* ***AVSS5***													199 CVS	191 VP7	193 PCLK	194 EVIDEO#	T
R	18 AD29	17 AD30	16 AD31	**P2** **VDD**													**P2** **VDD**	187 VP4	188 VP5	190 VP6	R
P	23 AD25	20 AD27	19 AD28	**P2** **VDD**													183 VP0	184 VP1	185 VP2	186 VP3	P
N	26 AD22	25 AD23	24 AD24	22 AD26													178 P5	179 P6	180 P7	181 P8	N
M	30 AD18	29 AD19	28 AD20	27 AD21													**P2** **VDD**	174 P2	175 P3	177 P4	M
L	34 AD16	33 AD17	***G2*** ***VSS***	***G2*** ***VSS***													170 MD62	171 MD63	172 P0	173 P1	L
K	38 AD12	37 AD13	36 AD14	35 AD15													166 MD58	167 MD59	168 MD60	169 MD61	K
J	43 AD9	40 AD10	39 AD11	**P2** **VDD**													162 MD55	163 MD56	***G2*** ***VSS***	165 MD57	J
H	46 AD6	45 AD7	44 AD8	**P2** **VDD**													158 MD51	159 MD52	160 MD53	161 MD54	H
G	49 AD3	48 AD4	47 AD5	50 AD2													**P2** **VDD**	154 MD48	156 MD49	157 MD50	G
F	53 AD0	52 AD1	54 ROMCS#	55 MD31													150 MD44	151 MD45	152 MD46	153 MD47	F
E	57 MD29	56 MD30	58 MD28	**P1** **VCCA2**													146 MD40	147 MD41	148 MD42	149 MD43	E
D	59 MD27	61 MD26	62 MD25	68 MD22	77 MD15	82 MD11	86 MD7	90 MD4	**P1** **VCCPW2**	98 DQM1	102 MA2	107 MA4	**P1** **VCCP2**	**P1** **VCCP1**	112 BA	**P1** **VCCPW1**	**P1** **VCCA1**	135 VP15	142 MD38	144 MD39	D
C	63 MD24	64 MD23	69 MD21	74 MD18	78 MD14	83 MD10	87 MD6	91 MD3	94 MD0	99 DQM0	G1 VSSM	108 MA5	111 MA8	120 MTEST	124 DQM6	127 GPIO7	134 VP14	139 MD35	140 MD36	141 MD37	C
B	65 VP10	66 VP11	70 MD20	75 MD17	79 MD13	84 MD9	88 MD5	92 MD2	96 DQM3	100 MA0	104 SDMCLK	109 MA6	115 WE#	119 CAS#	122 DQM4	125 DQM7	128 SUSPND	131 ENPBLK	137 MD33	138 MD34	B
A	73 VSSF	67 VP12	71 MD19	76 MD16	80 MD12	85 MD8	G1 VSSM	93 MD1	97 DQM2	101 MA1	106 MA3	110 MA7	116 RAS#	118 CKE	123 DQM5	126 REFCLK	129 VP13	132 ENPVEE	133 ENPVDD	136 MD32	A
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Note:
Die is rotated 180 degrees.

TRIDENT MICROSYSTEMS
Cyber9388 BGA

T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	
T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	
T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	
T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	T/G G2	
T/G G1	T/G G1	T/G G1	T/G G1	T/G G1	T/G G1	
T/G G1	T/G G1	T/G G1	T/G G1	T/G G1	T/G G1	

A14 & C10 go to Ground Ring #1 (G1)

L17, L18, J2, W1 & Y3 go to ground Ring #2 (G2)

Pin#
Pin Name

MOLDGATE

Revision History

1: 1.00 First BGA pinout for 9388, 2/4/97

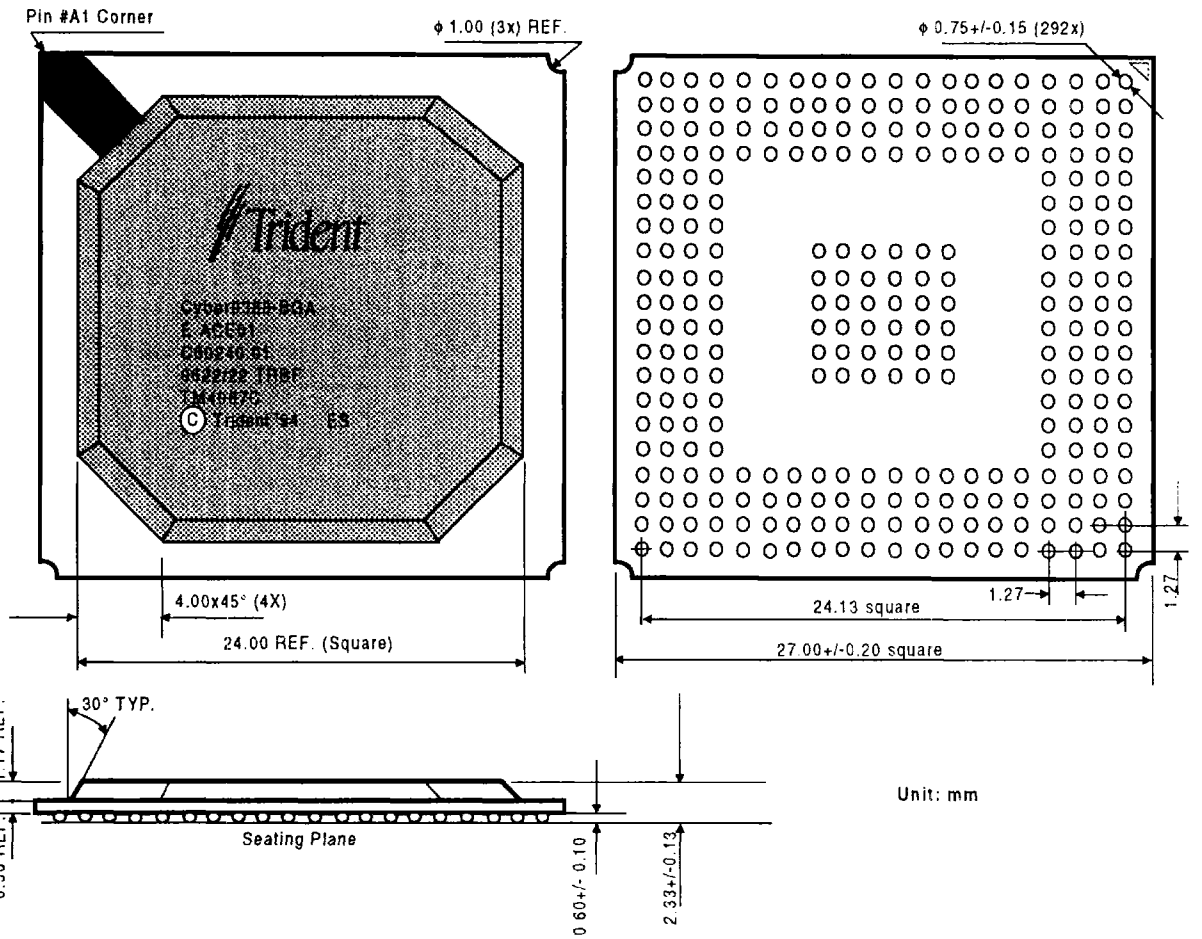
Note: Changes since last BGA layout:

1: Pad #73, VSSF, will not be bound out.

2: BGA balls A14 & C10 need to be connected to Ground Ring #1 (G1)

3: BGA balls L17, L18, J2, W1 & Y3 need to be connected to Ground Ring #2 (G2).

6.5 Cyber9388 BGA Package Physical Dimensions



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7. System Design

7.1 Power Up Configuration

During system reset and power up, the configuration information of the video subsystem is latched into the Cyber9388's internal configuration registers based on the status of the memory data lines MD [63:0] (In the sample schematic, only MD[39:0] are used for this purpose). No external pull-up resistors are necessary for the setup of the configuration since all MD pins of the Cyber9388 have been internally pulled up on their I/O buffers.

Refer to Table 7-1 for the power up configuration of MD lines.

The state of the MD bus is determined as follows: each of MD[63:0] bus has an internal pull-up. It can be set to logical 0 value by pulling-down to GND through a 4.7K - 10K resistor. These pull-up and pull-down resistors are weak so that they will not affect the normal operation.

Table 7-1. Power Up Configuration

MD	Description	I/O Port	HD/SF
MD[7:0]	General Purpose MD Configuration	3C5.28.7:0	Soft
MD8	BIOS control: 1 = Enable, 0 = Disable	3C5.0F.6	Soft
MD9	Linear/Bank Addressing Control: 0 = Linear Only, 1 = Linear/Bank	3C5.0F.4	Hard
MD[11:10]	Memory interface control: 11 = Internal memory only, 10 = External memory only 01 = Internal/External memory, 00 = Reserved	3C5.0C.3:2	Hard
MD12	BIOS Size: 0: 64K, 1: 32K	3C5.0C0.3 (old mode)	Hard
MD13	Video Subsystem enable: 0 = 46E8, 1 = 3C3	3C5.0C0.4 (old mode)	Hard
MD14	Clock Source Select: 0 = External, 1 = Internal	~3X5.3B.6	Hard
MD15	Memory I/F Control: 0 = Tri-stated, 1 = Normal	~3X5.23.0	Hard
MD16	Memory Mapped I/O Control: 0 = Enable, 1 = Disable	~3X5.39.0	Hard
MD17	PCI target fast back-to-back transaction: 0 = Enable, 1 = Disable	~pci.06.7	Hard
MD18	PCI master fast back-to-back transaction: 0 = Enable, 1 = Disable	~pci.04.9	Hard
MD19	TV Control: 1 = PAL, 0 = NTSC	3X5.C0.7	Hard
MD20	Display Type: 0 = TV enable, 1 = CRT only	~3X5.C0.1	Hard
MD21	FSC select: 1 = FSC X1, 0 = FSC X4	3X5.C0.0	Hard
MD22	TV Control: 0 = Simultaneous display, 1 = Exclusive TV	3X5.C0.3	Hard
MD23	Reserved		
MD[31:24]	Flat Panel Type Select: TFT: 0000=6x4-18, 0001=8x6-18, 0010=10x7-18, 0011=10x7-18+18, 0100=12x10-18+18 DSTN: 0101=6x4-16, 0110=8x6-16, 0111=10x7-16, 1000=10x7-24, 1001=12x10-24	3CF.41.7:0	Soft
MD[39:32]	DRAM clock select	3X5.2C.7:0	Soft

Notes: 1. The symbol "~" represents bit inversion.
2. MD setting: 1: OPEN or PULL HIGH; 0: PULL DOWN
3. Switches and jumpers that are ON or closed are 0; switches and jumpers that are OFF are 1.
4. Hard means MD directly controls the function defined by the bit.
5. Soft means MD configuration only sets the I/O register and the output of the register does not control any internal H/W function. BIOS will read the soft MD and configure the H/W function according to the soft bit.

7.1.1 PCI Bus Interface

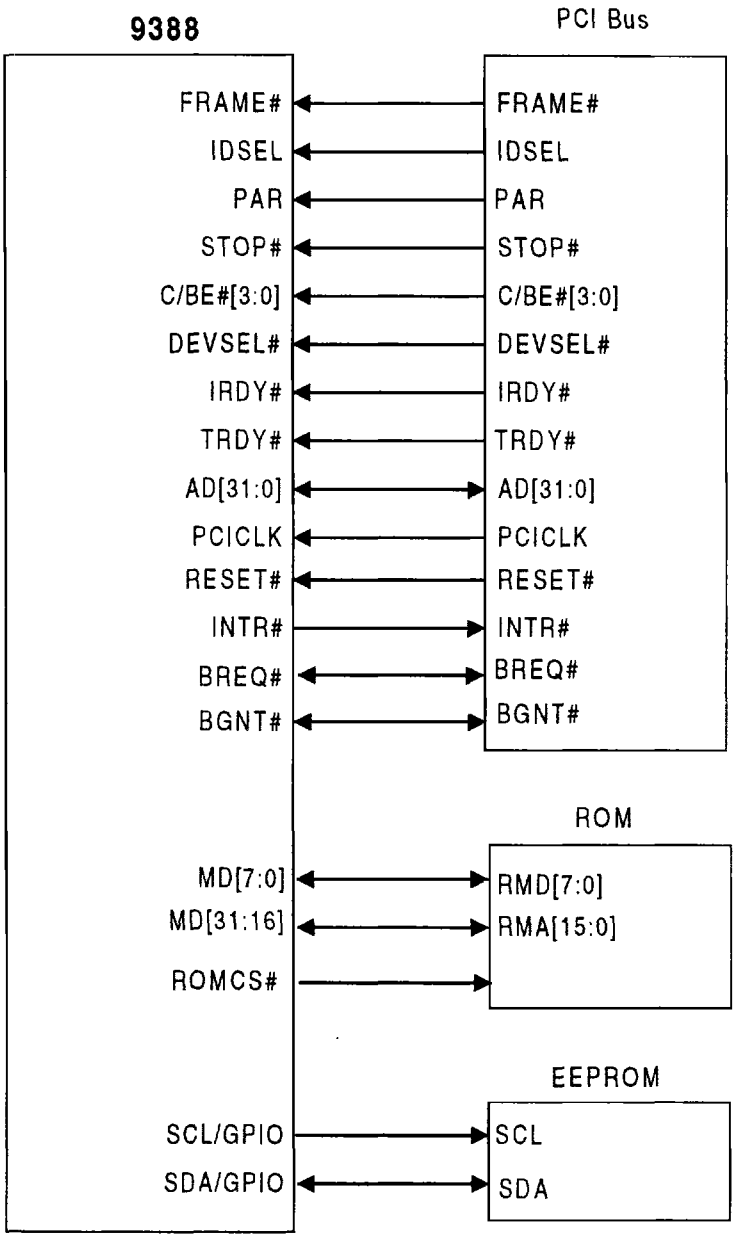


Figure 7-1. PCI Bus Interface

7.1.2 TFT Panel (Single Pixel/Clk) Interface (Direct Drive)

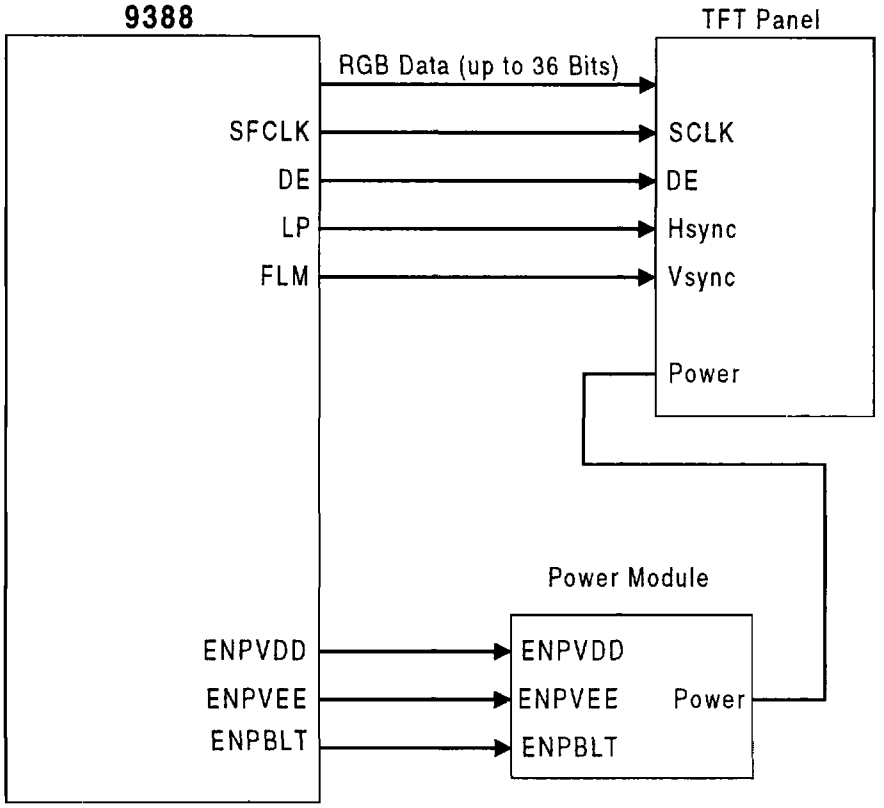


Figure 7-2. TFT Panel (Single Pixel/Clk) Interface

7.1.3 TFT Panel (Double Pixel/Clk) Interface

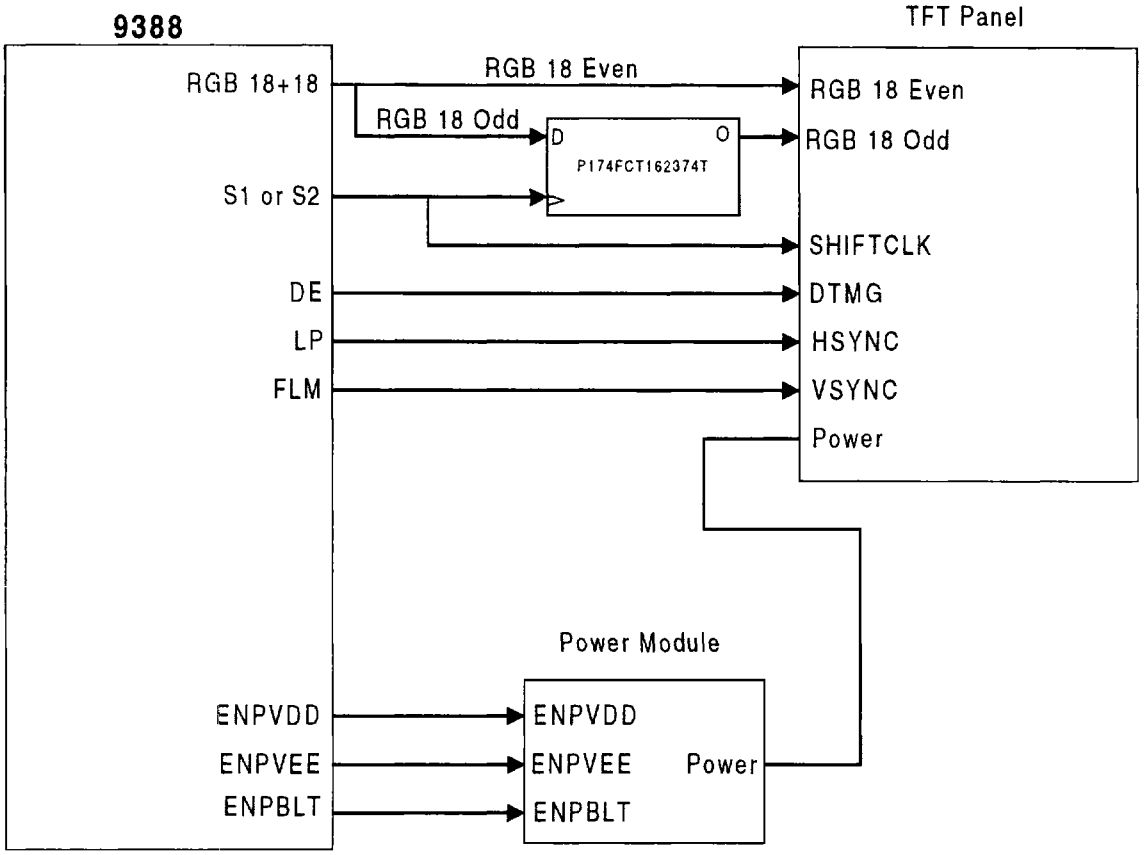


Figure 7-3. TFT Panel (Double Pixel/Clk) Interface

7.1.4 STN Panel Interface - 16 Bit Color Data

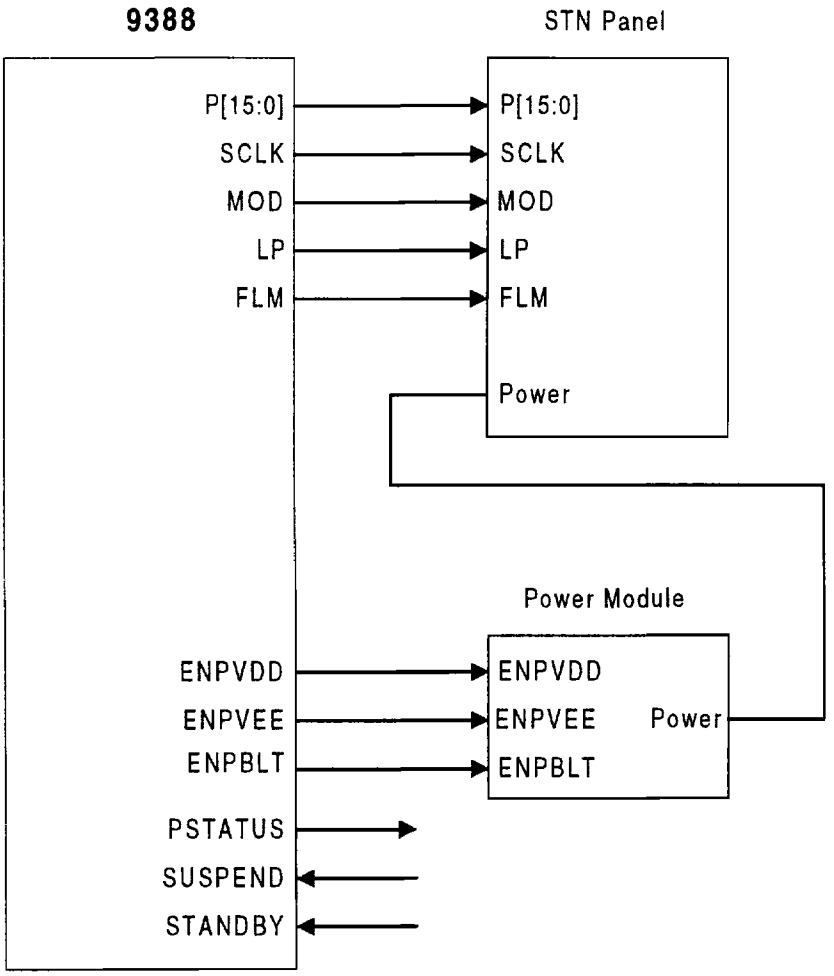


Figure 7-4. STN Panel Interface - 16 Bit Color Data

7.1.5 CRT/TV Interface

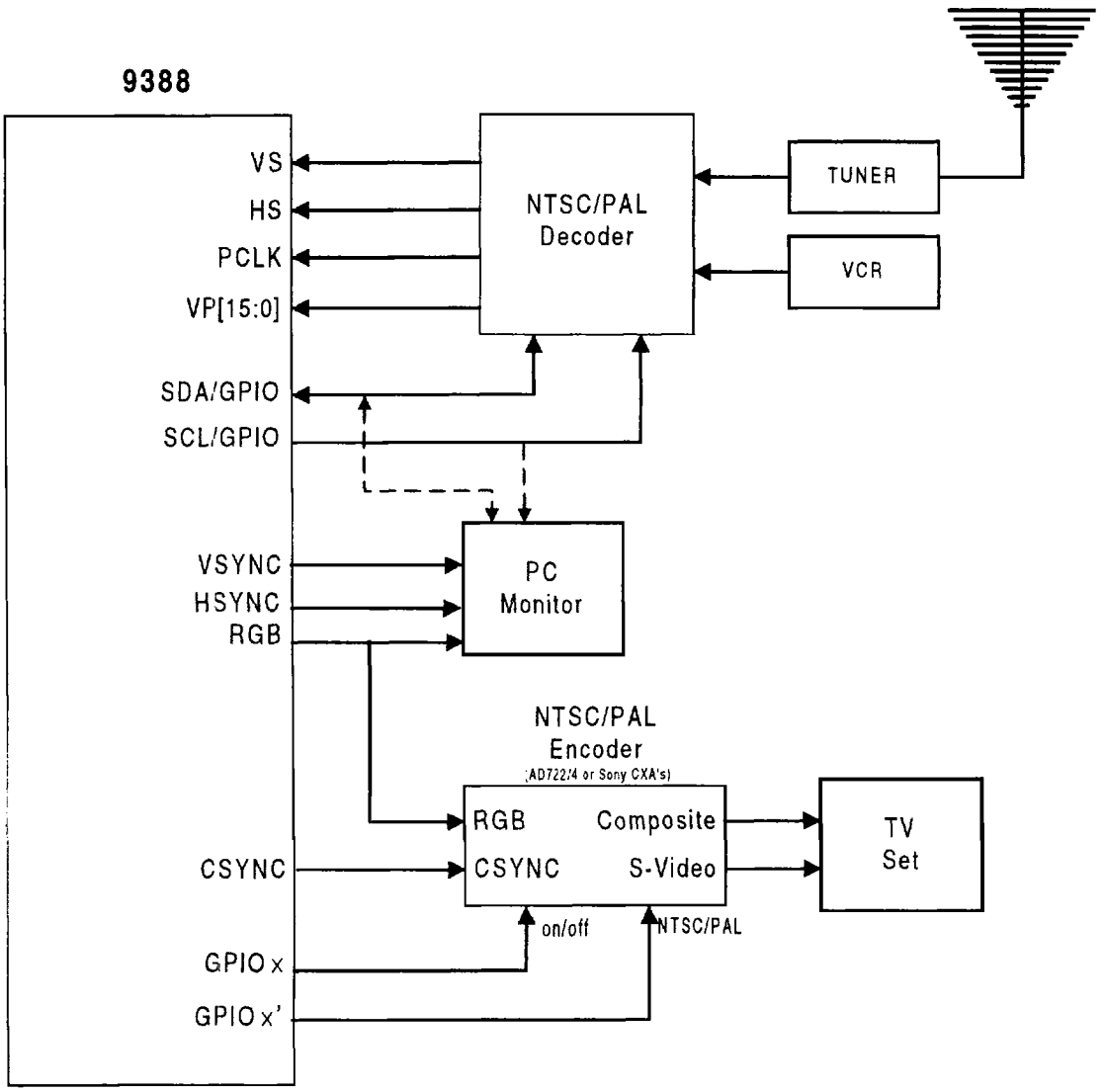


Figure 7-5. CRT/TV Interface

7.2 Layout Considerations

7.2.1 Clock Synthesizer

The on-chip clock synthesizer requires a quartz crystal of the following characteristics:

Table 7-2. Clock Synthesizer Characteristics

Frequency	14.318 MHz +0.5% and/or 17.734 MHz +0.5% fundamental resonance.
Load Capacitance	15 pF to 40 pF in parallel resonance mode.
ESR	25 to 45 ohms.
Shunt Capacitance	Approximately 5 pF.

The crystal should be connected across XTLI (A16) and XTLO (B16). If a 14.318 MHz or a 17.634 MHz oscillator is used instead of a crystal, then the clock output of the oscillator should be connected to XTLI only, and XTLO should be left open. If the clock signal is tapped off the AT Bus, the same connection applies. If a crystal is used, both sides of the crystal should have soldering pads to allow grounding of the case and attaching of the crystal to PCB in a secure manner. A ground area should be present under the crystal for multi-layer board designs. To prevent shorts between the case and other signal traces or VCC there should not be any vias close to or underneath the crystal case.

7.2.2 Analog and Digital GND Separation

Analog and digital GND separation is very important for mixed signal devices. For the design presented, not only is the analog ground separated from the digital ground, but the analog ground for the DAC side is separated from the analog ground for the clock side of the chip. Traces for the analog ground should not have any digital connections.

For the example in Figure 8-8:

- FBs are used to isolate analog voltages from digital voltages (choke).
- C_{D1} and C_{D2} act as local noise filters. C_{D1} and C_{D2} are actually pre-filters for FB; thus, they should be located as close to the inductors as possible.
- C_{S1} an C_{S2} are bulk capacitors, used as a supply of local charge, smoothing power flow from the supply to the local circuit. The FB is used to isolate digital ground noise from analog ground.

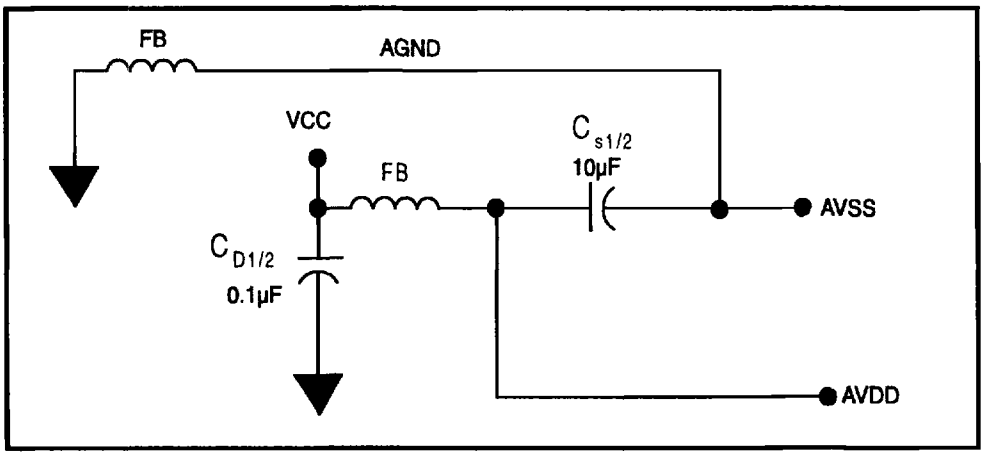


Figure 7-6. Analog and Digital GND Separation

Analog R, G, and B (red, green, and blue) traces should be designed to be as short as possible; however, careful design will allow considerable trace lengths with no visible artifacts. V.GND is an "analog current balance path" for the RGB lines:

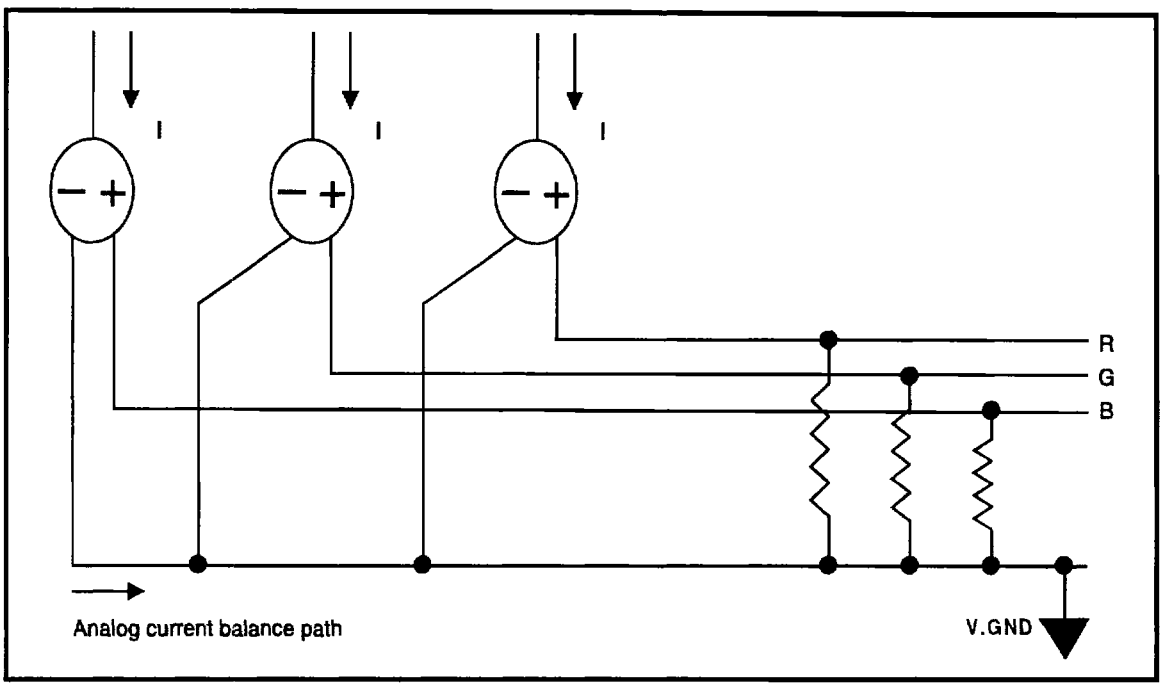


Figure 7-7. Analog Current Balance Path for RGB Lines

In terms of layout, V.GND should follow 2 traces that encapsulate the RGB traces all the way to the D-shell connector, and should not be tied to ground until connected to the Right Angle D-type connector. V.GND should also be tied to pins 6, 7, and 8 of the connector.

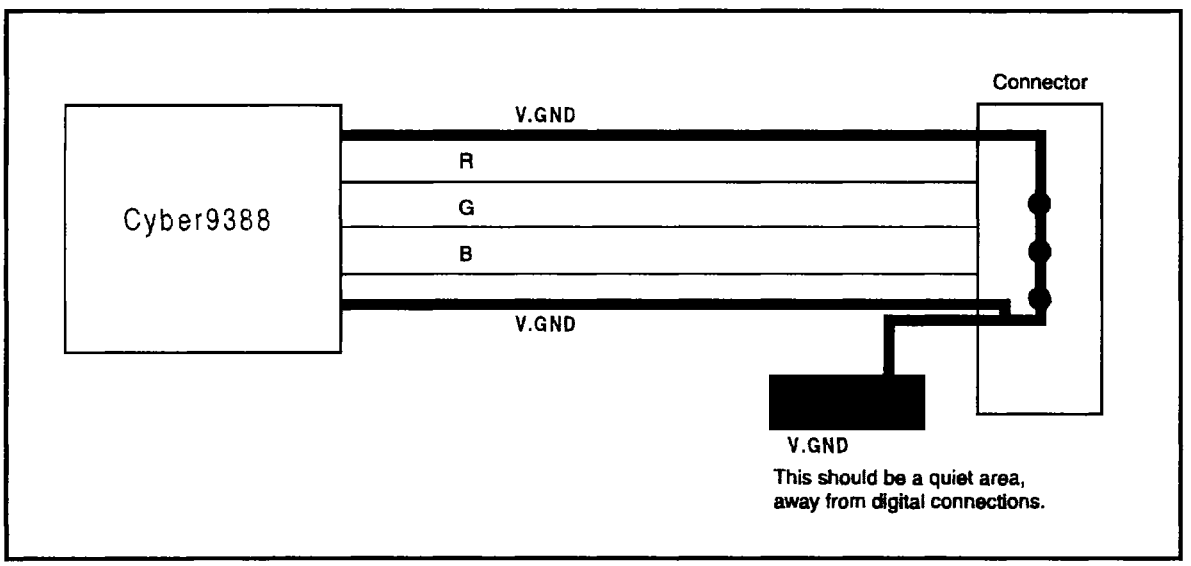


Figure 7-8. V.GND Placement Diagram

7.2.3 Trace Size and Restrictions

The recommended trace sizes and restrictions presented in this section are based on conservative "worst case" design conditions for two large add-on cards. There is a degree of flexibility in the trace widths, but the values presented in this section are strongly recommended if the real estate and budget permit so.

7.2.3.1 Power and GND Routing

All analog and digital power / ground traces should be minimum of 50 mil in routed width. The traces should be as short as possible coming from the defining point (or PCB card edge in the case of add-on card designs) and should terminate at the IC.

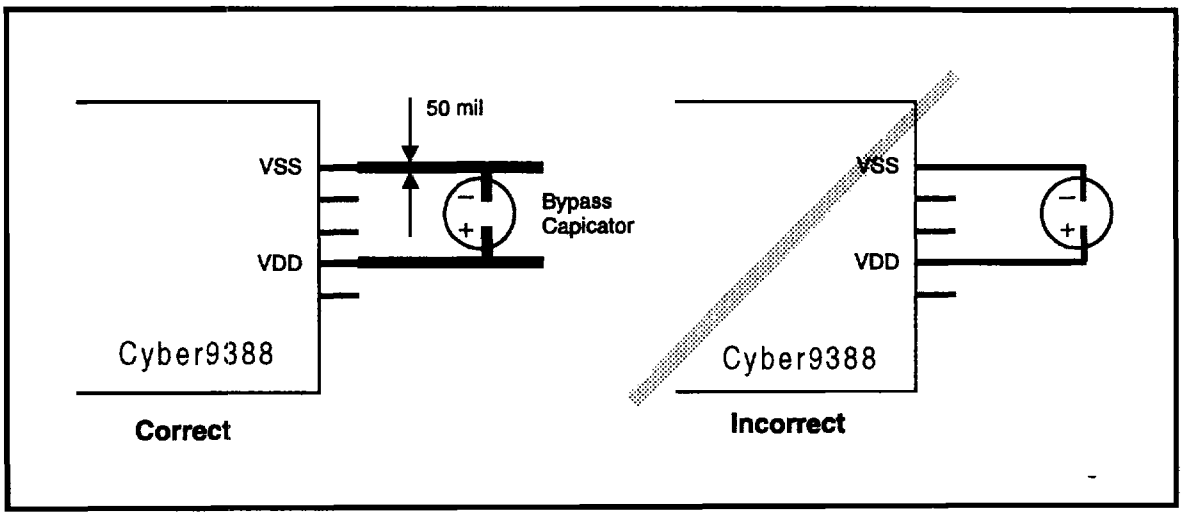


Figure 7-9. Trace Size Diagram

For two-layer add-on card designs two dimensional gridding of VCC and GND should be implemented, with the loop sizes minimized as much as possible. (It is not recommended to use a 2-layer board for 64 bit memory data bus configuration.)

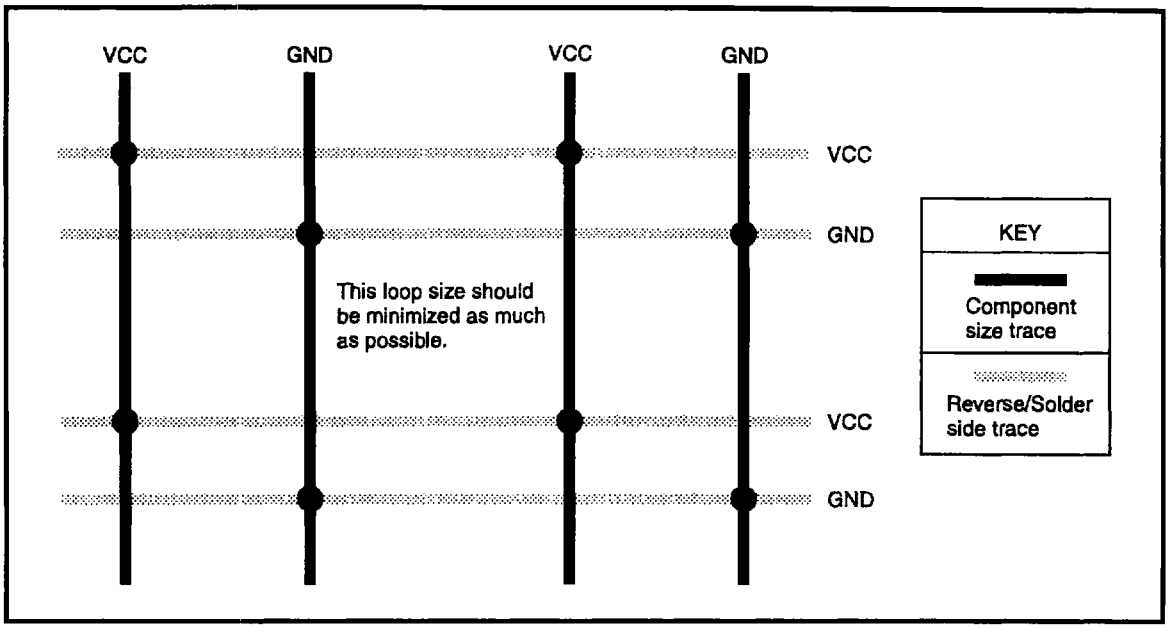


Figure 7-10. Two Dimensional VCC and GND Grid Diagram

In addition to minimizing the loop size of VCC and GND grids for two-layer boards, VCC and GND should be routed across the bottom of the board to allow short access to the edge connector. Two vias are recommended for every tie point (VCC / GND) between layers to minimize AC connection resistance. Bypass capacitors are recommended for every VCC entry point on the edge connector.

7.2.4 Signal Routing

In terms of routing, signal traces are classified as critical high-speed, relatively slow, and static. The table below shows the details of the signal classifications for the Cyber9388.

Table 7-3. Signal Classification

Signal	Critical Hi-Speed	Relatively Slow	Static
C/BE[3:0]#	●		
AD[31:0]	●		
ROMCS#		●	
PAR	●		
STOP#		●	
IRDY#	●		
DEVSEL#	●		
TRDY#	●		
INT#	●		
CLK	●		
RST#			●
RMD[7:0]		●	
IDSEL	●		

7.2.4.1 Clock Signals

The recommended clock signal trace width for clock signals is 15 to 20 mil. Clock signals should be routed first with minimum bending to ensure signal integrity and minimize EMI. 90° bends should be strictly avoided.

7.2.4.2 Critical High-Speed Signals

Traces for the critical high-speed signals should be routed after the clock signals. Trace bending should be kept at a minimum to ensure signal integrity and minimize EMI. The trace width should be at least 12 to 15 mil. Signal spacing from other traces should be at least 12 to 15 mil to avoid cross-talk. There should not be any traces "lined up" with the clock signal on the other side of the board so that capacitive coupling is kept to a minimum.

7.2.4.3 Relatively Slow Signals

These traces should be routed after the critical high-speed signals. Minimum trace width recommended is 10 mil. If the function of the signal is critical, it should be routed two trace widths away from high speed signals to prevent cross-talk induced activation.

7.2.4.4 Static Signals

Static signal traces should be routed after the relatively slow signal traces. The recommended minimum trace width is 8 mil. Static signal traces should be routed two trace widths away from high speed signal traces to prevent cross talk induced activation.

7.3 FCC Compliance Guide

7.3.1 Layout Issues/Component Placement

1. For two-layer add-on card designs, power and ground should be routed from one end of the board to the other, near the connectors, connecting to all power and ground pins on each connector. Bypass capacitors should be placed for each entry point for power. (See Figure 9-14.)
2. Separation of analog power and ground traces from digital power and ground traces should be implemented as recommended in section 8.4.2, with special attention to VGA analog ground return trace (VGA connector pins 6, 7 and 8).
3. Clock chips, oscillators and crystals should be positioned as far away from the feature connectors and VGA connector as possible.
4. All non analog signal traces should be kept out of the sensitive areas where analog components are located (e.g., the capacitors for the MLF and VLF).
5. For all RC filters, the capacitor should be positioned at the receiving end of the trace.
6. Bypass capacitors for the power supply must be present on the board. Tantalum or electrolytic capacitors must be present at every point where power comes into the board. This stabilizes power flow at the board interface. Tantalum capacitors are recommended because they provide a lower ESR and better bypassing capability than electrolytic capacitors. If electrolytic capacitors are to be used, then a 10-20% larger capacitance value should be selected.
7. Bypass capacitors should be placed for each power-ground pairs on the chip to provide the transient current required by the chip when signal levels are switched. Bypass capacitors for the power-ground pairs should be placed as close to the chip as possible, and the recommended trace width is 50 mil.

7.4 Schematics Examples (PCI Bus)

7.4.1 Special Layout Considerations

The following table summarizes special layout considerations for the components shown in the reference schematic.

Table 7-4. Layout Considerations

Component	Purpose	Location
CY1	14.318 MHz Quartz crystal for on-chip clock synthesizer.	As close to the Cyber9388 as possible. The frequency range of the crystal is better to be able to go 0.5% higher than the specified 14.318 MHz.
CY2	17.734 MHz Quartz crystal for on-chip clock synthesizer.	As close to the Cyber9388 as possible. The frequency range of the crystal is better to be able to go 0.5% higher than the specified 17.734 MHz.
VC1	Variable capacitor for adjusting the frequency.	Close to the Crystal.
C7	Capacitor used to adjust the frequency.	Close to the crystal.
C19, C20, C21	Used for Phased Locked Loop filter for the Video Clock (VLF) and the Memory Clock (MLF).	These components need to be as close to the chip as possible. There should not be any signal traces under or close to these components.
R1	Used to set zero reference voltage for internal DAC.	Should be isolated from noisy signal traces.
C10,C14, FB3, FB4, C15	Used for digital-analog GND separation, and to filter out noise to analog section of Clock Synthesizer.	C10, C14, C15, FB3 and FB4 should be as close to each other and close to the pins on the chip as possible.
C12, C23, C24, FB5, FB6	Used for digital-analog GND separation, and to filter out noise to analog section of Clock Synthesizer.	C12, C23, C24, FB5 and FB6 should be as close to each other and close to the pins on the chip as possible.
C16, C17, C22, FB1, FB2	Used for digital-analog GND separation, and to filter out noise to analog section of Clock Synthesizer.	C16, C17, C22, FB1 and FB2 should be as close to each other and close to the pins on the chip as possible.
C8, C9, C11, C13, C18, FB7, FB8	Used for digital-analog GND separation, and to filter out noise to analog section of RAMDAC.	C8, C9, C11, C13, C18, FB7 and FB8 should be as close to each other and close to the pins on the chip as possible.
R134, R5	Pull-ups used to hold signal level after being tri-stated from a logic high.	These resistors should on the chip side.
C170	High pass filter.	These capacitors should on the chip side.
R10-R13	Termination resistors for LCD control signals.	
C26, C27, L11	Used for digital-analog GND separation, and to filter out noise to analog section of switch.	C26, C27, and FB11 should be as close to each other and close to the pins on the chip as possible.
C173	Used to adjust frequency.	Close to the oscillator.
R2, R3, R6-R9	Load resistors used to match standard load requirements.	
R14, C31	Low pass filter for RESET# signal.	C31 should be placed as close to pin RST# as possible.
R18, C41	Termination resistor and filter capacitor for the PCI clock.	R18 should be as close to the defining point as possible. C41 should be as close to the PCICLK pin on the chip as possible.
R16, R17	Termination resistors for TRDY# and DSEL#.	Should be as close to the chip as possible.
R19, R20	Pull-up resistors	

Table 7-4. Layout Considerations (Cont'd)

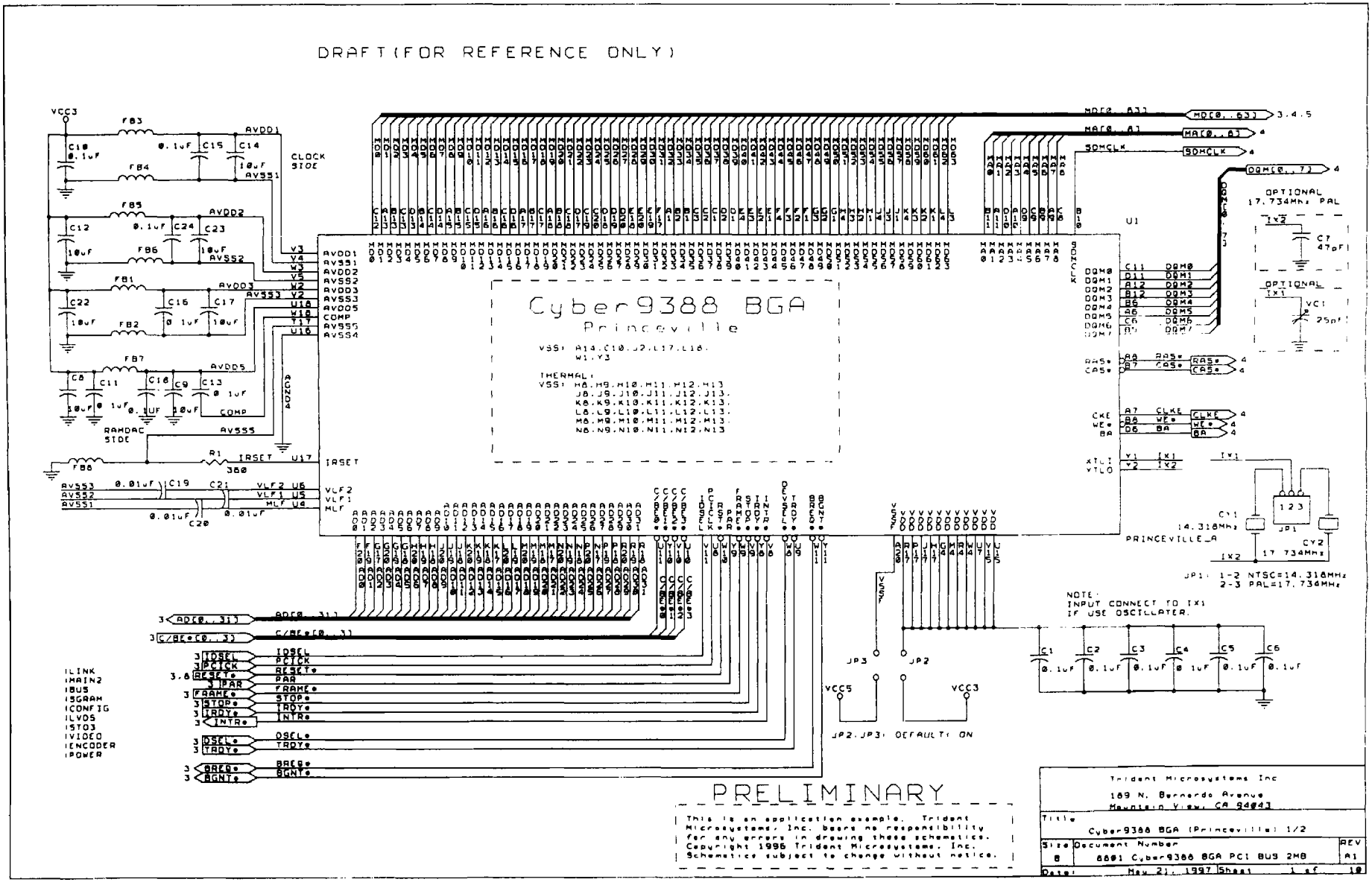
Component	Purpose	Location
R21, C174	Filter	
R15	Pull-up resistor for EEPROM.	Close to the pin.
R128,R129,R130, R131,C181,C182, C183, C184	Low pass filters for C/BE[3:0]# signal lines.	These filters should be close to the C/BE[3:0]# pins on the chip.
R30-R34	Serial termination resistors for SGRAM control signal lines.	These should be as close to the pins as possible, on the chip side.
C55, C56	Used as a delay / filter for the R/CAS# line.	If used as a delay, C55 and C56 should be placed close to the R/CAS on the chip. If used for filtering, it should be placed close to SGRAM.
R22-R29	Termination resistors for DQM signal lines.	These should be as close to the DQM pins as possible, on the chip side.
C47-C54	Delay of DQM signal lines and noise reduction.	For noise reduction purposes, the capacitors should be as close to the DRAMs as possible. When used as delays, they should be closer to the chip. The noise reduction application is recommended.
C90-C93	Decoupling capacitors for SGRAM.	Close to SGRAM pins.
RP1-RP5	4.7K resistors pack used to configure the chip on system reset.	
L1	Inductor for power switch regulator SI9145BQ	The connection of the inductor to the switching FET SI9433DY and gate control pin 15 of SI9245BQ are high dv/dt points. They must be kept away from high impedance pins 9 and 10 as well as the feedback path.
C129	Bypass capacitor.	If a ground plane is not used in the PCB layout, the ground connection of the capacitor should be as close to pin 8 (GND) as possible.
C128,R61,C127,R60, C125,C124,C123, R59,R57,C122,R56, C120, R58,C121	Resistors and capacitors for power supply module.	Refer to technical notes from TEMIC, Siliconix
C179, C180, L7	LC filter	
C131-C136, FB18-FB20	These form PI Filters for the RGB signal lines.	The capacitors should be closest to the connector, followed by the ferrite beads.
R74,R75,C137,C138	Low pass filters for H/V sync signal lines.	Should be placed as close to the connector as possible.
C150-C152	AC coupling capacitors for RGB	
R78-R80,C141,C145, C147	Driving out loads and capacitors.	Resistors shall be as close to the drive-out pins and to the capacitors as possible.
C1-C6,C28,C127, C32-C36,C42-C46, C37,C69-C79, C80-C83	De-coupling capacitors for power supplies.	Capacitors should be close to pins on the chip and "power-ground" paired.

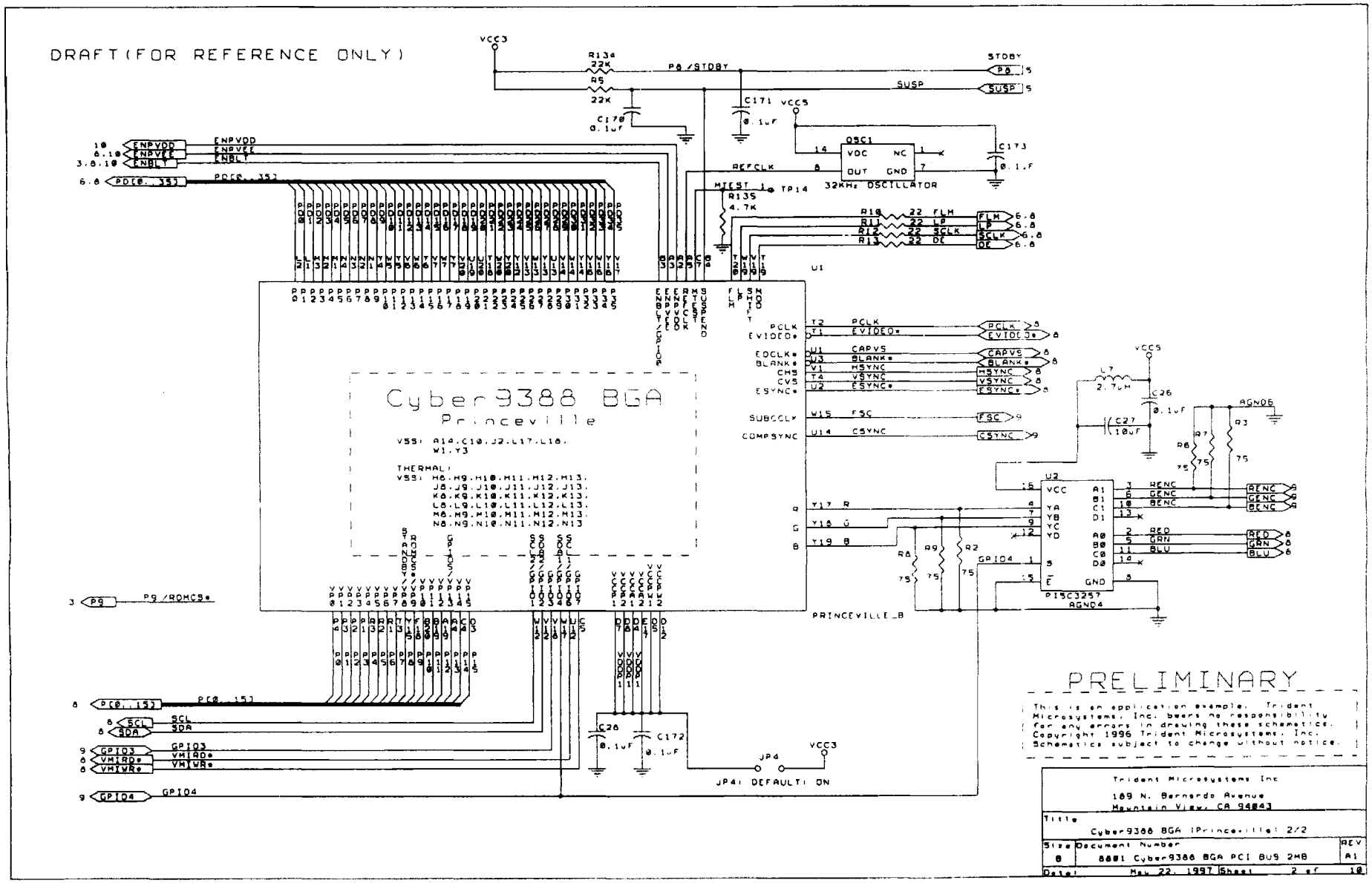
Note: For information about TUNER, DECODER, and ENCODER layout considerations, please contact your local Trident Microsystems, Inc. Sales Representative

7.4.2 PCI Bus Schematic Example

The following schematics represent sample designs and are for reference only. Working schematics, BOM, and Gerber files for various board designs may be obtained from the local Trident Microsystems, Inc. Sales Representative.

Set 1: 9801 Cyber9388 BGA PCI Bus




DRAFT (FOR REFERENCE ONLY)
VCC3
R134 22K
R5 22K
P8 /STDBY
STDBY
SUSP
C170 0.1uF
C171 0.1uF
VCC5
OSC1
VDC
NC
OUT
GND
32MHz OSCILLATOR
C173 0.1uF
REFCLK
TP14
R135 4.7K
ENPVDD
ENPVEE
ENBLT
PD[0..35]
R10 22 FLM
R11 22 LP
R12 22 SCLK
R13 22 OE
FLM
LP
SCLK
OE
U1
Cyber9388 BGA
Princeville
VSS: A14,C10,J2,L17,L18, W1,Y3
THERMAL: VSS: H6,H9,H10,H11,H12,H13, J6,J9,J10,J11,J12,J13, K6,K9,K10,K11,K12,K13, L6,L9,L10,L11,L12,L13, M6,M9,M10,M11,M12,M13, N6,N9,N10,N11,N12,N13
PCLK
EVIDEO
EDCLK
BLANK
CHS
CVS
ESYNC
CAPVS
HSYNC
VSYNC
SUBCLK
COMPSYNC
FSC
CSYNC
PRINCEVILLE_B
VCC5
L7 2.7uH
C26 0.1uF
C27 10uF
AGND6
R6 75
R7 75
R3 75
U2
PI5C3257
AGND4
RENC
GENC
BENC
RED
GRN
BLU
Y17 R
Y18 G
Y19 B
R8 75
R9 75
R2 75
GPIO4
P9
P9 /ROMCS#
P8[0..15]
SCL
SDA
GPIO3
VMIRD#
VMIWR#
C26 0.1uF
C172 0.1uF
JP4
JP4: DEFAULT: ON
PRELIMINARY
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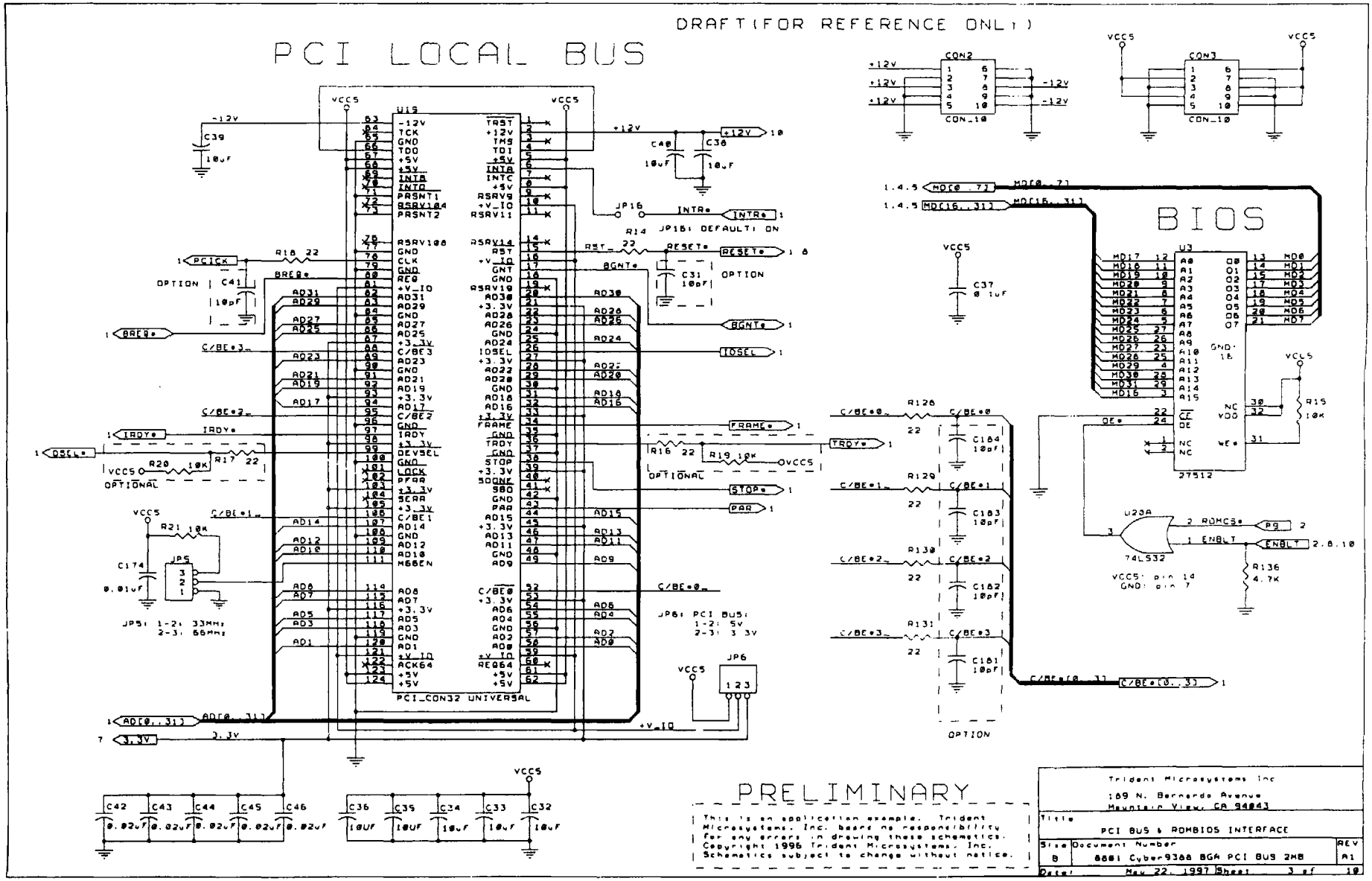
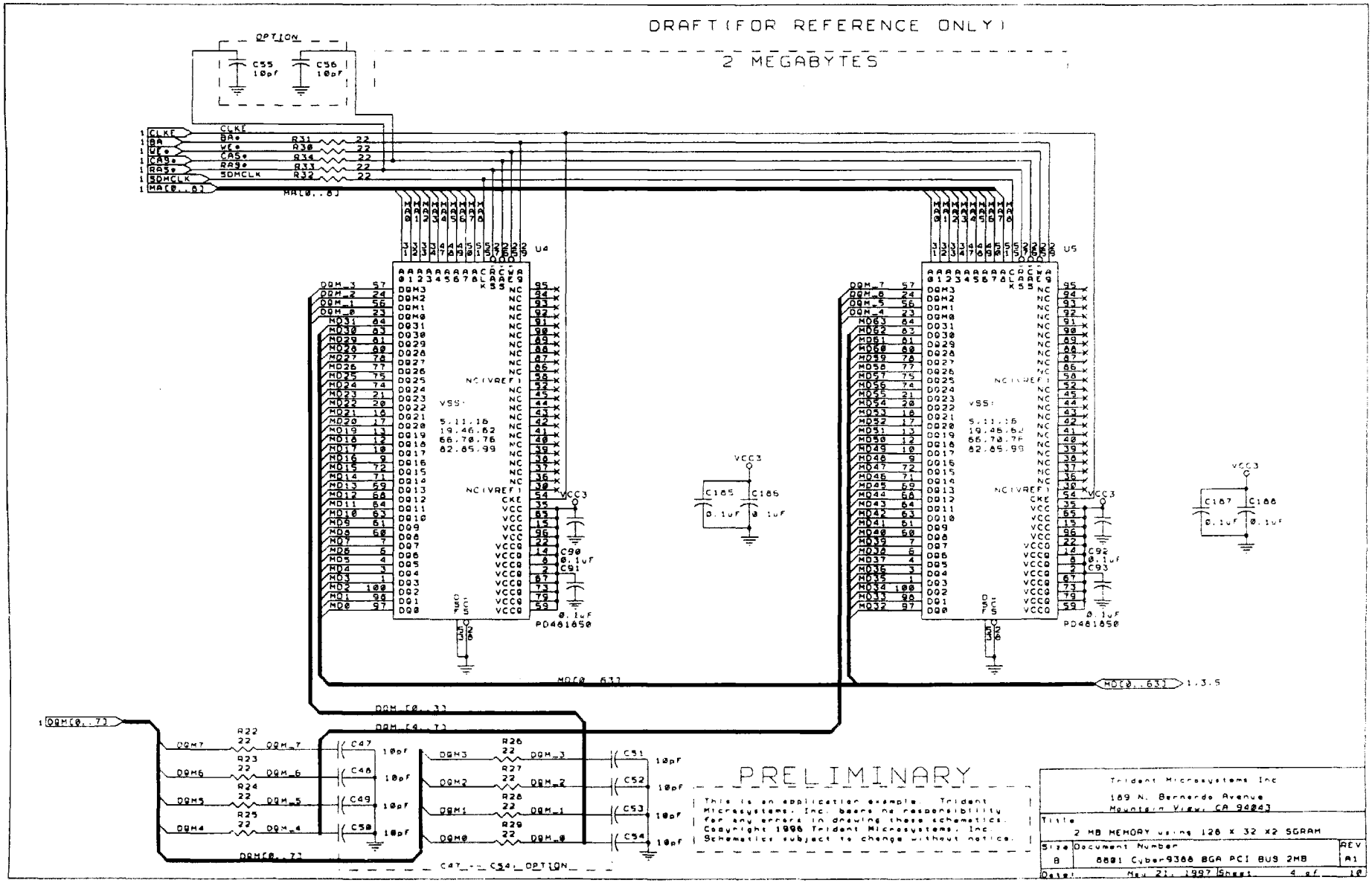
Trident Microsystems Inc
189 N. Bernardo Avenue
Mountain View, CA 94043
Title
Cyber9388 BGA (Princeville) 2/2
Size B
Document Number
8881 Cyber9388 BGA PCI BUS 2MB
REV A1
Date: May 22, 1997 Sheet 2 of 10


DRAFT (FOR REFERENCE ONLY)
PCI LOCAL BUS
BIOS
PRELIMINARY
PCI_CON32 UNIVERSAL
PCI BUS & ROMBIOS INTERFACE
Trident Microsystems Inc
189 N. Bernardo Avenue
Mountain View, CA 94043
8881 Cyber9388 BGA PCI BUS 2MB
Date: May 22, 1997


DRAFT (FOR REFERENCE ONLY)
2 MEGABYTES
OPTION
C55 10pF
C56 10pF
CLKE
BA*
WE*
CAS*
RAS*
SDMCLK
MA[0..8]
R31 22
R30 22
R34 22
R33 22
R32 22
U4
U5
PD481850
VCC3
C90 0.1uF
C91
C92
C93
C185 0.1uF
C186 0.1uF
C187 0.1uF
C188 0.1uF
MD[0..63]
DQM[0..7]
DQM_F0..3]
DQM_F4..7]
R22
R23
R24
R25
R26
R27
R28
R29
C47 10pF
C48 10pF
C49 10pF
C50 10pF
C51 10pF
C52 10pF
C53 10pF
C54 10pF
C47_-_C54_OPTION
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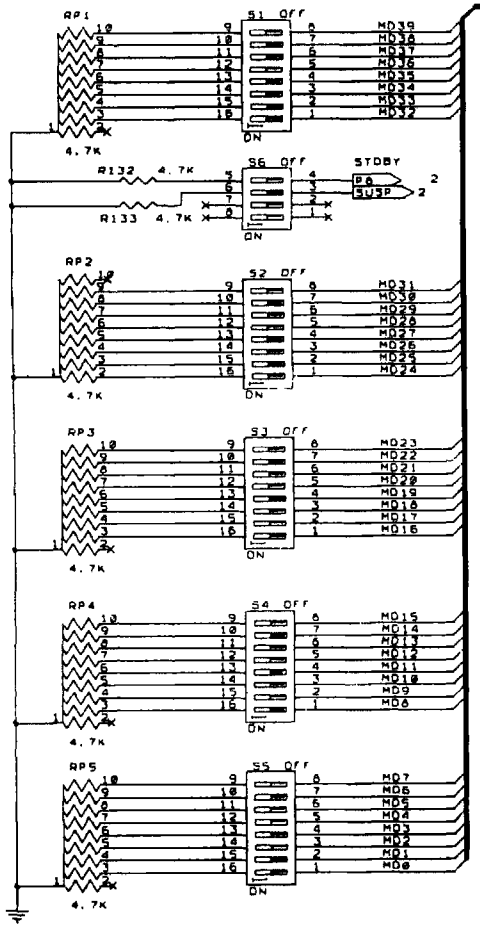
Title
2 MB MEMORY using 128 x 32 x2 SGRAM
Size B
Document Number 8881 Cyber9388 BGA PCI BUS 2MB
REV A1
Date: May 21, 1997 Sheet 4 of 10

CONFIG & MISCELLANEOUS CONTROL

DRAFT (FOR REFERENCE ONLY)



NOTE: SWITCH OFF = 1; ON = 0

MD[0..31] MD[0..32] 1.3.4

MD[39:32]: GENERAL PURPOSE, RESERVED FOR PCI SUBSYSTEM.

ON: STDBY; OFF: RESUME

ON: SUSP; OFF: RESUME

MD[31:28]: RESERVED
MD[27:24]: PANEL TYPE SELECT

	TFT		DSTN
0000	6X4-18	1000	6X4-18
0001	8X6-18	1001	8X6-18
0010	10X7-18	1010	10X7-18
0011	10X7-18+18	1011	10X7-24
0100	12X10-18+18	1100	12X10-24
0101	10X6-18	1101	10X6-18
0110	10X6-18+18	1110	10X6-24
0111	RESERVED	1111	RESERVED

MD23: RESERVED
MD22: DISPLAY TYPE: 0 = SIMULTANEOUS; 1 = TV ONLY
MD21: FSC SELECT: 0 = X4; 1 = X1
MD20: DISPLAY TYPE; 0 = TV; 1 = CRT
MD19: TV OUT STANDARD: 0 = NTSC; 1 = PAL
MD18: PCI MASTER: 0 = ENABLE; 1 = DISABLE
MD17: PCI TARGET: 0 = ENABLE; 1 = DISABLE
MD16: MMIO CONTROL: 0 = ENABLE; 1 = DISABLE

MD15: MEMORY I/F CONTROL: 0 = TRI-STATED; 1 = NORMAL
MD14: CLOCK SOURCE SELECT: 0 = EXTERNAL; 1 = INTERNAL
MD13: VIDEO SUBSYSTEM ENABLE: 0 = 46E8; 1 = 3C3
MD12: BIOS SIZE: 0 = 64K; 1 = 32K
MD[11:10]: MEMORY INTERFACE CONTROL: 00 = RESERVED 01 = INTERNAL AND EXTERNAL MEMORY
10 = EXTERNAL MEMORY ONLY 11 = INTERNAL MEMORY ONLY
MD9: LINEAR/BANK ADDRESSING CONTROL 0 = LINEAR ONLY; 1 = LINEAR/BANK
MD8: BIOS CONTROL: 0 = DISABLE; 1 = ENABLE

MD[7:5]: GENERAL PURPOSE, RESERVED

MD4: LCD ON/OFF CONTROL: 0 = LCD OFF; 1 = LCD ON
MD3: READ LATENCY CONTROL: 0 = 3 CLOCK-CYCLE; 1 = 2 CLOCK-CYCLE
MD[2:0]: MEMORY CLOCK CONTROL(MHz)
000=60 001=75 010=90 011=120 100=66 101=83 110=100 111=132

PRELIMINARY

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Schematics subject to change without notice

Trident Microsystems, Inc
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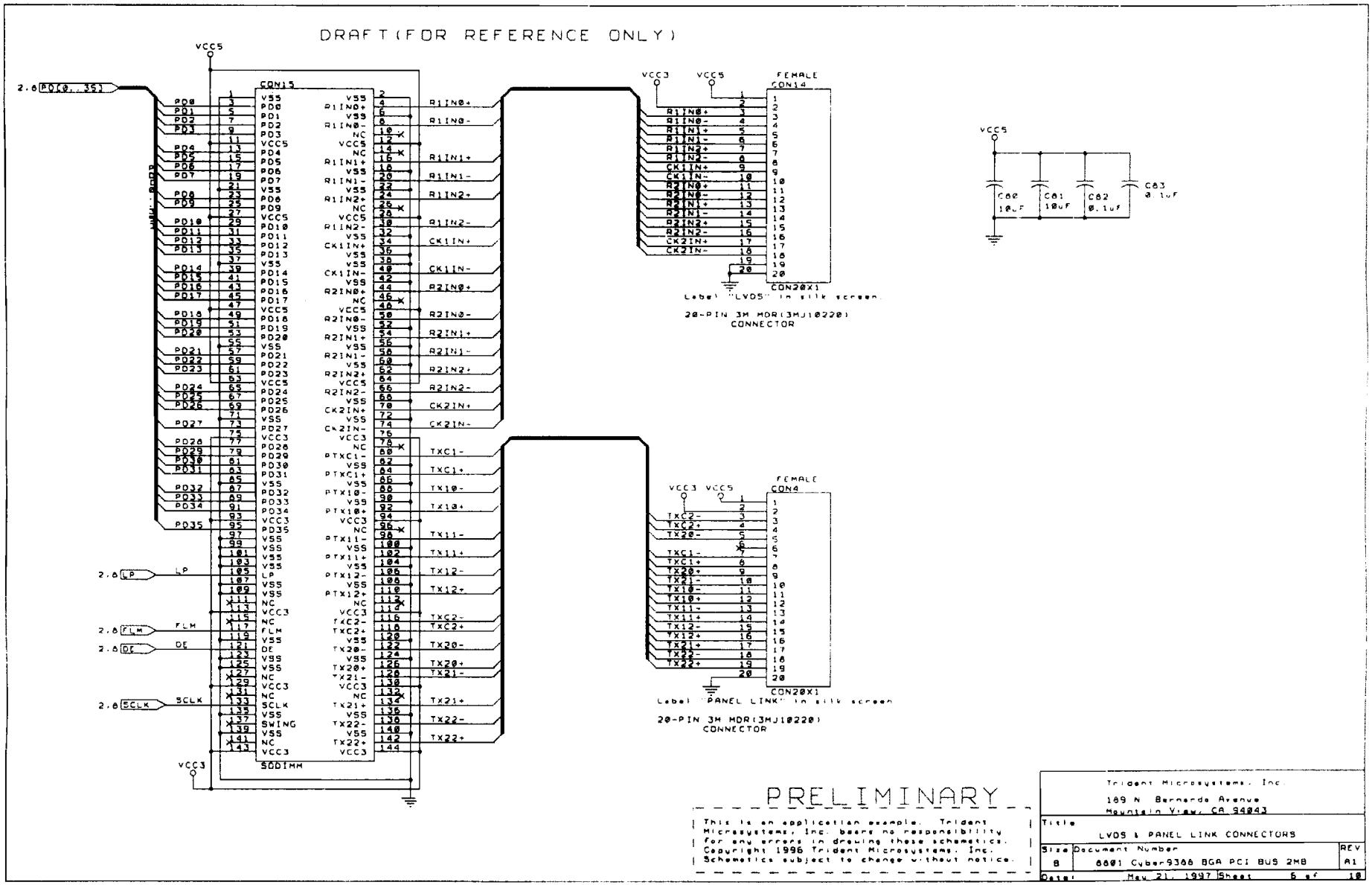
Mountain View, CA 94043

Title: CONFIGURATION AND MISCELLANEOUS

Size	Document Number	REV
B	6881 Cyber9388 BGA PCI BUS 2MB	A1

Date: May 22, 1997 Sheet 5 of 10


DRAFT (FOR REFERENCE ONLY)
VCC5
CON15
SODIMM
2.6 PD[0..35]
LP
FLM
DE
SCLK
VCC3
R1IN0+
R1IN0-
R1IN1+
R1IN1-
R1IN2+
R1IN2-
CK1IN+
CK1IN-
R2IN0+
R2IN0-
R2IN1+
R2IN1-
R2IN2+
R2IN2-
CK2IN+
CK2IN-
TXC1-
TXC1+
TX10-
TX10+
TX11-
TX11+
TX12-
TX12+
TXC2-
TXC2+
TX20-
TX20+
TX21-
TX21+
TX22-
TX22+
FEMALE
CON14
CON20X1
Label "LVDS" in silk screen
20-PIN 3M MDR(3MJ10220)
CONNECTOR
C80
10uF
C81
10uF
C82
0.1uF
C83
0.1uF
FEMALE
CON4
Label "PANEL LINK" in silk screen
20-PIN 3M MDR(3MJ10220)
CONNECTOR
PRELIMINARY
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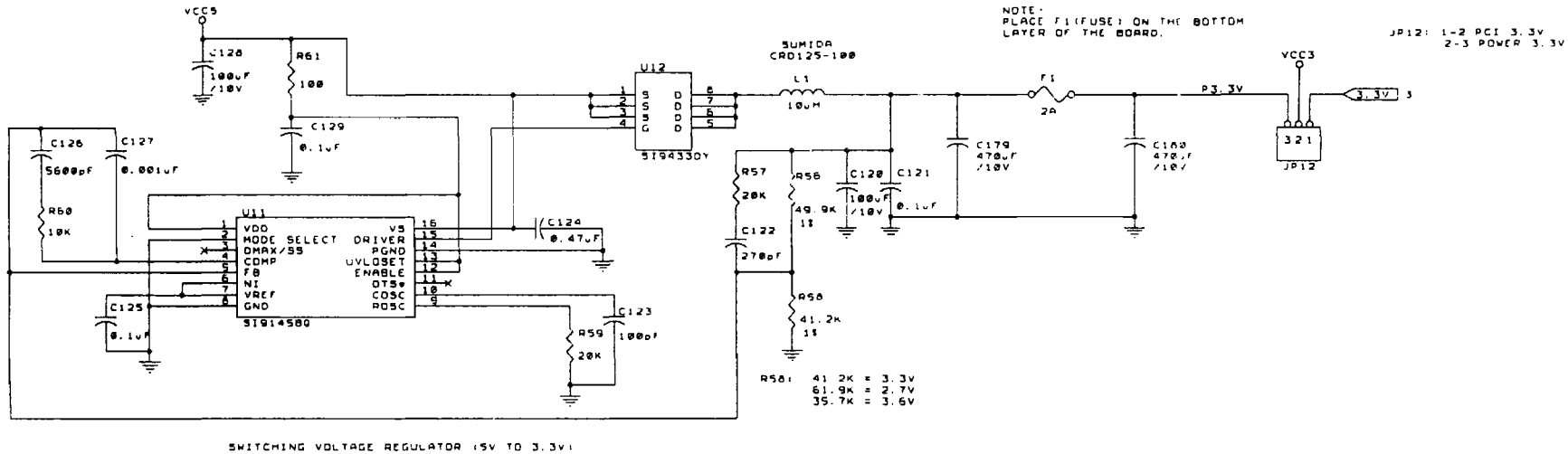
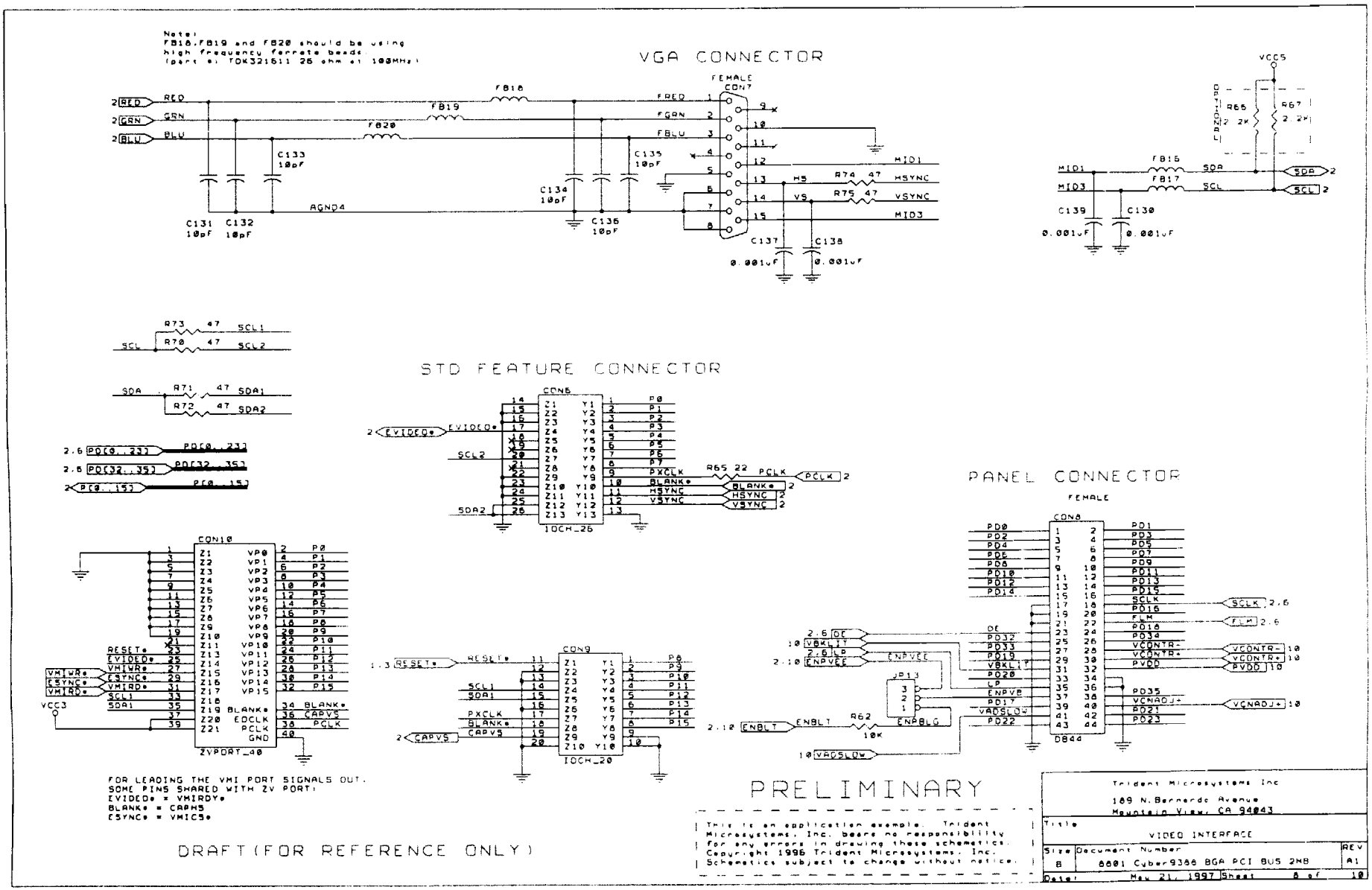
189 N. Bernardo Avenue
Mountain View, CA 94043
Title
LVDS & PANEL LINK CONNECTORS
Size
B
Document Number
8601 Cyber9388 BGA PCI BUS 2MB
REV
A1
Date: May 21, 1997 Sheet 6 of 10

DRAFT (FOR REFERENCE ONLY)

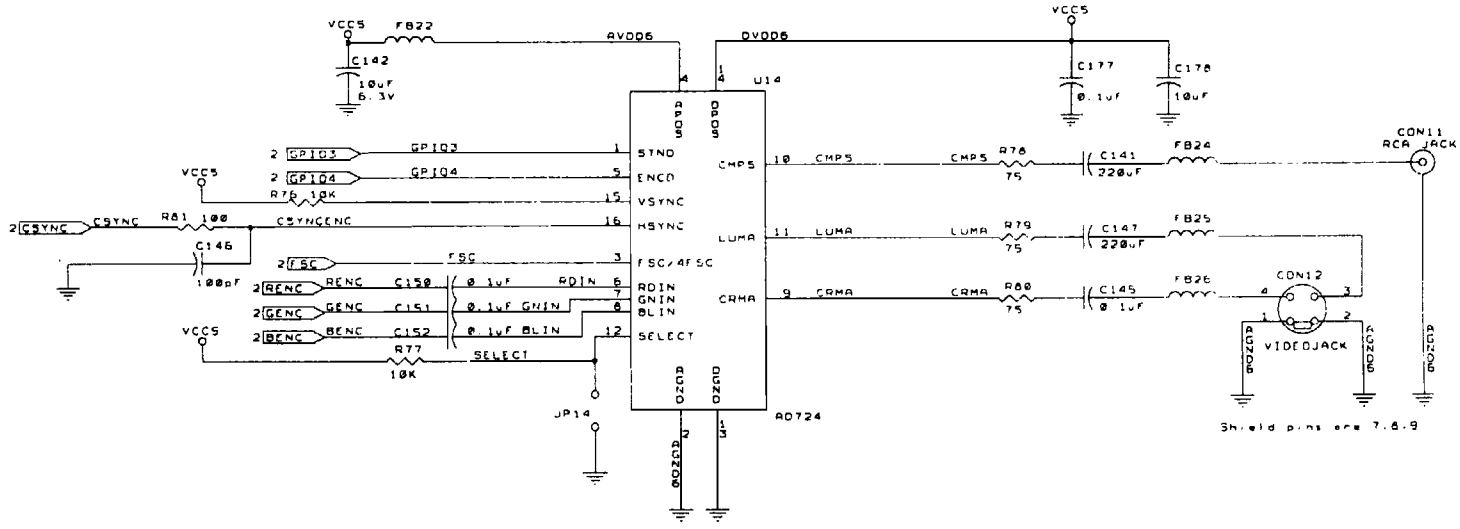


SWITCHING VOLTAGE REGULATOR (5V TO 3.3V)

Trident Microsystems Inc. 189 North Bernardo Avenue Mountain View, CA 94043-5203		
Title: 3.3V POWER SUPPLY		
Size: B	Document Number: 8881 Cyber9388 BGA PCI BUS 2MB	REV: A1
Date: May 21, 1997	Sheet: 7 of 10	


VGA CONNECTOR
STD FEATURE CONNECTOR
PANEL CONNECTOR
PRELIMINARY
DRAFT(FOR REFERENCE ONLY)
VIDEO INTERFACE
Trident Microsystems Inc
189 N.Bernardo Avenue
Mountain View, CA 94043

DRAFT(FOR REFERENCE ONLY)



PRELIMINARY

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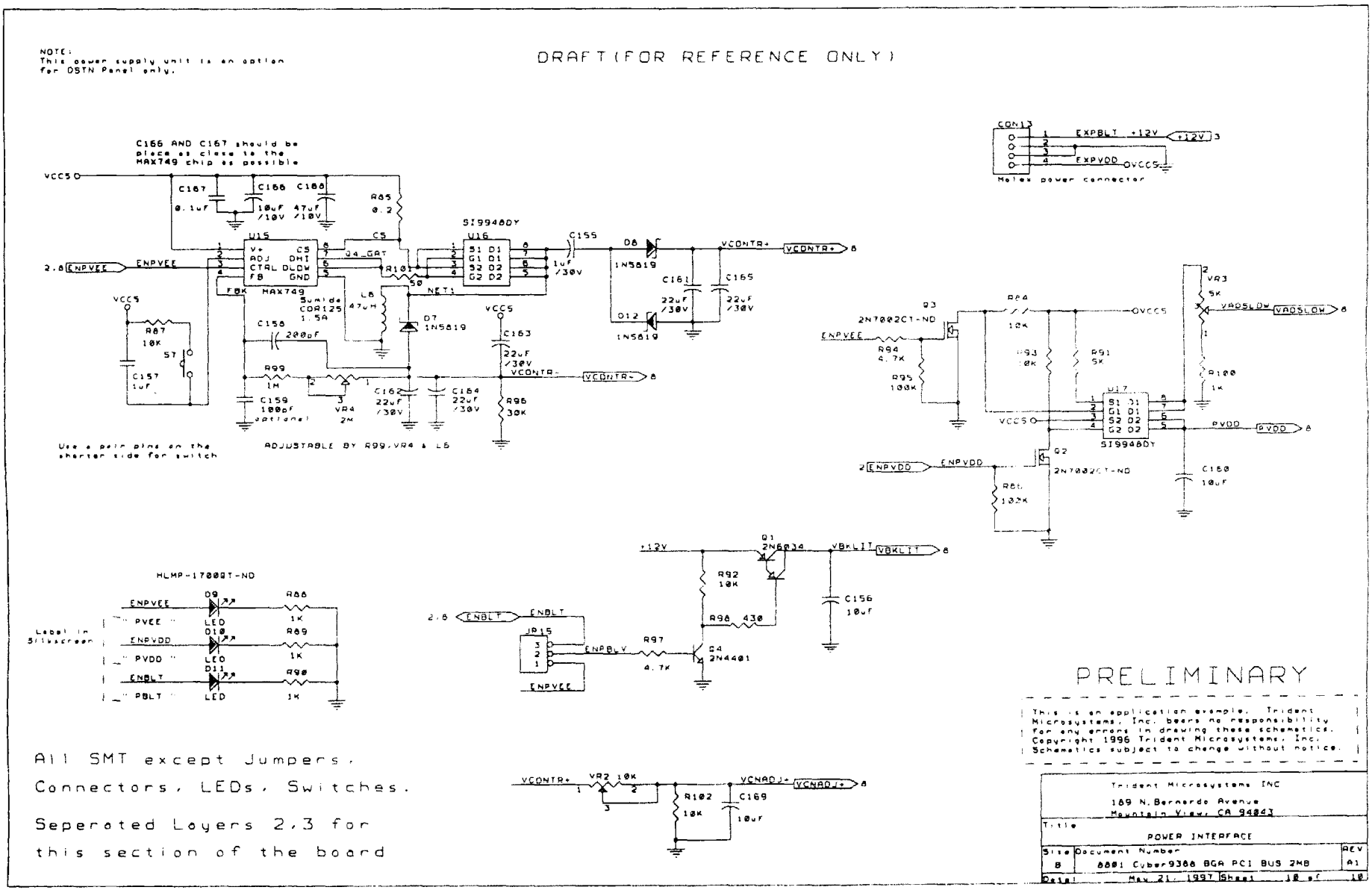
189 North Bernado Avenue
Mountain View, CA 94043

Title: RGB ENCODER

Size	Document Number	REV
B	8691 Cyber9388 BGA PCI BUS 2MB	A1

Date: May 21, 1997 Sheet 9 of 10


NOTE:
This power supply unit is an option for DSTN Panel only.
DRAFT (FOR REFERENCE ONLY)
C166 AND C167 should be place as close to the MAX749 chip as possible
Use a pair pins on the shorter side for switch
ADJUSTABLE BY R99,VR4 & L5
HLMP-1700#T-ND
All SMT except Jumpers, Connectors, LEDs, Switches.
Seperated Layers 2,3 for this section of the board
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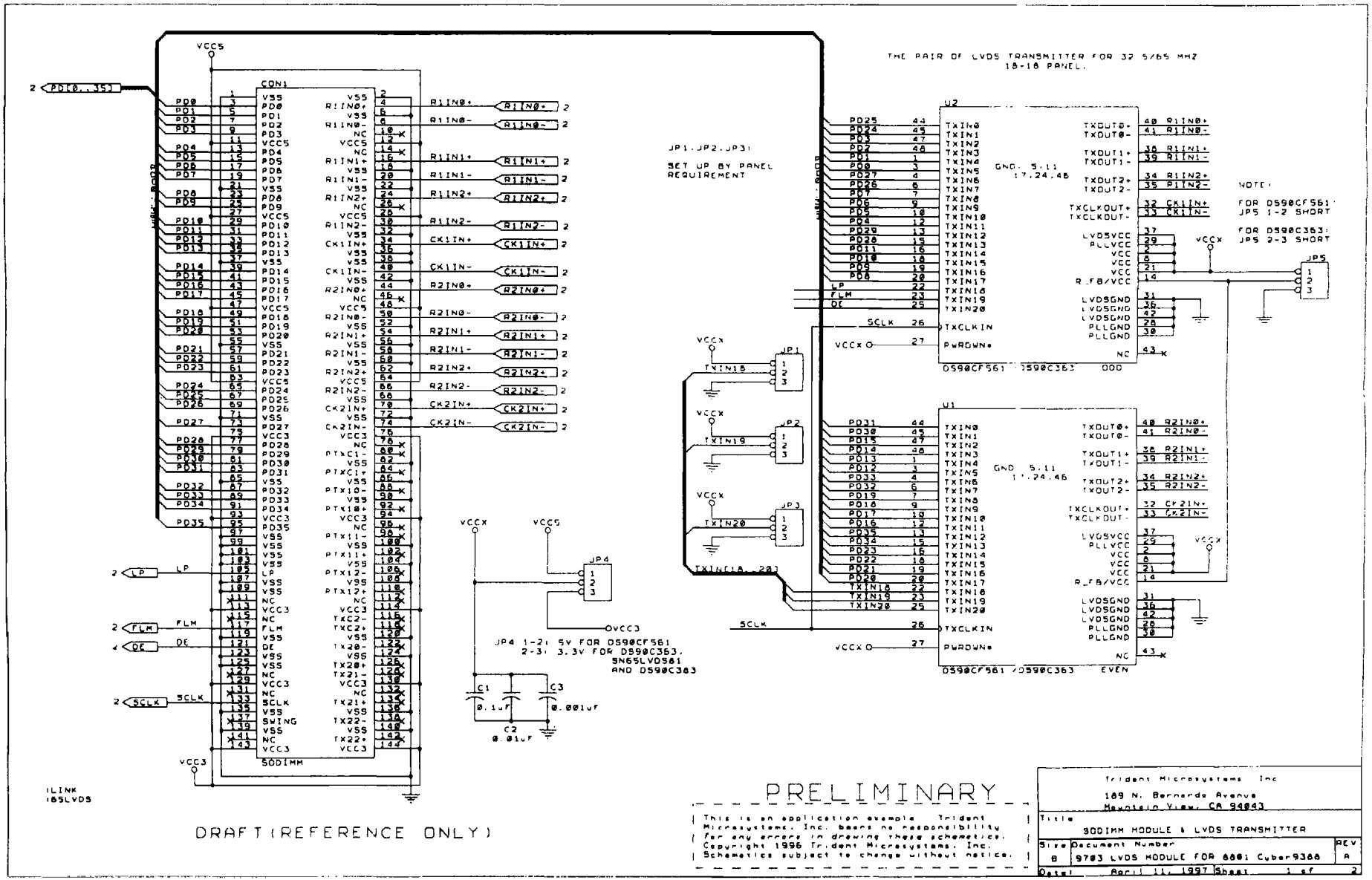
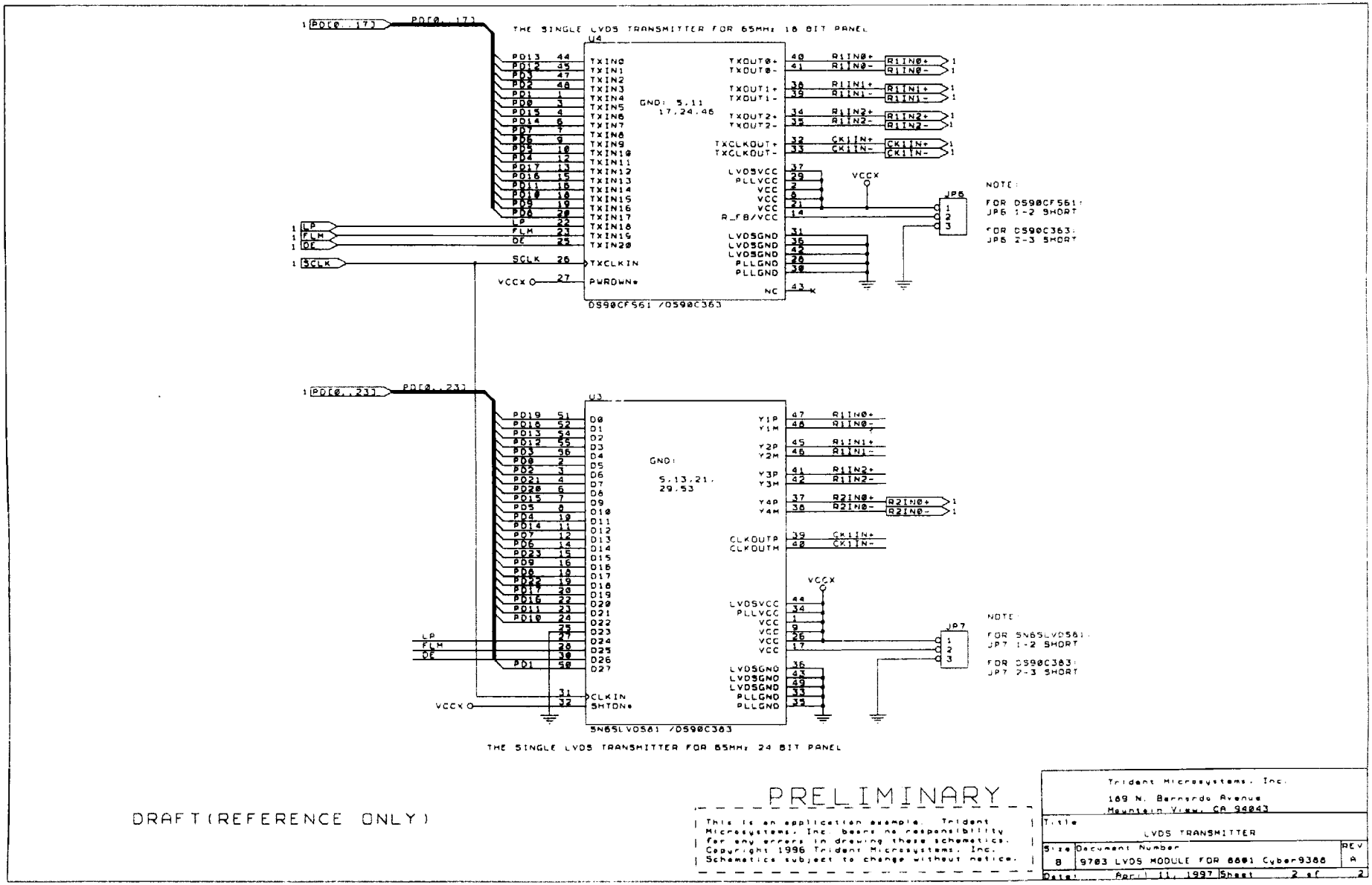
Trident Microsystems INC
189 N. Bernardo Avenue
Mountain View, CA 94043
Title
POWER INTERFACE
Size B
Document Number 8881 Cyber9388 BGA PCI BUS 2MB
REV A1
Date: May 21, 1997 Sheet 10 of 10



DRAFT (REFERENCE ONLY)


THE SINGLE LVDS TRANSMITTER FOR 65MHz 18 BIT PANEL
U4
DS90CF561 /DS90C363
GND: 5,11 17,24,46
VCCX
NOTE:
FOR DS90CF561: JP6 1-2 SHORT
FOR DS90C363: JP6 2-3 SHORT
U3
SN65LVDS61 /DS90C383
GND: 5,13,21, 29,53
NOTE:
FOR SN65LVDS61: JP7 1-2 SHORT
FOR DS90C383: JP7 2-3 SHORT
THE SINGLE LVDS TRANSMITTER FOR 65MHz 24 BIT PANEL
DRAFT(REFERENCE ONLY)
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189 N. Bernardo Avenue
Mountain View, CA 94043
Title
LVDS TRANSMITTER
Size B
Document Number 9703 LVDS MODULE FOR 8691 Cyber9388
REV A
Date: April 11, 1997 Sheet 2 of 2

Contact your local Trident representative for:

- Technical Reference Manuals
- Software Programmer's Guides
- Evaluation Kits (Documentation plus evaluation board and software)

USA	Taiwan	Hong Kong
Trident Microsystems, Inc. 189 North Bernardo Avenue Mountain View, CA 94043-5203 Phone: 415 / 691-9211 Fax: 415 / 968-0820 BBS: 415 / 691-1016 Website: http://www.trid.com	Trident Microsystems (Far East), Ltd. Taiwan Branch 18F, No. 202, Sec 2 Yen Ping North Road Taipei, Taiwan, R.O.C. Phone: 886-2-577-5299 Fax: 886-2-577-1608	Trident Microsystems (Far East), Ltd. Unit 6, 19F, Tower II Enterprise Square 9 Sheung Yuet Road, Kowloon Bay Kowloon, Hong Kong Phone: 852-2756-9666 Fax: 852-2796-9849

Trident