Ordering number : ENA0249

Discontinued

SANYO Semiconductors

DATA SHEET

Monolithic Linear IC

LA75675M — For Use in TV/VTR Applications IF Signal Processing (VIF+SIF)

Overview

This LA75675M is IF signal processing (VIF+SIF) for use in TV/VTR applications.

Functions

- VIF Block: VIF Amplifier, Buzz Canceller, PLL Detector, IF AGC, RF AGC, AFT, Equalizer Amplifier
- SIF Block: Limiter Amplifier, PLL FM Detector

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V13, V17		V_{CC}	V
Circuit current	I_6		-3	mA
	I_{10}		-10	mA
	I_{24}		-2	mA
Allowable power dissipation	Pd max	Ta ≤ 50°C, Independent IC	420	mW
		* Mounted on a board	720	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* When mounted on a 65×72×1.6mm^3 paper phenol board.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage	VCC op		4.5 to 5.5	V

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Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, fp = 45.75MHz

VIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_5		32	40	48	mA
Maximum RF AGC voltage	$V_{14}H$		V_{CC}-0.5	V_{CC}		V
Minimum RF AGC voltage	$V_{14}L$			0	0.5	V
Input sensitivity	Vi	S1 = OFF	32	38	44	dBμV
AGC range	GR		58	63		dB
Maximum allowable input	Vi max		95	100		dBμV
No-signal video output voltage	V_6		3.5	3.8	4.1	V
Sync. signal tip voltage	V_6tip		0.9	1.2	1.5	V
Video output level	Vo		1.7	2	2.3	Vp-p
Black noise threshold voltage	V_{BTH}		0.5	0.8	1.1	V
Black noise clamp voltage	V_{BCL}		1.6	1.9	2.2	V
Video S/N	S/N		48	52		dB
C-S best	IC-S		38	43		dB
Frequency characteristics	fc	6MHz	-3	-1.5		dB
Differential gain	DG			3	6.5	%
Differential phase	DP			3	5	°C
No-signal AFT voltage	V_{13}		2.0	2.5	3.0	V
Maximum AFT voltage	$V_{13}H$		4.0	4.4	5.0	V
Minimum AFT voltage	$V_{13}L$		0	0.18	1.0	V
AFT detection sensitivity	Sf		28	40	52	mV/kHz
VIF input resistance	Ri	45.75MHz		1.5		kΩ
VIF input capacitance	Ci	45.75MHz		3		pF
APC pull-in range (U)	fpu		1.3	2.0		MHz
APC pull-in range (L)	fpl			-2.0	-1.4	MHz
AFT tolerance frequency 1	dfa1		-150	0	+150	kHz
VCO1 maximum variable range (U)	dfu		1.5	2.0		MHz
VCO1 maximum variable range (L)	dfl			-2.0	-1.5	MHz
VCO control sensitivity	β		1.3	2.7	5.4	kHz/mV

SIF Block

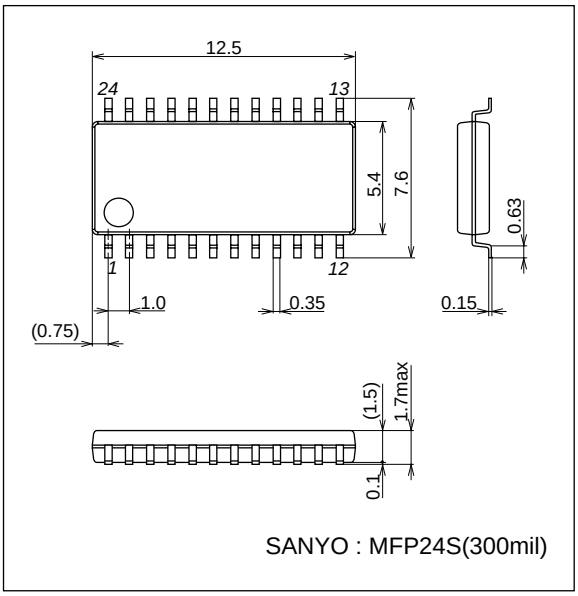
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Limiting sensitivity	Vi (lim)		39	45	51	dBμV
FM detector output voltage	Vo (FM)	4.5MHz ± 25kHz	400	520	660	mVrms
AM rejection ratio	AMR		50	60		dB
Distortion	THD			0.3	0.8	%
SIF S/N	S/N (FM)		59	64		dB
4.5MHz output level	Vsout	SIF IN, 80dBμV	82	89	96	dBμV

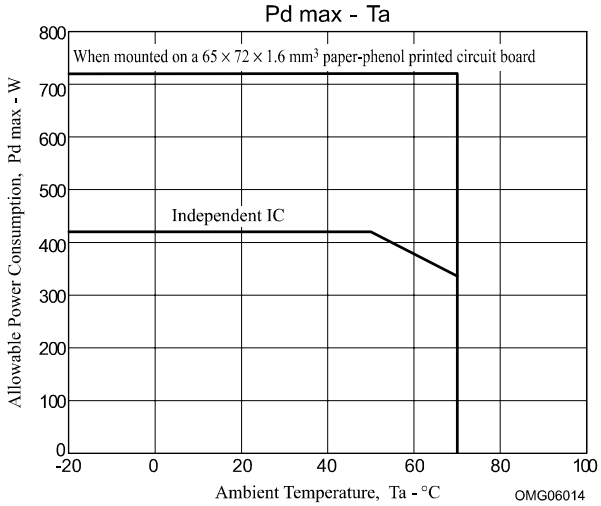
* IF the dynamic range of the FM detection output needs to be widened, connect a resistor and a capacitor in series between pin 23 and GND for level adjustment.

Package Dimensions

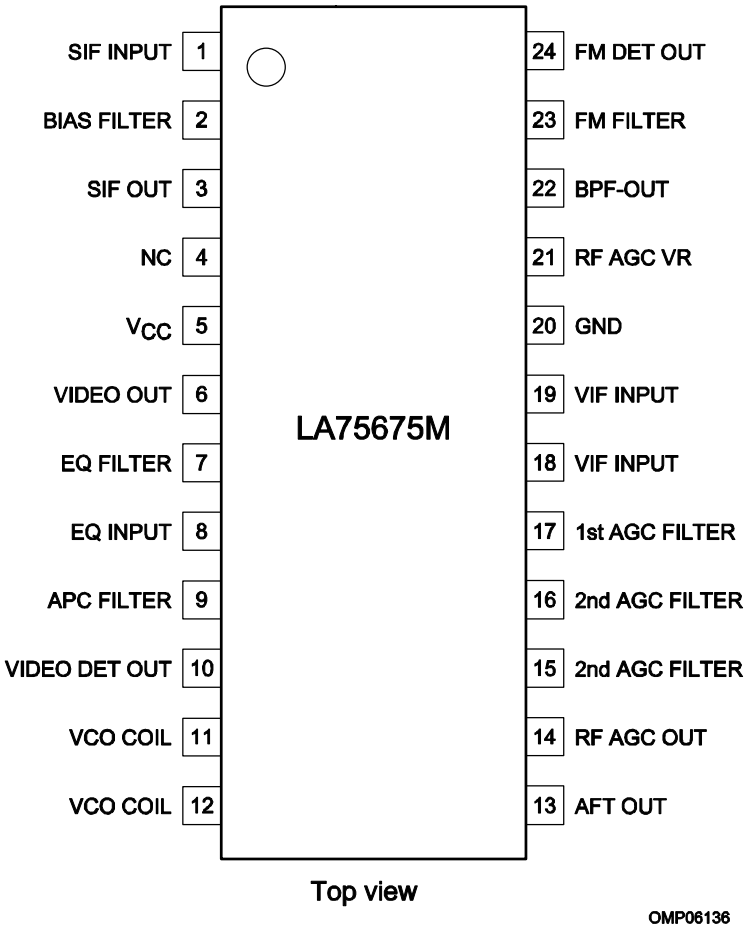
unit : mm

3112B

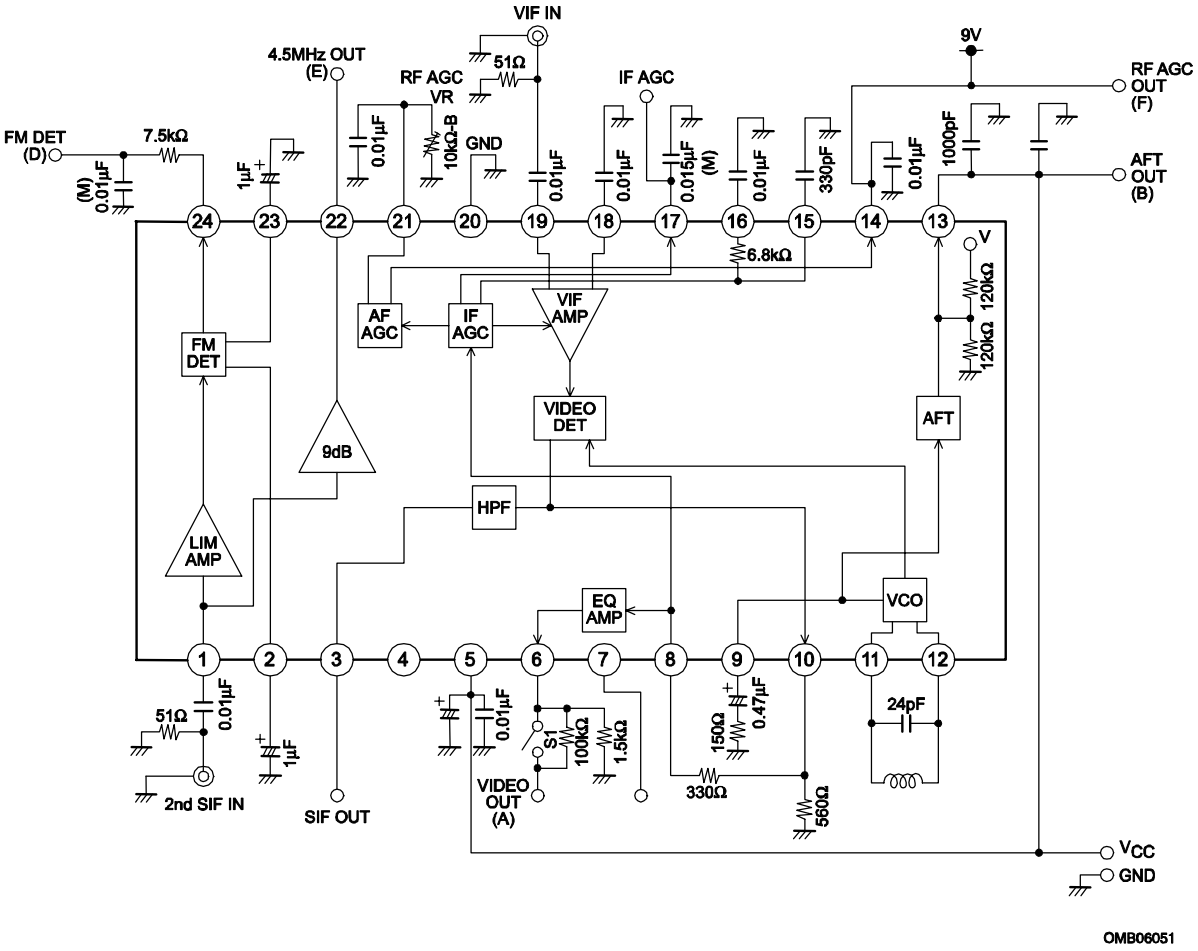




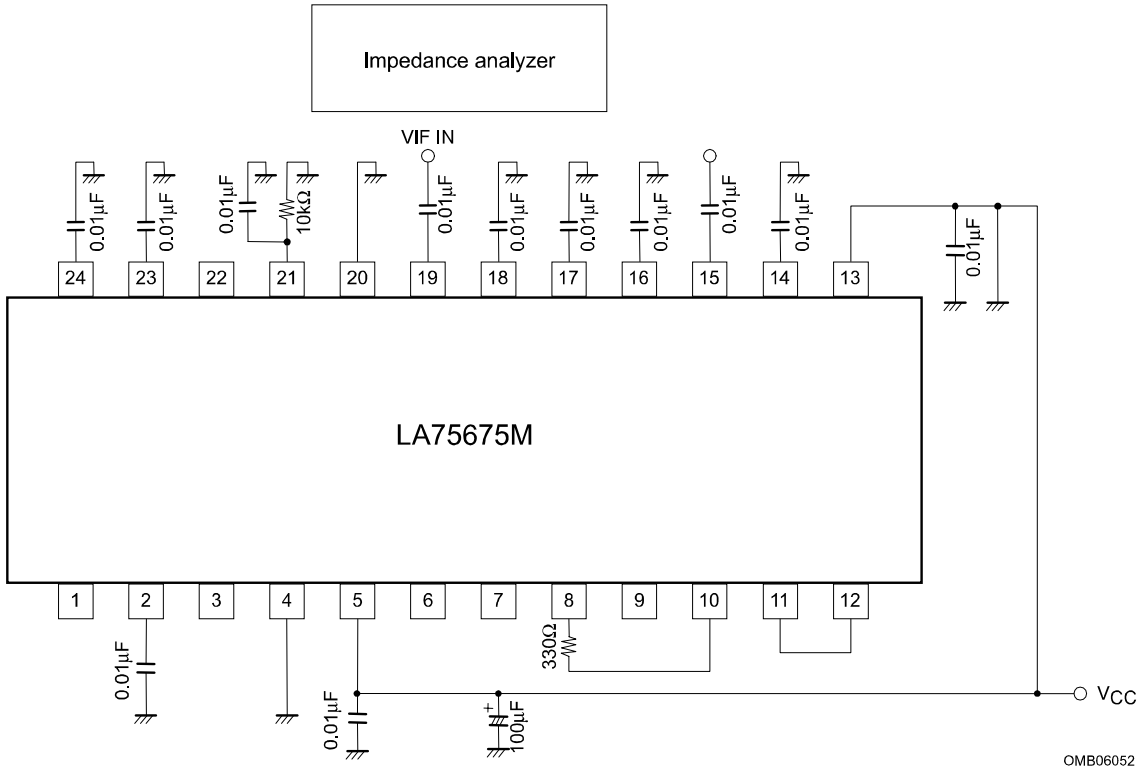
Pin Assignment



Block Diagram and AC Characteristics Test Circuit



Test Circuit



Test Conditions

V1. Circuit current [I_5]
(1) Internal AGC
(2) Input a 45.75MHz, 10mVrms, continuous wave to the VIF input pin.
(2) RF AGC Vr MAX
(3) Connect an ammeter to the V_{CC} and measure the incoming current.

V2. V3. Maximum RF AGC voltage, Minimum RF AGC voltage [$V_{14}H$, $V_{14}L$]
(1) Internal AGC
(2) Input a 45.75MHz, 10mVrms, continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistance max.) and measure the maximum RF AGC voltage. ····· $V_{14}H$
(4) Adjust the RF AGC Vr (resistance min.) and measure the minimum RF AGC voltage. ····· $V_{14}L$

V4. Input sensitivity [Vi]
(1) Internal AGC
(2) fp = 45.75MHz 400Hz 40% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) Measure the VIF input level at which the 400Hz detection output level at test point A becomes 0.64Vp-p.

V5. AGC range [GR]
(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) In the same manner under the same conditions as for V4 (input sensitivity), measure the VIF input level at which the detection output level becomes 0.64Vp-p. ····· Vil
(3) $GR = 20\log \frac{Vil}{Vi}$ dB

V6. Maximum allowable input [Vi max]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A becomes video output (Vo) ±1dB.

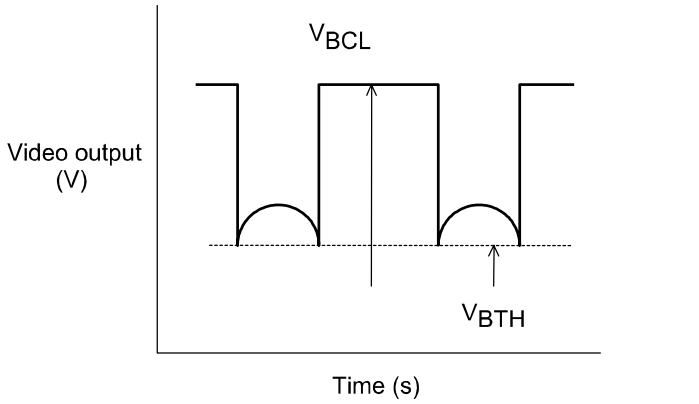
V7. No-signal video output voltage [V_6]
(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage at the VIDEO output (A).

V8. Sync. signal tip voltage [V_6tip]
(1) Internal AGC
(2) Input a 45.75MHz, 10mVrms, continuous wave to the VIF input pin.
(3) Measure the DC voltage at the VIDEO output (A).

V9. Video output level [Vo]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM Vi = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. (Vp-p)

V10. V11. Black noise threshold level and clamp voltage [V_{BTH}, V_{BCL}]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and vary it.
(2) fp = 45.75MHz 400Hz 40% AM 10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the V_{BTH}, V_{BCL} at test point A.



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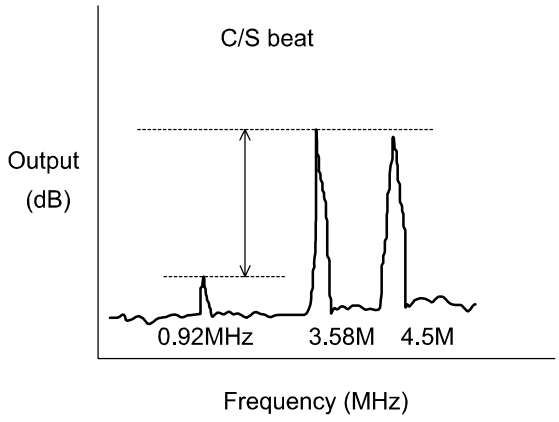
V12. Video S/N [S/N]

(1) Internal AGC
(2) fp = 45.75MHz CW = 10mVrms (VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
····· Noise voltage (N)

(4) $S/N = 20\log \frac{\text{Video position (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20\log \frac{1.12\text{Vp-p}}{\text{Noise voltage}}$ (dB)

V13. C/S beat [IC-S]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and vary it.
(2) fp = 45.75MHz CW; 10mVrms
fc = 42.17MHz CW; 10mVrms – 10dB
fs = 41.25MHz CW; 10mVrms – 10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 1.3Vp-p.
(4) Measure the difference between the levels for 3.58MHz and 0.92MHz components at test point A.



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V14. Frequency characteristics [fc]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and vary it.
(2) SG1 : 45.75MHz continuous wave 10mVrms
SG2 : 45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p. ····· V1
(4) Set the SG2 frequency to 39.75MHz and measure the output level. ····· V2
(5) Calculate as follows :

$$fc = 20\log \frac{V2}{V1} \text{ dB}$$

V15. V16. Differential gain, differential phase [DG, DP]

(1) Internal AGC
(2) fp = 45.75MHz APL50% 87.5% Modulation video signal Vi = 10mVrms
(3) Measure the DG and DP at test point A.

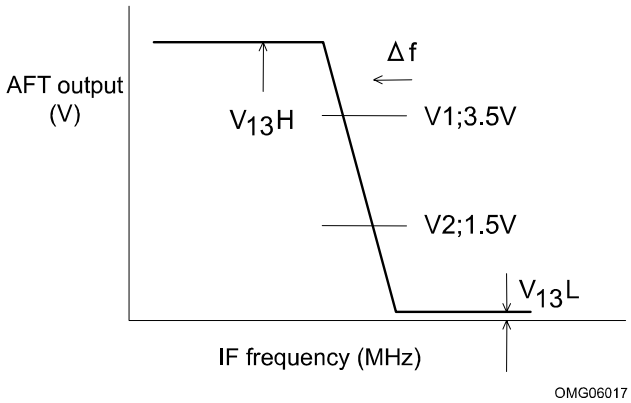
V17. No-signal AFT voltage [V_{13}]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V18. V19. V20. Maximum, minimum AFT output voltage, AFT detection sensitivity [$V_{13}H$, $V_{13}L$, Sf]

(1) Internal AGC
(2) fp = 45.75MHz ±1.5MHz, Sweep = 10mVrms (VIF input)
(3) Maximum voltage : $V_{13}H$, minimum voltage : $V_{13}L$.
(4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2. ····· Δf

$$Sf = \frac{2000(mV)}{\Delta f(kHz)} \text{ mV/kHz}$$



V21. V22. VIF input resistance, Input capacitance [Ri, Ci]

(1) Referring to the Input Impedance Test Circuit, measure Ri and Ci with an impedance analyzer.

V23. V24. APC pull-in range [fpu, fpl]

(1) Internal AGC
(2) fp = 39MHz to 51MHz CW; 10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 45.75MHz to bring the PLL to unlocked state.
Note : The PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. ····· f1
(5) Lower the SG signal frequency to bring the PLL to unlock state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. ····· f2
(7) Calculate as follows :

fpu = f1 – 45.75MHz
fpl = f2 – 45.75MHz

V25. AFT tolerance frequency 1 [ΔFa1]

(1) Internal AGC
(2) SG1 : 43.75MHz to 47.75MHz variable CW 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the V17.)
(5) Apply 9V to the IFAGC (pin 17) and then pick up the VCO oscillation frequency from the GND, etc.; that frequency is f2.
(6) Calculate as follows :

AFT tolerance frequency : ΔFa1 = f2 – f1 (kHz)

V26. V27. VCO maximum variable range (U, L) [dfu, dfl]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9).
In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).

dpu = fu – 45.75MHz
dfl = fl – 45.75MHz

V28. VCO control sensitivity [β]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) f1 is taken as the frequency when 3.0V is applied to the APC pin (pin 9).
In the same manner, f2 is taken as the frequency when 3.4V is applied to the APC pin (pin 9).

$$\beta = \frac{f2-f1}{400} \text{ (kHz/mV)}$$

S1. SIF Limiting sensitivity [Vi (lim)]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz ΔF = ±25kHz (SIF input)
(3) Set the SIF input level to 100mVrms and then measure the level at test point D. ····· V1
(4) Lower the SIF input level until V1–3dB occurs. Measure the input level at that moment.

S2. S4. FM detection output voltage, distortion [Vo (FM), THD]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz ΔF = ±25kHz (SIF input Vi = 100mVrms)
(3) Assign the level at test point D to the FM detection output voltage and measure the distortion factor.

S3. AM rejection ratio [AMR]

(1) Apply the VCC voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz AM = 30% (SIF input Vi = 100mVrms)
(3) Measure the output level at test point D. ····· VAM

(4) $AMR = 20\log \frac{Vo\ (FM)}{VAM}$ dB

S5. SIF S/N [S/N(FM)]

(1) External AGC ($V17 = V_{CC}$)
(2) fs = 4.5MHz NO MOD Vi = 100mVrms
(3) Measure the output level at test point D. ····· Vn

(4) $S/N = 20\log \frac{Vo\ (FM)}{Vn}$ dB

S6. 4.5MHz output level [Vsout]

(1) External AGC ($V_{17} = V_{CC}$)
(2) fs = 4.5MHz NO MOD Vi = 10mVrms
(3) Measure the output level at test point E. ····· Vsout

Note 1) Unless otherwise specified for VIF test, apply the VCC voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.7MHz.
2) Unless otherwise specified, leave the SW1 turned ON.