Order number: MC100ES60T23
Rev 0, 05/2004

Product Preview

3.3 V Dual Differential LVPECL-to-LVTTL Translator

The MC100ES60T23 is a dual differential LVPECL-to-LVTTL translator. The low voltage PECL levels, small package, and dual gate design is ideal for clock translation applications.

Features

- Maximum Frequency > 180 MHz
- Differential LVPECL Inputs
- LVPECL Operating Range: V_{CC} = 3.0 V to 3.6 V
- 24 mA LVTTL Compatible Outputs
- 8-Lead SOIC and 8-Lead TSSOP Packages
- Ambient Temperature Range: –40°C to +85°C

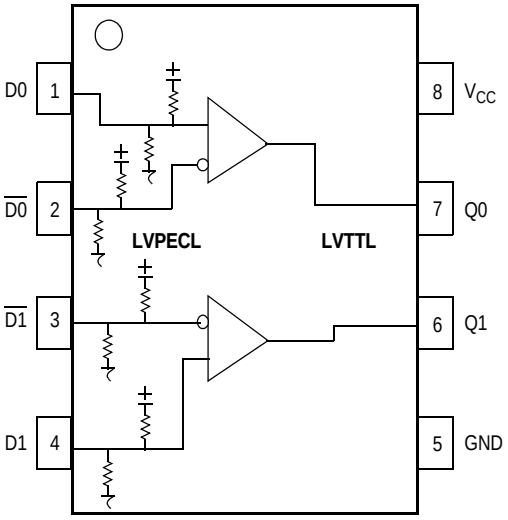

Figure 1. 8-Lead Pinout (Top View**) and Logic Diagram**

MC100ES60T23

DUAL LVPECL TO LVTTL TRANSLATOR

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

DT SUFFIX
8-LEAD TSSOP PACKAGE
CASE TBD

ORDERING INFORMATION

Device	Package
MC100ES60T23D	SO-8
MC100ES60T23DR2	SO-8
MC100ES60T23DT	TSSOP-8
MC100ES60T23DTR2	TSSOP-8

PIN DESCRIPTION

Pin	Function
Qn	LVTTL Outputs
Dn, $\overline{Dn}$	LVPECL Differential Inputs
V_{CC}	Positive Supply
GND	Negative Supply

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor	D $\overline{D}$	75 kΩ 112.5 kΩ
Internal Input Pullup Resistors		75 kΩ
ESD Protection	Human Body Model Machine Model	> 2000 V > 200 V
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	190 °C/W 130 °C/W
	0 LFPM, 8 TSSOP 500 LFPM, 8 TSSOP	TBD TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} and V_{EE}	3.9	V
V_{IN}	Input Voltage	V_{CC}–V_{EE} ≤ 3.6 V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. LVPECL Input DC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{CCH}	Power Supply Current (Outputs set to HIGH)		18	25		18	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)		26	33		26	33	mA
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{PP}	Differential Input Voltage[1]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[2]	V_{EE} +1.5		V_{CC}–0.65	V_{EE} +1.5		V_{CC}–0.65	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	 –150		0.5	 –150		0.5	μA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. LVTTL / LVCMOS Output DC Characteristics (V_{CC} = 3.0 to 3.6 V)

Symbol	Characteristic	Condition	–40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –24 mA	2.4			2.4			V
V_{0L}	Output LOW Voltage	I_{OL} = 24 mA			0.5			0.5	V
I_{0S}	Output Short Circuit Current			–150			–150		mA

Table 5. AC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency[2]	180			180			180			MHz
t_{PLH} t_{PHL}	Propagation Delay	1.0	1.5	2.5	1.0	1.7	2.5	1.0	1.7	2.5	ns
t_{SK++} t_{SK--} t_{SKPP} t_{SKPW}	Data Path Skew++[3] Data Path Skew--[3] Part-to-Part Skew[3] Pulse Width Skew[3]			60 25 500 250			60 25 500 250			60 25 500 250	ps ps ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1 σ)			1			1			1	ps
V_{PP}	Input Voltage Swing (Differential)[4]	200	800	1000	200	800	1000	200	800	1000	mV
t_r / t_f	Output Rise/Fall Times (0.8 V – 2.0 V)	120			120			120			ps

1. LVTTL output R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to **Figure 2**.
2. f_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
3. Skews are measured between outputs under identical conditions.
4. 200 mV input guarantees full logic swing at the output.

Figure 2. TTL Output Loading Used for Device Evaluation