



VP503

CRT Display Video Output Amplifier:
High-Voltage, Wideband Amplification

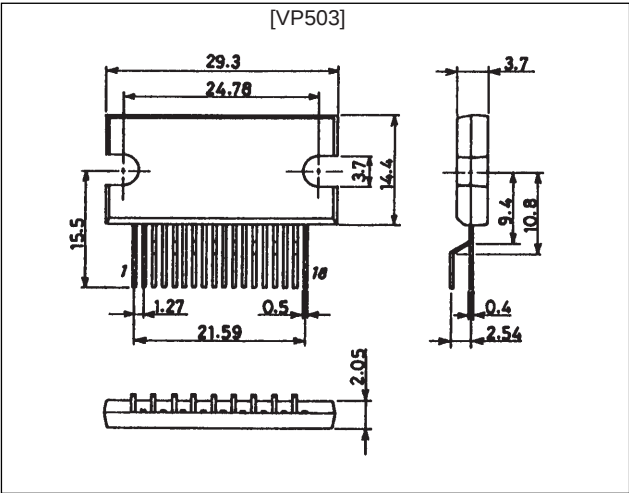
Function

- Three-channel video output circuit for CRT displays

Package Dimensions

unit: mm

2117



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		90	V
	V _{BB} max		15	V
Allowable power dissipation	Pd max		4.5	W
		At T _c = 25°C with an ideal heat sink	25	W
Case temperature	T _c max		100	°C
Storage temperature	T _{stg}		-20 to +110	°C

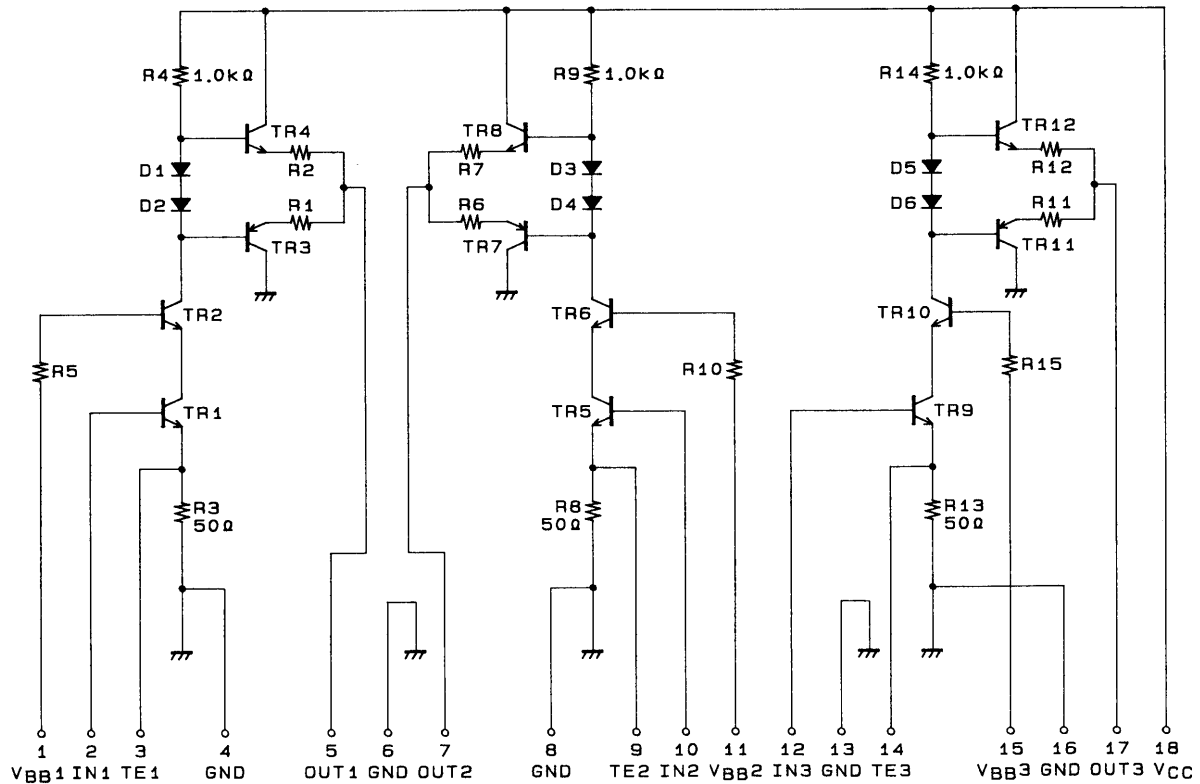
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage I	V _{CC}		70	V
	V _{BB}		10	V
Recommended supply voltage II	V _{CC}		80	V
	V _{BB}		10	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$

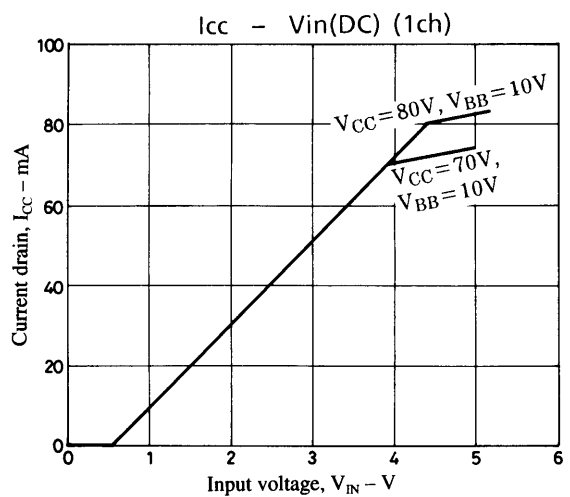
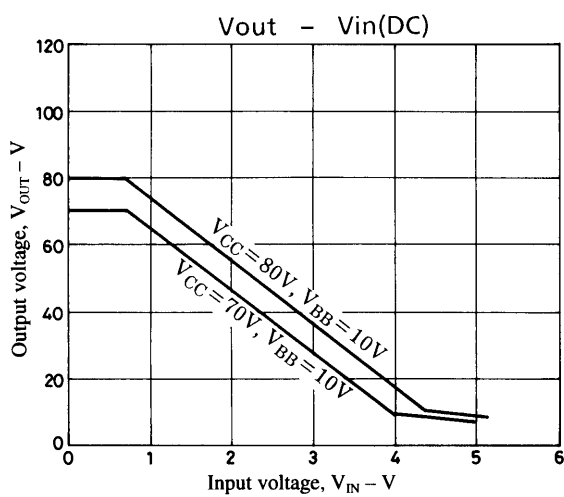
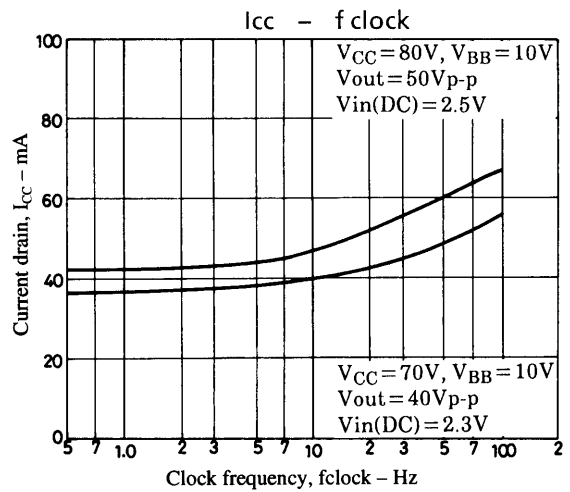
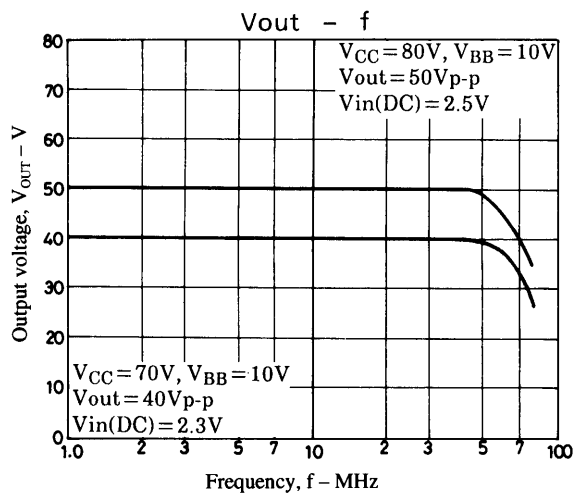
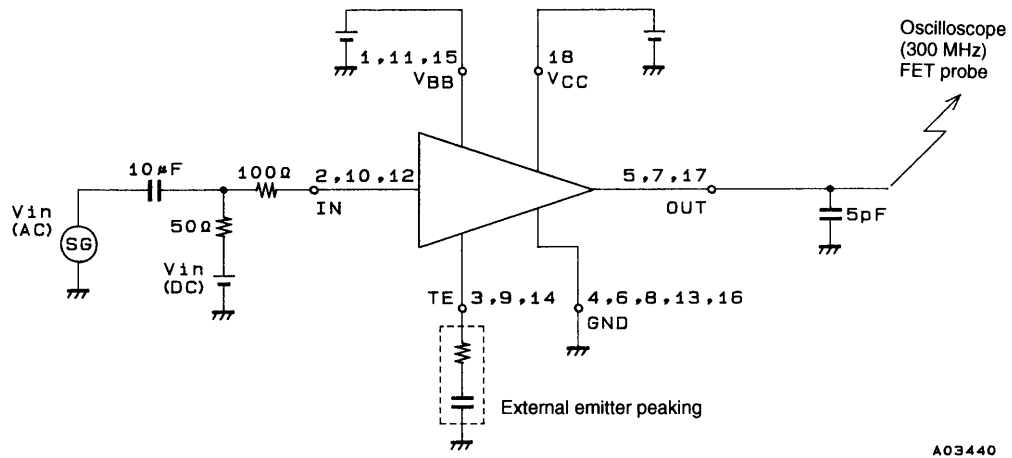
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Bandwidth I (–3 dB)	f_c	$V_{CC} = 70\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 5\text{ pF}$, $V_{IN}(\text{DC}) = 2.3\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		80		MHz
Bandwidth II (–3 dB)	f_c	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 5\text{ pF}$, $V_{IN}(\text{DC}) = 2.5\text{ V}$, $V_{OUT}(\text{p-p}) = 50\text{ V}$		75		MHz
Pulse response characteristics	t_r	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 5\text{ pF}$, $V_{IN}(\text{DC}) = 2.3\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		5.0		ns
	t_f	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 5\text{ pF}$, $V_{IN}(\text{DC}) = 2.3\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		5.0		ns
Voltage gain	$G_V(\text{DC})$		17	19	21	
Current drain I	I_{CC1}	$V_{CC} = 70\text{ V}$, $V_{BB} = 10\text{ V}$, $V_{IN}(\text{DC}) = 2.3\text{ V}$, $f = 10\text{ MHz}$ clock, $C_L = 5\text{ pF}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		40		mA
	I_{CC2}	$V_{CC} = 70\text{ V}$, $V_{BB} = 10\text{ V}$, $V_{IN}(\text{DC}) = 2.3\text{ V}$, $f = 70\text{ MHz}$ clock, $C_L = 5\text{ pF}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		50		mA
Current drain II	I_{CC1}	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $V_{IN}(\text{DC}) = 2.5\text{ V}$, $f = 10\text{ MHz}$ clock, $C_L = 5\text{ pF}$, $V_{OUT}(\text{p-p}) = 50\text{ V}$		45		mA
	I_{CC2}	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $V_{IN}(\text{DC}) = 2.5\text{ V}$, $f = 70\text{ MHz}$ clock, $C_L = 5\text{ pF}$, $V_{OUT}(\text{p-p}) = 50\text{ V}$		60		mA

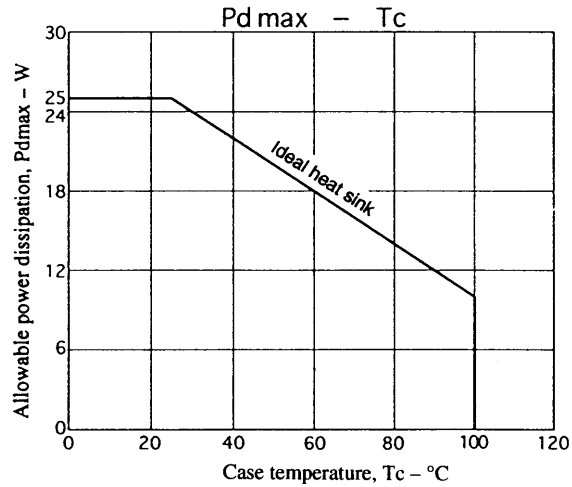
Internal Equivalent Circuit



A03434

Test Circuit





Product Features

The new VP503 series video packs provide the following features:

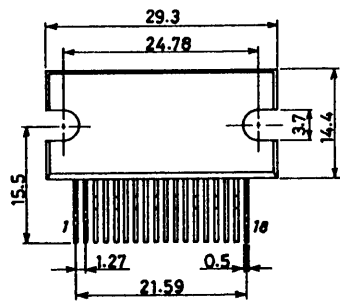
- 80 MHz operation and with three channels provided in a single package. The tr and tf times are 5 ns, as tested by Sanyo with $C_L = 10$ pF.

Cascode plus emitter follower circuit structure

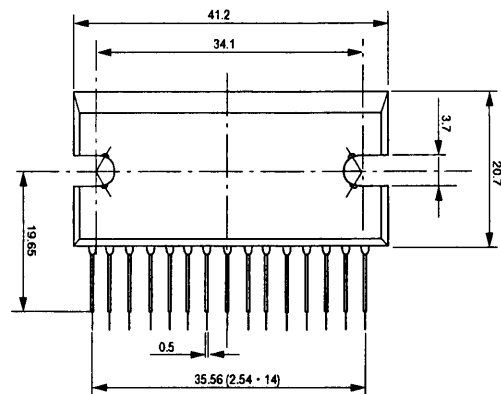
- Newly developed ultrahigh-frequency bipolar transistors adopted
- Ultraminiature package for a size reduction of 1/2 over the earlier Sanyo VPS series. This package supports standard zigzag forming.

Also, as shown in the figure below, 100 to 250-MHz product series are under development.

Package Dimensions



Newly developed VP Series



Earlier VP Series

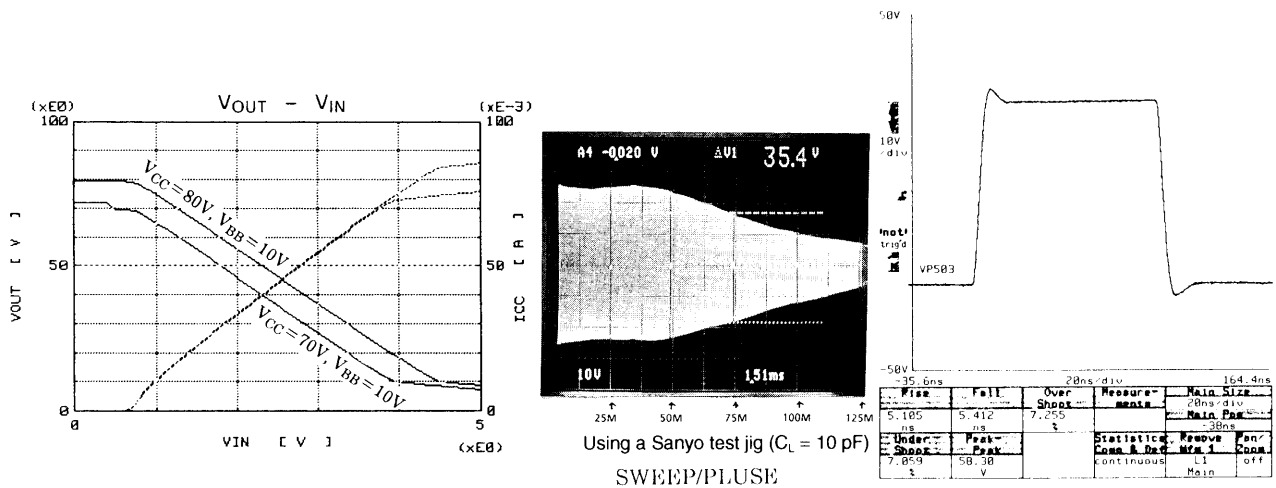
Operating Procedures

1. Setting the operating point

An optimal DC bias must be provided to operate a video pack and acquire the stipulated output dynamic range and bandwidth characteristics. Basically, the center point output voltage with no input should be set according to the following formula.

$$V_0 (\text{CENTER}) = (V_{CC} + V_{BB})/2$$

While the optimal operating point when an AC input is applied will be similar, the recommended electrical characteristics should be referred to when setting the operating point. The figures below show the DC and AC waveforms when the Sanyo test jig is used. The design of this product series was optimized so that these products provide adequate high-power characteristics.



2. Optimal peaking technique for mounted products (VP503 Series)

• Termination LC peaking

As can be seen from the internal equivalent circuit diagram, this series differs from earlier series in that peaking is not applied using an internal coil. Since the high-frequency region peaking point is determined by an LC resonator at the termination, the total distributed capacitance of the output side is particularly important. Accordingly, since the independent evaluation board timing characteristics will differ from the actual output load capacitance when an output cable is installed, the high-frequency area peaking point that corresponds to the output load state in the mounted circuit must be found.

(Adjust the circuit using an output matching RC circuit at the same time.)

• RC emitter peaking

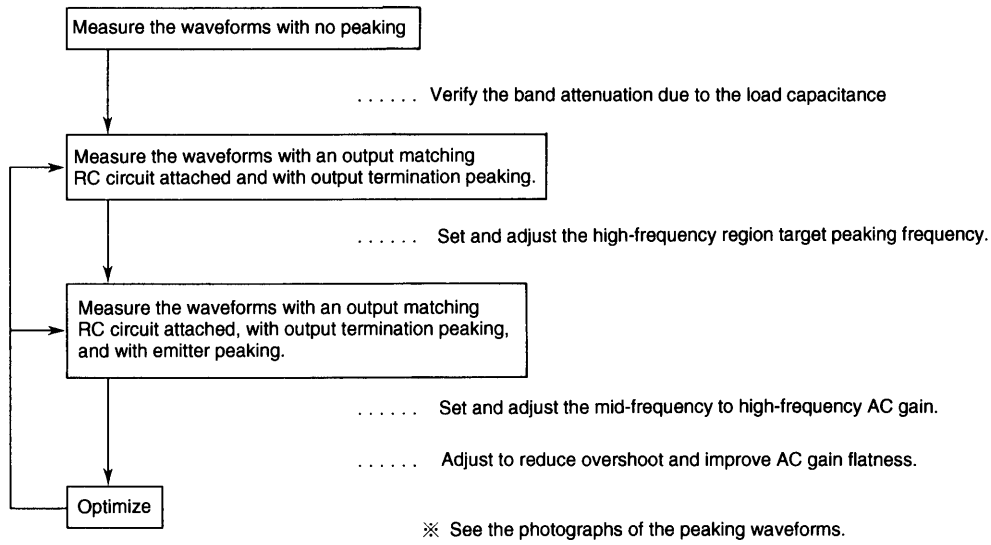
The purpose of the emitter peaking value is to increase the AC gain from the mid-frequency area to the high-frequency area. This should be determined last, after adjusting the termination peaking and output peaking RC circuits. (To compensate for high-frequency gain degradation at the IC side.)

• Output matching RC circuit

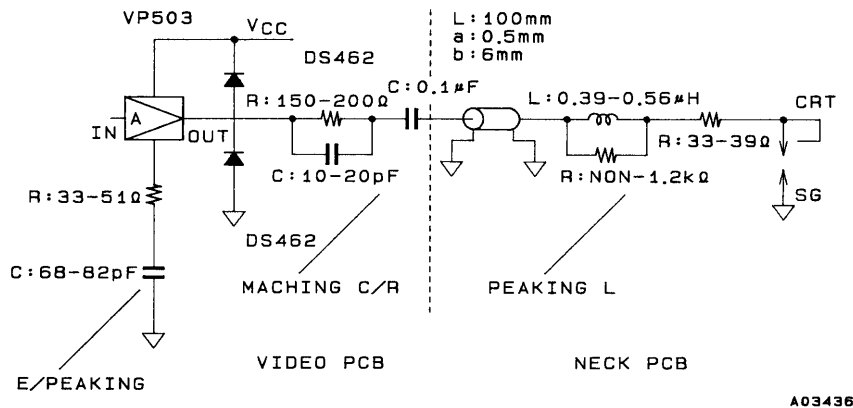
This circuit is used in conjunction with the peaking compensation in each section to match the IC internal impedance with the output load impedance. Mount this RC circuit in the vicinity of the protection diode and the IC output pins. Adjust this circuit to correct system characteristics while observing the mid-frequency characteristics, the amount of overshoot in the pulse response, and other aspects. Since the AC gain from the mid-frequency area to the high-frequency area will be reduced somewhat by this adjustment, determine the setting by adjusting the value of the resistor precisely.

The required circuit operating conditions can be set up smoothly if the following flowchart is used to adjust the peaking values.

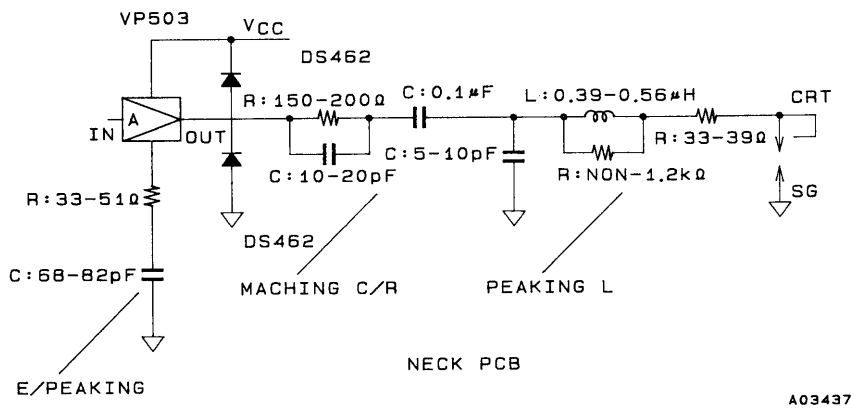
- Sample optimum peaking setup procedure flowchartWhen the total output load capacitance is between 15 and 20 pF (cable connection)



- Sample IC peripheral peaking compensation settings
When cable connection is used

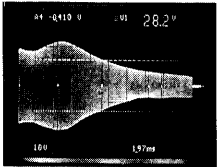
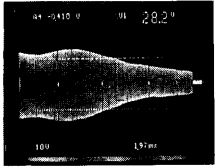
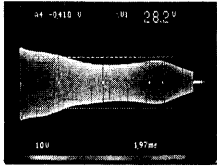
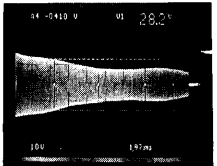
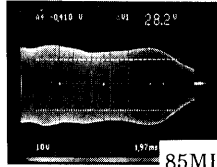
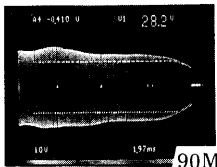
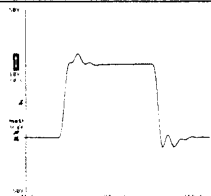
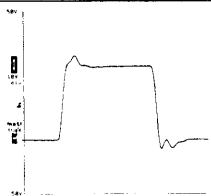


- When direct connection is used



Note: * Install a capacitor with the required value for the termination LC resonator.

Peaking Waveforms

Item	Cable waveforms	Direct waveforms
Peaking waveform		
Matching RC circuit + final peaking waveform		
Matching RC circuit + final peaking + emitter peaking waveform	 85MHz/-3dB	 90MHz/-3dB
	 $t_r : 6.36\text{ns}$ $t_f : 5.17\text{ns}$	 $t_r : 6.12\text{ns}$ $t_f : 5.37\text{ns}$

Thermal Design for the VP503

We recommended that the VP503 be used with the operating case temperature, T_c , under 100°C . Since the VP503 includes three channels, we first consider a single channel. The chip temperature of each transistor under actual operating conditions is determined using the following formula.

$$T_j = (T_{ri}) = \theta_{j-c} (T_{ri}) \times P_c (T_{ri}) + \Delta T_c + T_a [^{\circ}\text{C}] \dots\dots\dots (1)$$

$\theta_{j-c} (T_{ri})$: Thermal resistance of an individual transistor

$P_c (T_{ri})$: Collector loss for an individual transistor

ΔT_c : Case temperature rise

T_a : Ambient temperature

The $\theta_{j-c}(T_{ri})$ for each chip is:

$$\theta_{j-c} (T_{r2}) \text{ to } (T_{r4}) = 30^{\circ}\text{C/W} \dots\dots\dots (2)$$

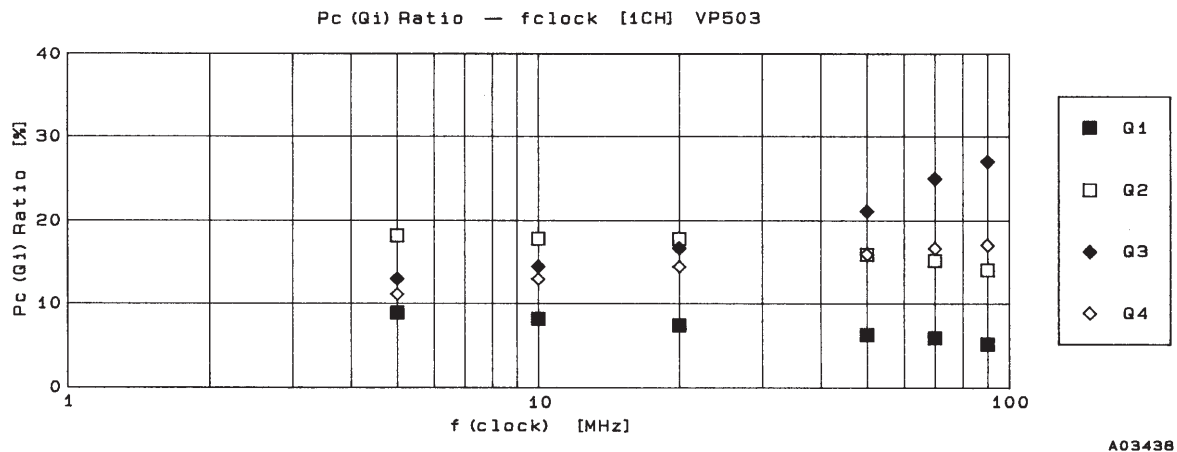
Although the loss for each transistor in a Video Pack varies with frequency and is not uniform, if we assume that the maximum operating frequency, $f = 85 \text{ MHz}$ (clock), then the chips with the largest loss will be transistor 3 and that loss will be about 1/4 of the total loss. Thus from the P_d for a single channel we have:

$$P_c (T_{r3}) f = 85 \text{ MHz} = P_d (1\text{CH}) f = 85 \text{ MHz} \times 0.25 [\text{W}] \dots\dots\dots (3)$$

Here, we must select a heat sink with a capacity θ_h such that the T_j of these transistors does not exceed 150°C . Equation (4) below gives the relationship between θ_h and ΔT_c .

$$\Delta T_c = P_d (\text{TOTAL}) \times \theta_h \dots\dots\dots (4)$$

The required θ_h is calculated using this equation and equation (1).



VP503 Thermal Design Example

Conditions: Using an $f_H = 64$ kHz class monitor, $f_v = 85$ MHz (clock)

$$V_{CC} = 80 \text{ V}, V_{BB} = 10 \text{ V}, V_{OUT} = 50 \text{ Vp-p} (C_L = 10 \text{ pF})$$

Since this class of monitor can be operated up to $T_a = 60^\circ\text{C}$, here we consider the case where the maximum clock frequency is 85 MHz.

As mentioned previously, the chip with the largest loss is transistor Tr3. Determining the value gives:

$$P_c (\text{Tr3}) = 5.0 \times 0.25 = 1.25 \text{ [W]} \dots\dots\dots (5)$$

We determine ΔT_j by substituting the value for θ_{j-c} in equation (5).

$$\Delta T_j = 1.25 \times 30 = 38 [^\circ\text{C}] \dots\dots\dots (6)$$

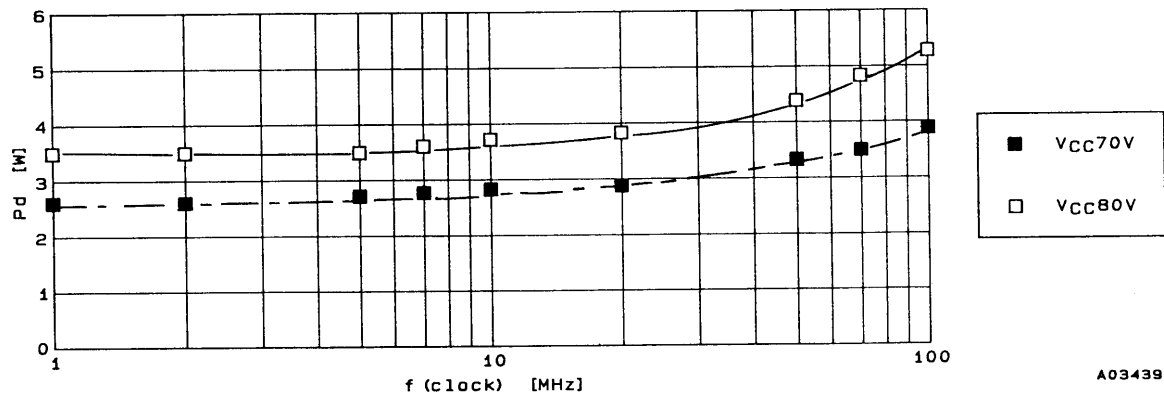
Here, ΔT_j is less than 50°C , and in the thermal design we only have to assure that T_c is less than 100°C . That is, we must set θ_h so that T_c is less than 100°C when $P_d (\text{TOTAL}) = P_d (\text{one channel}) \times 3$

Here, ΔT_c will be $\Delta T_c = 100 - 60 = 40^\circ\text{C}$

Since $\theta_h = \Delta T_c \div P_d (\text{TOTAL}) = 40 \div (5.0 \times 3) \approx 2.6^\circ\text{C/W}$

Thus the thermal resistance in this case is $\theta_h = 2.6^\circ\text{C/W}$.

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions into account is also required.



Surge Protection

Surge protection is required when this device is connected to a CRT. This product requires the same protection as earlier products.

1. Termination spark gap
2. Surge suppression resistor (Recommended value: 33 to 39 Ω)
3. Surge suppression diode (Installed in the vicinity of the IC output pin.)

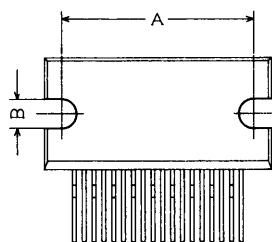
Note: The value of surge suppression resistors must be determined taking both the stipulated discharge test and the required frequency bandwidth into account. Note that the surge withstanding capacity of these products as independent video packs is equivalent to that of earlier products, e.g., the VPS Series.

Application Notes

Mounting notes:

Since the specified heat sink is required to operate a mounted Video Pack, we recommend the following mounting technique. (See the thermal design item for details on the required heat sink.) In particular, since the package used for this product is even more compact than that used in the earlier VPS series, the following points require special care. (These are recommendations.)

1. A tightening torque of between 0.39 and 0.88 N-m is recommended.
2. The bolt hole spacing in the heat sink should match that of the IC. In particular, the bolt hole spacing should be pulled in to be as close as possible, within the range that mounting is possible, to the dimensions A and B in the package dimensions drawing, as shown below.

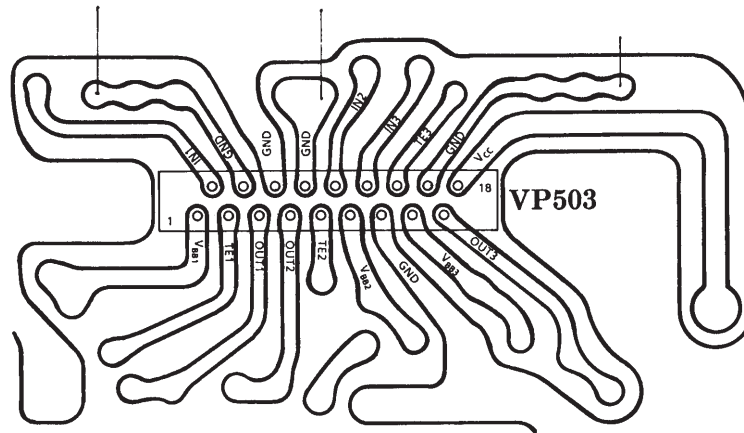


3. Use either the truss screws (truss bolts) or binding screws stipulated in the JIS standards as the mounting bolts. Also, use washers to protect the IC case.
4. Foreign matter, such as machining chips, must not be left trapped between the IC case and the heat sink. If grease is applied to the junction surface, be sure to apply the grease evenly.
5. Solder the IC leads to the printed circuit board after mounting the heat sink to the IC.

Note: The heat sink is absolutely required to operate this Video Pack. Never, in any situation, apply power to a Video Pack as an independent device. The Video Pack may be destroyed.

Peripheral wiring and ground leading:

When shipped, the VP503 product lead pins have standard support for forming (zigzag) so that the distance between pins will be 2.54 mm. Also, the pin layout is standardized to the I/O and power supply line arrangement shown below.



IC Surrounding Pin Layout (Top view)

Note: Design applications that use two-sided printed circuit boards or similar technologies so that input and output lines do not cross. Crossed lines can lead to increased crosstalk. Also, lines should be kept as short as possible, and lines in the ground pattern should be made as wide as possible. These layout design principles will minimize bandwidth degradation and oscillation.

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