Hitachi 16-Bit Microcomputer

HD64541

Link Layer Controller

User's Manual

HITACHI

ADE-602-036A

Rev. 2.0
5/26/00
Hitachi, Ltd.

Hitachi semiconductor

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Differences between the HD64541 and HD64541S

The HD64541 system includes an old HD64541 and new HD64541S.

Differences between the HD64541 and HD64541S are shown below.

Item	HD64541	HD64541S
Double frequency mode	None	Implemented
Operating frequency	Normal mode: 2.0 MHz to 6.0 MHz	Normal mode: 2.0 MHz to 6.25 MHz Double frequency mode: 4.0 MHz to 12.5 MHz
Package	68-pin plastic PLCC*[1] (CP-68)	80-pin plastic TQFP*[2] (TFP-80C)
Process	1.3 µm CMOS	0.8 µm CMOS

Notes: 1. PLCC: Plastic leaded chip carrier
2. TQFP: Thin quad flat package

Changes in the Revised Edition

The following tables list the main differences between this revision and the previous edition (ADE-602-036(0)). The changes are marked with stars (★) in the text.

Changes in the Specifications

Specifications	Modifications
Double frequency mode added	HD64541S has the double frequency mode which can operate with a double frequency system clock.
Operating frequency	The operating frequency of the HD64541S is 2.0 MHz to 6.25 MHz in normal mode 4.0 MHz to 12.5 MHz in double frequency mode
Reset command	Issuing condition and the operation of Reset command is changed.
AC electrical characteristics	(16A) t_{RHHI} is added.
TFP-80C package added	A TFP-80C package has been added to the product lineup.

Changes in the Text

Page	Title	Modifications
4	1.3 Pin Arrangement	Figure for TFP-80C package added
6	1.4 Pin Function	Pin numbers for TFP-80C package added Description of double frequency mode added CLKSEL pin added
11	2.1 Operational Outline	Description of double frequency mode added
32	2.5.1 System Parameter Table (SYSPT)	Description of double frequency mode added
101	5.3.2 AC Electrical characteristics	(16A) t_{RHHI} added
127	A.15 RSET (Reset)	Issuing condition and operation are changed
167	Appendix E Package Dimensions	TFP-80C package added

Contents

Section 1 Description

1.1 Description

The HD64541 one-chip CMOS communications device supports T.90, X.75, and X.25 protocols described by CCITT recommendation. Because of its asynchronous bus interface, it can be used with 16-bit external microprocessors.

The new HD64541S operates at a higher speed than the old HD64541. The HD64541S also has a very small package to achieve high density mounting.

HD64541 features:

- CCITT recommendation T.90, X.75, and X.25 support
  - — Processes T.90, X.75, and X.25 layer 2 protocols
  - — Reduces main processor load, improving system throughput
- Protocol processing operations
  - — HDLC framing, zero insertion/deletion, flag control, retransmission control, and state transition control
- Statistical counters
  - — Includes seventeen counters for statistical information: counters for specific frame types transmitted or received, transmission errors, etc.
  - — Reports counter status to host processor
- Selectable mode and parameters
  - — T.90, X.75, and X.25 modes
  - — System parameters programmable
- Chained transmit/receive function
  - — Long frames may be stored in multiple data buffers that are chained together and, except for UI, TEST, and XID frames, may be transmitted or received.
  - — Transmitted UI, TEST, and XID frame lengths are limited to a single buffer
- High throughput through unique architecture
  - — High performance protocol processing and data transmission
- Double frequency mode (HD64541S only)
  - — The HD64541S is able to operate with a 12.5 MHz system clock in the double frequency mode.
- TQFP*[1] package (HD64541S only)
  - — The HD64541S has a very small 80-pin TQFP package.

Note: TQFP: Thin quad flat package

Table 1-1 summarizes HD64541 functions.

Table 1-1 HD64541 Function Summary

Feature	Function
Communication protocol	CCITT T.90 layer 2/X.25 layer 2 (LAPB)/X.75 layer 2
Line rate (data rate)	Max 5 Mbps
Number of lines	One full duplex line
Operation Mode	T.90, X.75, X.25 mode
Selectable parameters	Maximum number of retransmissions: N2
	Maximum number of octets in an information field: N1
	Maximum time allowed without receiving acknowledgement to transmitted frames (0.1 to 25.5 seconds, 0.1 second steps): T1
	Maximum time allowed for idle state (0.1 to 25.5 seconds, 0.1 second steps): T3 or (1 to 255 seconds, 1 second steps)
	Maximum number of outstanding I frames (1 to 127): K
	Time for delayed acknowledgement: T2
Diagnostics	Auto-echo
	Local loopback
	Auto-echo and local loopback
Peripheral I/O ports	3 inputs, 2 outputs (general-purpose I/O, level detection)
Data encoding	NRZ serial data
Data transfer with memory	DMA
Address space	16 Mbyte
Data bus width	16 bits (multiplexed with address bus)
Power supply	Single +5 V
Power consumption	130 mW (typ.)
Process	CMOS 1.3 µm (HD64541)
	CMOS 0.8 µm (HD64541S)
Package	68-pin plastic PLCC*[1] (CP-68) (HD64541)
	80-pin plastic TQFP*[2] (TFP-80C) (HD64541S)
Ordering code	HD64541C01CP (CP-68)
	HD64541SC01TF (TFP-80C)

Notes: 1. PLCC: Plastic leaded chip carrier
2. TQFP: Thin quad flat package

1.2 Block Diagram

Figure 1-1 is the HD64541 block diagram.

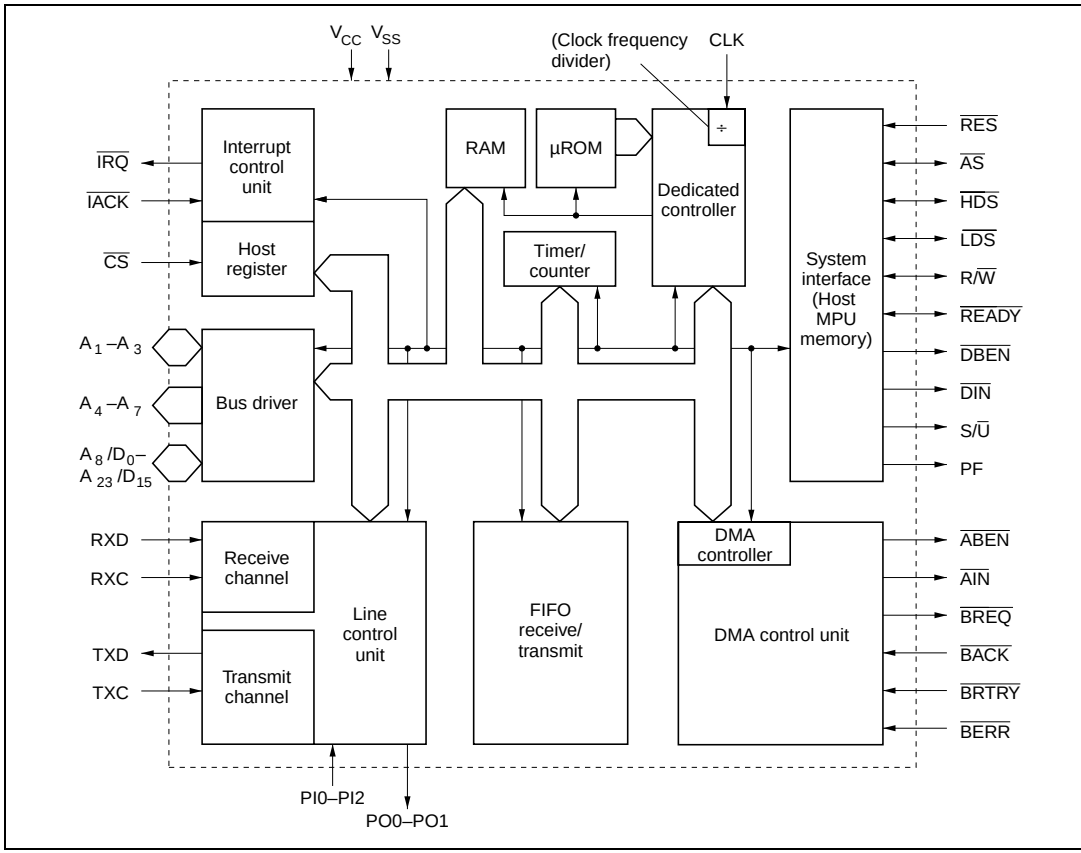


Figure 1-1 HD64541 Block Diagram

1.3 Pin Arrangement

Figure 1-2 (a) shows the HD64541 pin arrangement.

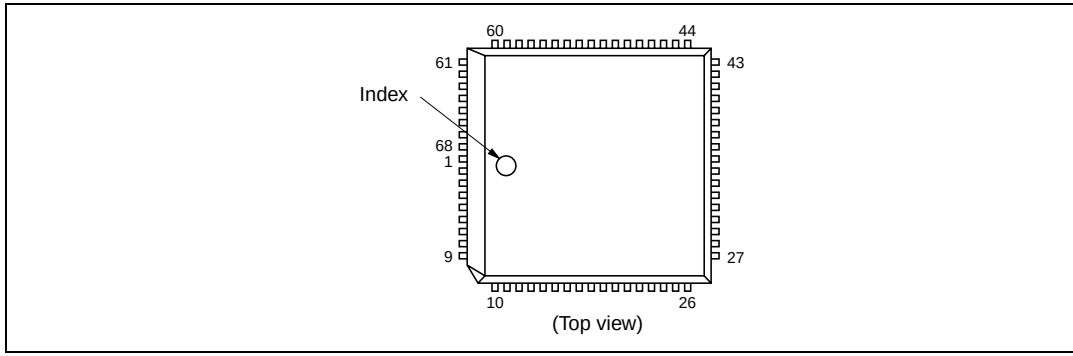


Figure 1-2 (a) HD64541 Pin Arrangement (CP-68)

PLCC Pin arrangement

Pin No.	Names	Pin No.	Names	Pin No.	Names	Pin No.	Names
1	V_{SS}	18	CLK	35	A18/D10	52	PI1
2	V_{CC}	19	A3	36	A19/D11	53	PI2
3	R/$\overline{W}$	20	A4	37	A20/D12	54	RXC
4	$\overline{HDS}$	21	A5	38	A21/D13	55	RXD
5	$\overline{LDS}$	22	A6	39	A22/D14	56	V_{SS}
6	$\overline{READY}$	23	A7	40	A23/D15	57	V_{CC}
7	$\overline{AIN}$	24	A8/D0	41	V_{SS}	58	TXD
8	$\overline{IRQ}$	25	A9/D1	42	V_{CC}	59	TXC
9	$\overline{IACK}$	26	A10/D2	43	V_{CC}	60	NUM
10	NC	27	A11/D3	44	$\overline{BRTRY}$	61	$\overline{BREQ}$
11	S/$\overline{U}$	28	A12/D4	45	$\overline{BERR}$	62	$\overline{BACK}$
12	PF	29	A13/D5	46	$\overline{RES}$	63	$\overline{CS}$
13	NUM	30	A14/D6	47	NUM	64	$\overline{AS}$
14	A1	31	A15/D7	48	NUM	65	$\overline{ABEN}$
15	A2	32	A16/D8	49	PO0	66	NC
16	V_{SS}	33	V_{SS}	50	PO1	67	$\overline{DIN}$
17	V_{CC}	34	A17/D9	51	PI0	68	$\overline{DBEN}$

NUM: Not users mode

NC: No connection

Figure 1-2 (b) shows the HD64541S pin arrangement.

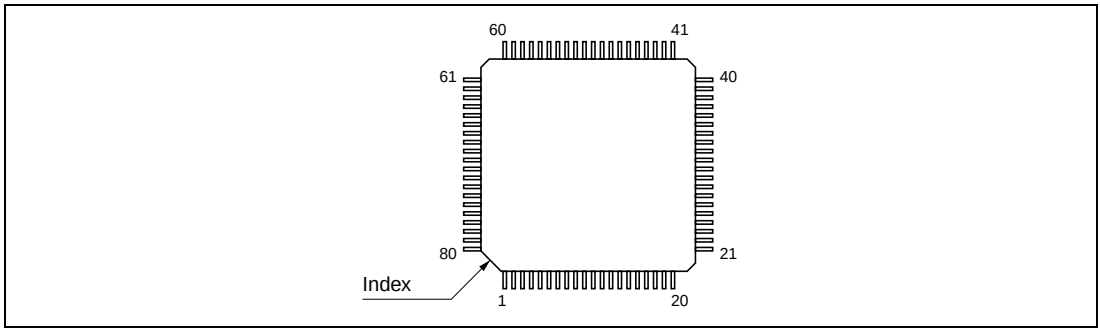


Figure 1-2 (b) HD64541S Pin Arrangement (TFP-80C)

Pin No.	Names	Pin No.	Names	Pin No.	Names	Pin No.	Names
1	NC	21	NC	41	NC	61	NC
2	NC	22	A11/D3	42	$\overline{\text{BRTRY}}$	62	$\overline{\text{BREQ}}$
3	S/$\overline{\text{U}}$	23	A12/D4	43	$\overline{\text{BERR}}$	63	$\overline{\text{BACK}}$
4	PF	24	A13/D5	44	$\overline{\text{RES}}$	64	$\overline{\text{CS}}$
5	CLKSEL	25	A14/D6	45	NUM	65	$\overline{\text{AS}}$
6	A1	26	A15/D7	46	NUM	66	$\overline{\text{ABEN}}$
7	A2	27	A16/D8	47	PO0	67	NC
8	V_{SS}	28	V_{SS}	48	PO1	68	$\overline{\text{DIN}}$
9	NC	29	A17/D9	49	PI0	69	$\overline{\text{DBEN}}$
10	V_{CC}	30	A18/D10	50	PI1	70	V_{SS}
11	CLK	31	A19/D11	51	PI2	71	NC
12	A3	32	A20/D12	52	RXC	72	V_{CC}
13	A4	33	A21/D13	53	RXD	73	R/$\overline{\text{W}}$
14	A5	34	A22/D14	54	V_{SS}	74	$\overline{\text{HDS}}$
15	A6	35	A23/D15	55	NC	75	$\overline{\text{LDS}}$
16	A7	36	V_{SS}	56	V_{CC}	76	$\overline{\text{READY}}$
17	A8/D0	37	NC	57	TXD	77	$\overline{\text{AIN}}$
18	A9/D1	38	V_{CC}	58	TXC	78	$\overline{\text{IRQ}}$
19	A10/D2	39	V_{CC}	59	NUM	79	$\overline{\text{IACK}}$
20	NC	40	NC	60	NC	80	NC

NUM: Not users mode

NC: No connection

1.4 Pin Function

Table 1-2 describes the pin functions.

Table 1-2 Pin Description

Group	Mnemonic	Pin No. CP-68	Pin No. TFP-80C	I/O	Function
Power supply	V_{CC}	2, 17, 42, 43, 57	10, 38, 39, 56, 72	I	+5 V power supply
	V_{SS}	1, 16, 33, 41, 56	8, 28, 36, 54, 70	I	0 V ground
Address/data bus	A_1 to A_3	14, 15, 19	6, 7, 12	I/O	Address bus
	A_4 to A_7	20, 21, 22, 23	13, 14, 15, 16	O	Address bus
	A_8/D_0 to A_{23}/D_{15}	24 to 32, 34 to 40	17 to 19 22 to 35	I/O	Address data bus
System control	$\overline{CS}$	63	64	I	Chip select
	$\overline{AS}$	64	65	I/O	Address strobe
	R/$\overline{W}$	3	73	I/O	Read/write
	$\overline{HDS}$	4	74	I/O	High data strobe
	$\overline{LDS}$	5	75	I/O	Low data strobe
	$\overline{READY}$	6	76	I/O	Ready
DMA control	$\overline{BREQ}$	61	62	O	Bus request
	$\overline{BACK}$	62	63	I	Bus acknowledge
Interrupt control	$\overline{IRQ}$	8	78	O	Interrupt request
	$\overline{IACK}$	9	79	I	Interrupt acknowledge
Bus control	$\overline{ABEN}$	65	66	O	Address bus enable
	$\overline{AIN}$	7	77	O	Address indication
	$\overline{DBEN}$	68	69	O	Data bus enable
	$\overline{DIN}$	67	68	O	Data indication
Bus driver control	$\overline{BRTRY}$	44	42	I	Bus cycle retry
	$\overline{RES}$	46	44	I	Reset
	$\overline{BERR}$	45	43	I	Bus error
Area control	S/$\overline{U}$	11	3	O	Supervisor/user
	PF	12	4	O	Program fetch

Table 1-2 Pin Description (cont)

Group	Mnemonic	Pin No. CP-68	Pin No. TFP-80C	I/O	Function
Serial interface	RXD	55	53	I	Receive data
	RXC	54	52	I	Receive clock
	TXD	58	57	O	Transmit data
	TXC	59	58	I	Transmit clock
General-purpose	PI0 to PI2	51, 52, 53	49, 50, 51	I	Port input
	PO0 to PO1	49, 50	47, 48	O	Port output
Clock	CLK	18	11	I	Clock
Clock select	CLKSEL	—	5	I	Select the clock mode
Others	NUM	13, 47, 48, 60	45, 46, 59	I	Not user mode
	NC	10, 66	1, 2, 9, 20, 21, 37, 40, 41, 55, 60, 61, 67, 71, 80	O	No connection

1.4.1 Power Supply

V_{CC}: Connect V_{CC} to the +5 V power supply.

V_{SS}: Connect V_{SS} to ground (0 V).

1.4.2 Address/Data Bus

A_1 to A_3 (Address Bus): When the HD64541 controls the bus, it is said to be in master mode and drives active address pins A_1 to A_3 as outputs. When the HD64541 is in slave mode, A_1 to A_3 become inputs and, together with the $\overline{HDS}$ and $\overline{LDS}$ input pins, address the HD64541's internal registers.

A_4 to A_7 (Address Bus): In master mode, the HD64541 drives active address pins A_4 to A_7 as outputs.

A_8/D_0 to A_{23}/D_{15} (Address/Data Bus): The A_8/D_0 to A_{23}/D_{15} pins are time-multiplexed between address and data. Output pins $\overline{ABEN}$, $\overline{AIN}$, $\overline{DIN}$, and $\overline{DBEN}$ are used to externally demultiplex data and addresses.

In master mode, the HD64541 drives active these pins as outputs to carry both addresses and data. In slave mode, these pins may be either inputs or outputs, but for data only.

1.4.3 System Control

$\overline{CS}$ (Chip Select): When the HD64541 does not control the bus, $\overline{CS}$ is the chip select input.

$\overline{AS}$ (Address Strobe): When the HD64541 controls the bus and is outputting address bits A_1 to A_7 and A_8/D_0 to A_{23}/D_{15}, the $\overline{AS}$ output is active low.

When the HD64541 does not control the bus, this line is an input indicating valid address input.

R/$\overline{W}$ (Read/Write): When the HD64541 is reading the bus, R/$\overline{W}$ is high. When it is writing to the bus, R/$\overline{W}$ is low. This controls the direction of data flow.

$\overline{HDS}$ (High Data Strobe): $\overline{HDS}$ indicates the presence of data on the high-order eight bits of the data bus (D_{15} to D_8). In master mode, the HD64541 drives active this signal as an output. In slave mode, the HD64541 reads this bit as an input.

$\overline{LDS}$ (Low Data Strobe): $\overline{LDS}$ indicates the presence of data on the low-order eight bits of the data bus (D_7 to D_0). In master mode, the HD64541 drives active this signal as an output. In slave mode, the HD64541 reads this bit as an input.

$\overline{READY}$ (Ready): When the HD64541 controls the bus, $\overline{READY}$ is an input signalling the completion of a data transfer. When the HD64541 releases the bus, $\overline{READY}$ becomes an output indicating the completion of data read/write.

1.4.4 DMA Control

$\overline{BREQ}$ (Bus Request): The HD64541 uses $\overline{BREQ}$ to request the bus.

$\overline{BACK}$ (Bus Acknowledge): The $\overline{BAC}$ input responds to $\overline{BREQ}$, indicating that the bus is available.

1.4.5 Interrupt Control

$\overline{IRQ}$ (Interrupt Request): The $\overline{IRQ}$ output requests an MPU interrupt. It is an open-drain output.

$\overline{IACK}$ (Interrupt Acknowledge): The $\overline{IACK}$ input responds to $\overline{IRQ}$, indicating that the interrupt request has been accepted. The HD64541 then supplies the interrupt vector, whose value was established by VADD (byte 2 of SYSPT) at initialization.

1.4.6 Bus Driver Control

$\overline{\text{ABEN}}$ (Address Bus Enable): The $\overline{\text{ABEN}}$ output latches the address on the address/data lines when the HD64541 controls the bus.

$\overline{\text{AIN}}$ (Address Indication): The $\overline{\text{AIN}}$ output is asserted while the HD64541 controls the bus. It controls the output of the address line latch.

$\overline{\text{DBEN}}$ (Data Bus Enable): The $\overline{\text{DBEN}}$ output controls the direction of the bidirectional address data buffer.

$\overline{\text{DIN}}$ (Data Indication): The $\overline{\text{DIN}}$ output controls the direction of the data lines.

1.4.7 Bus Exception Conditions

$\overline{\text{BRTRY}}$ (Bus Retry): The $\overline{\text{BRTRY}}$ input requests a bus cycle retry. The retry exception causes the HD64541 to hold the current operation and retry the operation until the retry is removed.

$\overline{\text{RES}}$ (Reset): The HD64541 is initialized when $\overline{\text{RES}}$ goes low. It must be held low for at least 24 clock cycles.

$\overline{\text{BERR}}$ (Bus Error): When the HD64541 recognizes a bus error input on $\overline{\text{BERR}}$, the bus cycle ends and the bus is released. This takes at least 8 clock cycles.

1.4.8 Area Control

S/$\overline{\text{U}}$ (Supervisor/User): The S/$\overline{\text{U}}$ output indicates user-space or supervisor-space access.

PF (Program Fetch): The PF output indicates program-space or data-space access.

1.4.9 Serial Interface

RXD (Receive Data): Input pin RXD connects to the received data channel. Data bits on RXD are synchronized to the rising edges of the clock pulses on RXC.

RXC (Receive Clock): Input pin RXC connects to the synchronous receive data clock.

TXD (Transmit Data): Output pin TXD connects to the transmit data channel. Data bits on TXD are synchronized to the falling edges of the clock pulses on TXC.

TXC (Transmit Clock): Output pin TXC sources a synchronous transmit data clock.

1.4.10 General-Purpose I/O

PI0 to PI2 (Port Input): PI0 to PI2 are general-purpose input ports whose levels are reported to the external microprocessor by means of PITL status. These ports are independent of the HD64541's protocol operations.

PO0 to PO1 (Port Output): PO0 to PO1 are general-purpose output ports whose levels are controlled by the external microprocessor by means of the CPOL command. These ports are independent of the HD64541's protocol operations.

1.4.11 Clock

CLK (Clock): Input pin CLK connects to the system clock. The frequency of the system clock should be the same frequency for the normal mode, and double the frequency for the double frequency mode, versus the frequency which is specified with TDIV on the system parameter table (SYSTP). (refer 2.5.1)

CLKSEL (Clock Select): The CLKSEL input selects the system clock frequency mode. High level input selects the double frequency mode and the CLK input is divided by 2 to use in the chip. Low level input selects the normal mode and the CLK input is directly used in the chip.

1.4.12 Others

NUM (Not User Mode): The NUM pins must be connected to logic low.

NC (No Connection): Leave NC pins unconnected.

1.5 System Configuration

Figure 1-3 is an example of a system configuration using the HD64541. The HD64541 processes the signal received from the line according to protocol procedure. The processed result is sent to the host MPU. Transmit data is transferred to the line according to commands from the host MPU.

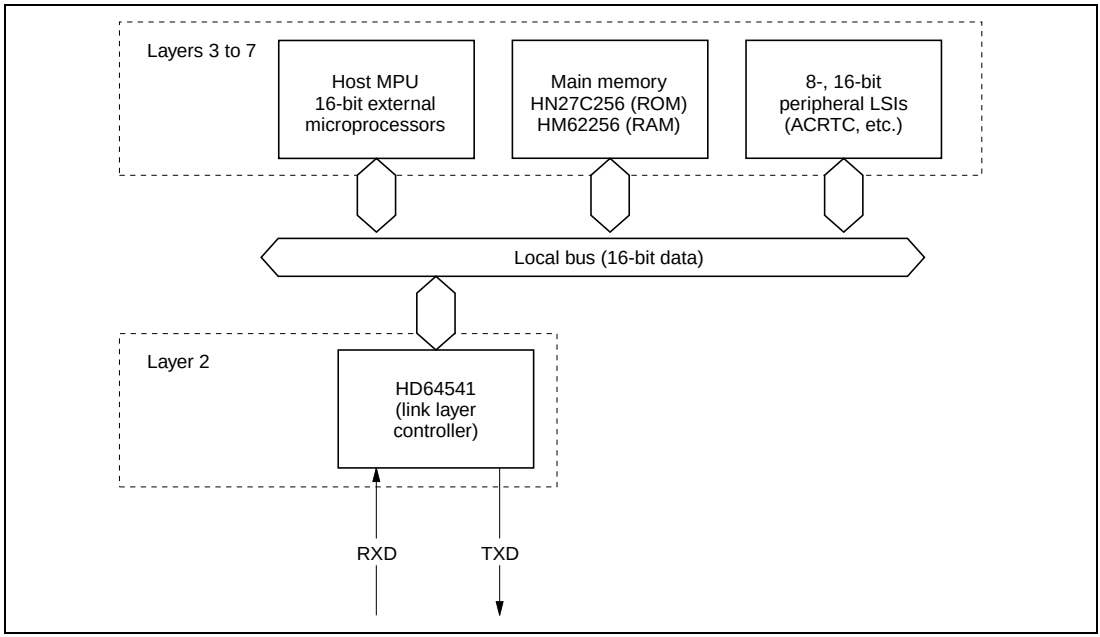


Figure 1-3 System Configuration Block Diagram

Section 2 Functional Description

2.1 Operational Outline

The HD64541 requires an external microprocessor and memory to operate (figure 2-1).

The external microprocessor controls HD64541 operations by writing command codes into the command register (CR). The HD64541 returns the results of command execution or protocol processing through codes made available to the microprocessor through the status register (SR). A command status register (CMSR), interrupt source register (ISR), and interrupt mask register (IMR) complete the microprocessor interface register set. For details, see section 2.2, Registers. For command types and formats, see section 2.3, Commands, and appendix A. For status types and formats, see section 2.4, Status, and appendix B.

External memory holds a total of nine control tables (see section 2.5, Tables Implemented in External Memory, for details), including the transmit data buffer (SDB), receive data buffer (RDB), sending I-frame information table (SIIT), receive buffer information table (RBIT), and system parameter table (SYSPT). The HD64541 reads from and writes into the tables on command from the external microprocessor.

Double frequency mode (only for HD64541S)

The HD64541S can use the internal clock, which is the system clock divided by 2 in the chip.

As a result, the HD64541S can operate at 12.5 MHz maximum.

The double frequency mode is set by inputting a high level into the CLKSEL pin.

However note that the minimum period of each bus cycle is the same in double frequency mode and normal mode, since the maximum internal operating frequency is the same for both modes.

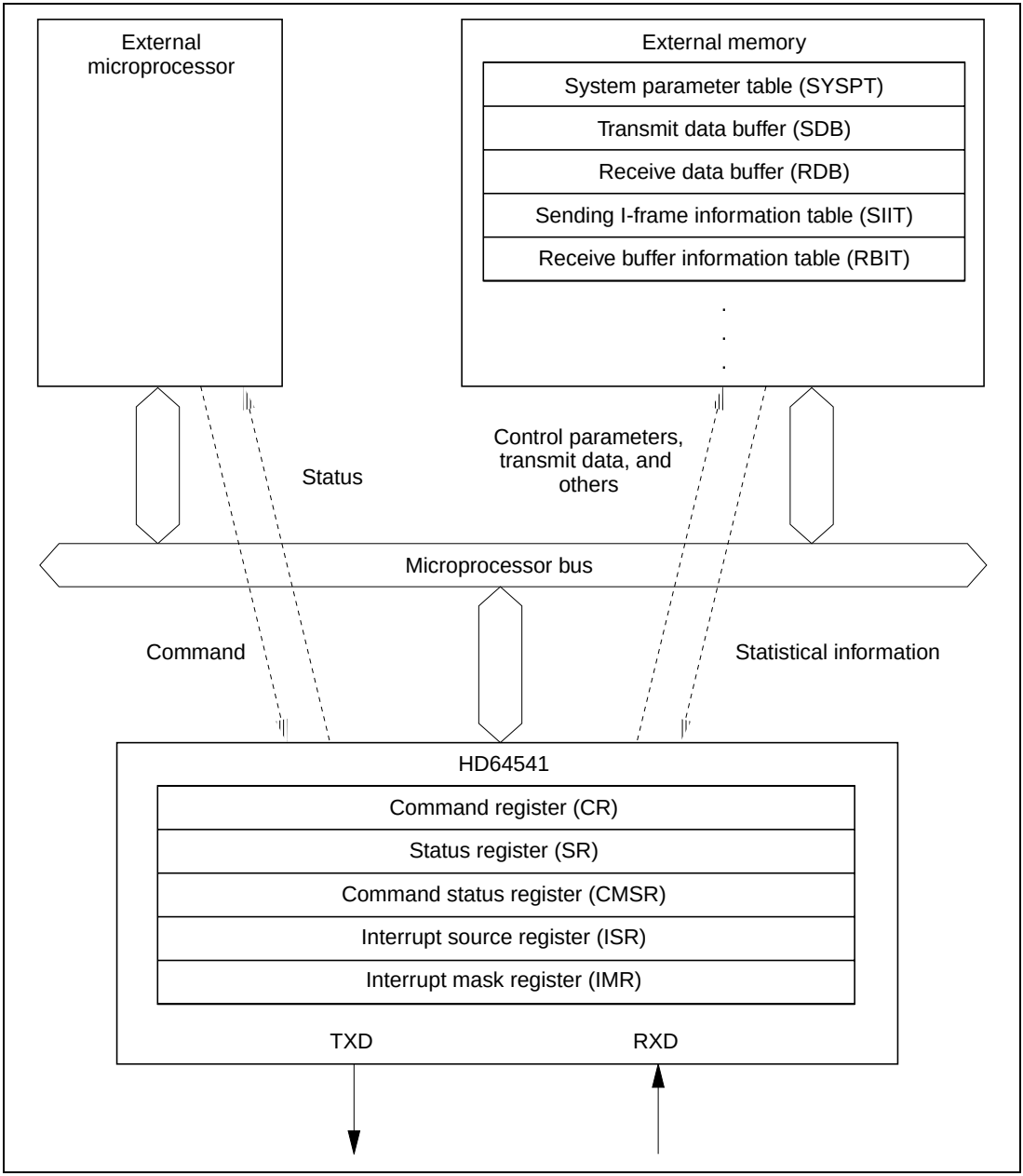


Figure 2-1 HD64541 External Device Interfaces

2.2 Registers

The HD64541 has five registers that can be directly accessed by the external microprocessor through the system bus.

1. Command register (CR)
2. Command status register (CMSR)
3. Status register (SR)
4. Interrupt source register (ISR)
5. Interrupt mask register (IMR)

Table 2-1 shows the address assignment of each register.

Table 2-1 Register Address Map

Address							Configuration								
A_3	A_2	A_1	$\overline{HDS}$	$\overline{LDS}$	Register	R/$\overline{W}$	Reset	7	6	5	4	3	2	1	0
0	0	0	0	1	Command register (CR)	W	—	—	—	Command code					
0	0	0	1	0			—			Parameter 1					
0	0	1	0	1			—			Parameter 2					
0	0	1	1	0			—			Parameter 3					
0	0	0	0	1	Status register (SR)	R	$00			Status code					
0	0	0	1	0			$00			Parameter 1					
0	0	1	0	1			$00			Parameter 2					
0	0	1	1	0			$00			Parameter 3					
0	1	0	0	1	—	—	—			—					
0	1	0	1	0	Interrupt source reg. (ISR)	R/W	$00	0	0	Interrupt source					
0	1	1	0	1	—	—	—			—					
0	1	1	1	0	Interrupt mask reg. (IMR)	R/W	$3F	0	0	Interrupt mask					
1	0	0	0	1	—	—	—			—					
1	0	0	1	0	Command status reg. (CMSR)	R	$00	0	0	0	0	0	Code		

Note: CR and SR have the same address. CR is accessed by write cycles, and SR is accessed by read cycles.

2.2.1 Command Register

The external microprocessor controls the HD64541 by writing command codes into its command register (figure 2-2). The command register is four octets wide and may be addressed either as four contiguous single-octet registers (CR-HH, CR-HL, CR-LH, and CR-LL) or as two contiguous two-octet registers (CR-H and CR-L). The command register is write-only and shares addresses with the read-only status register.

The low order half (CR-L) or quarter (CR-LL) of the command register must be written last since the HD64541 takes that as an indication that the full CR write has been completed.

The 7 and 6 bit of CR-HH are don't care bits.

When the HD64541 is busy executing a command started earlier, the low-order bit (CMSR0) of the command status register (CMSR) is set to 1 and any attempt to write into the command register (CR) is ignored.

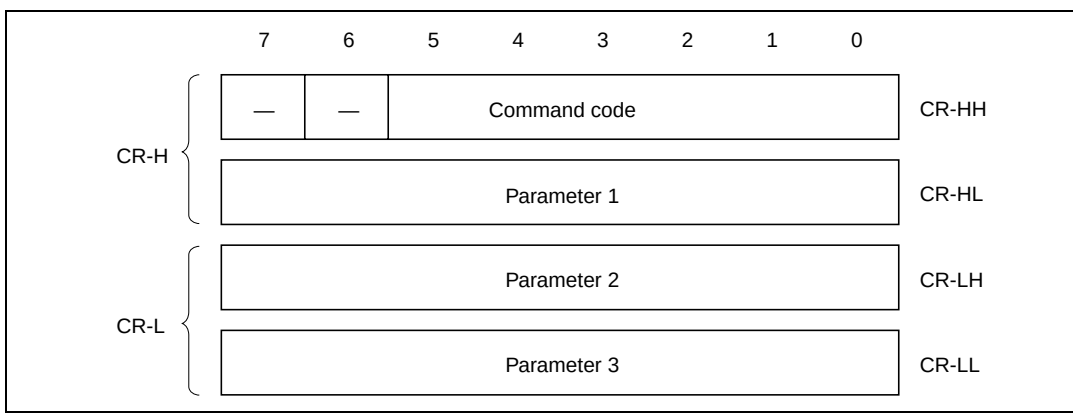


Figure 2-2 Command Register

2.2.2 Command Status Register (CMSR)

The command status register (figure 2-3) controls writing to the CR and indicates the results of command execution.

CMSR0 set to 1 indicates that a command is being executed, and the MPU cannot write another command. The MPU should check the state of CMSR0 before writing to the CR.

CMSR1 and CMSR2 are valid when CMSR0 is cleared to 0. They indicate the result of the execution of the previous command.

Whenever CMSR0 makes a transition from 1 to 0 (that is, busy to not busy), the low-order bit of the ISR (ISR0) is set to 1 and generates an interrupt unless masked by the IMR.

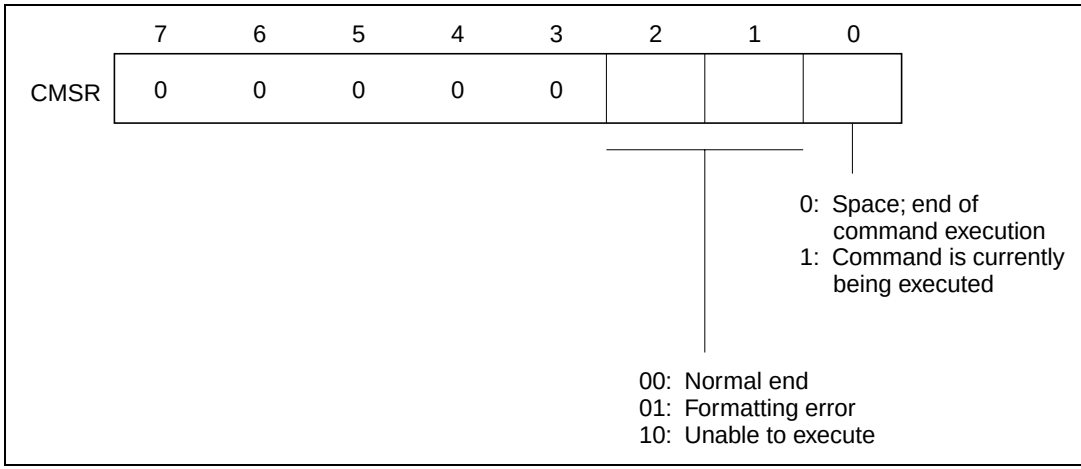


Figure 2-3 Command Status Register

2.2.3 Status Register (SR)

The HD64541 returns the results of command or protocol processing to the external microprocessor by setting status codes in its status register (figure 2-4). The status register is four octets wide and may be addressed either as four contiguous single-octet registers (SR-HH, SR-HL, SR-LH, and SR-LL) or as two contiguous two-octet registers (SR-H and SR-L). The status register is read-only and shares addresses with the write-only command register.

The low-order half (SR-L) or quarter (SR-LL) of the status register must be read last since the HD64541 takes that as an indication that the full SR read has been completed.

Status code = $00 shows that the SR does not contain an active status.

Whenever the status is set in SR, ISR1 is set to 1. This causes an interrupt if it is not masked by the IMR.

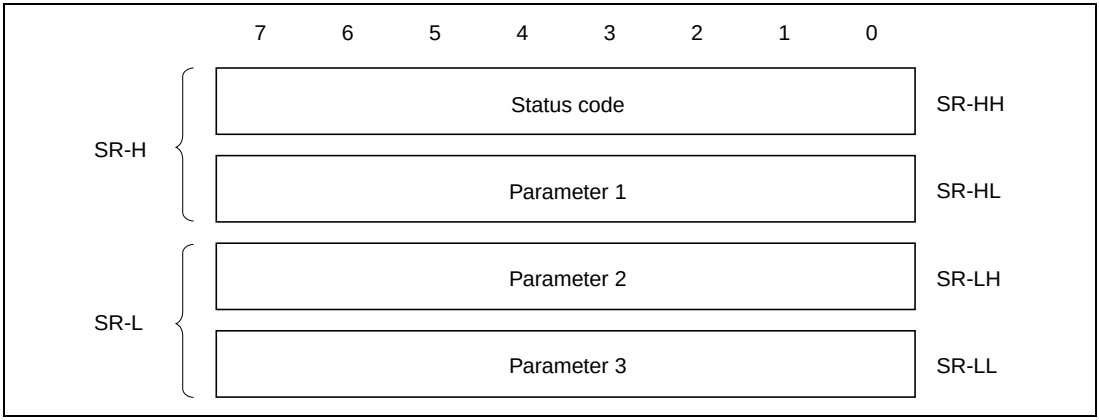


Figure 2-4 Status Register

2.2.4 Interrupt Source Register (ISR)

The interrupt source register (figure 2-5) indicates interrupt causes. All bits except ISR4 can be read and written. Table 2-2 shows the function of the ISR bits.

To reset any ISR bit, write 1 to that bit.

Note that ISR4 cannot be reset by writing to it. It remains high during internal processing.

Even though the ISR is masked by the interrupt mask register (IMR), the ISR operates normally.

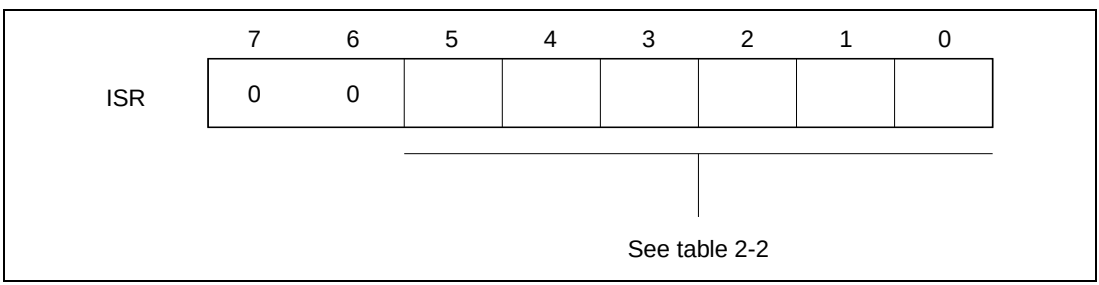


Figure 2-5 Interrupt Source Register

Table 2-2 ISR Function

Bit	Name	Description
ISR0	End of command execution	Command was executed; result was written into CMSR; HD64541 ready to accept next command
ISR1	End of status write	Status written into SR; request that MPU read SR
ISR2	Internal queue overflow	Internal queue overflow; stop all operations and enter reset command waiting state
ISR3	Receive buffer overflow	I-, UI, XID ,or TEST frame was lost because the receive buffer was not ready
ISR4	Internal busy	Entered own receiver busy state (see note)
ISR5	DMA bus error	Bus error during DMA access; HD64541 enters reset command waiting state

Note: The HD64541 enters the internal busy state when it cannot locate the RDB. The external microprocessor remedies this condition by establishing an RDB and setting its address and size into the RBIT. The HD64541 also enters internal busy when an excessive number of status conditions are pending. The external microprocessor must read the SR to clear this condition. Command execution stops temporarily during internal busy. Internal busy state is maintained even after link is reestablished.

2.2.5 Interrupt Mask Register (IMR)

The interrupt mask register (figure 2-6) masks interrupt requests. It has the same structure as the ISR. Bits 5 to 0 correspond to ISR bits 5 to 0. The IMR can be read and written to. To mask an interrupt request, set the corresponding bit to 1.

The reset command (RSET) sets IMR to $3F (all requests masked).

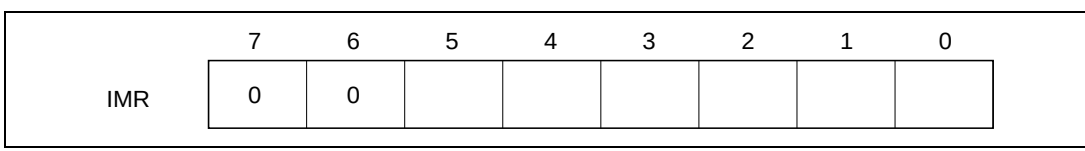


Figure 2-6 Interrupt Mask Register

2.3 Commands

The external microprocessor controls the HD64541 with the command codes listed in table 2-3. Figure 2-7 shows the command bit encodings.

Commands are classified into two types:

- Type B: Commands to activate I-, UI, XID, and TEST frame transmission.
- Type A: All other commands.

Figure 2-8 is a command processing flowchart.

Before issuing a command, the external microprocessor must verify that CMSR0 = 0, indicating that the previous command has terminated. If a write to the CR is attempted when CMSR0 = 1, the contents of CR will remain unchanged and the next command will not be accepted.

A command format error is posted on three conditions:

1. The command code is undefined.
2. The command is not allowed in the current protocol mode.
3. The command parameters are illegal.

The HD64541 sets the CMSR to 00000010 and generates a maskable interrupt request.

A correctly formatted command may not be valid under all conditions. Appendix A, which contains a description of every command recognized by the HD64541, specifies the conditions under which each command may be executed and the conditions under which the HD64541 rejects the command with a cannot execute error (CMSR = 00000100) maskable interrupt.

After a type A command is executed, the HD64541 sets the CMSR to 00000000.

When a type B command is executed to effect I-, UI, XID, or TEST frame transmission, the CMSR may indicate successful completion (CMSR = 00000000) even though the frame is merely queued and actual transmission occurs later, when HD64541 status and the state of the protocol permit.

Set Area Code (STAC)

Command code	Parameter 1	Parameter 2	Parameter 3
$00	AC0	AC1	AC2

Reset (RSET)

Command code	Parameter 1	Parameter 2	Parameter 3
$01	A23	System parameter table starting address	A0

Set Operation Mode (OMDS)

Command code	Parameter 1								Parameter 2	Parameter 3
$02	0	0	0	0	0	M2	M1	M0		

Control Peripheral Output Pin Level (CPOL)

Command code	Parameter 1	Parameter 2														Parameter 3	
$10		0	0	0	0	0	0	EN1	EN0	0	0	0	0	0	0	PO1	PO0

Mask Peripheral Input Information (MPIS)

Command code	Parameter 1	Parameter 2								Parameter 3
$11		0	0	0	0	0	PI2	PI1	PI0	

Dump System Parameter Table (DSPT)

Command code	Parameter 1	Parameter 2	Parameter 3
$12	A23	Dump address	A0

Dump Statistical Information (DERC)

Command code	Parameter 1	Parameter 2	Parameter 3
$13	A23	Dump address	A0

I-Frame Transmission 1 (DDR1)

Command code	Parameter 1	Parameter 2		Parameter 3
$20			P	FN

I-Frame Transmission 2 (DDR2)

Command code	Parameter 1	Parameter 2		Parameter 3
$21			P	FN

Figure 2-7 Commands

U and X Frame Transmission (MUDR)

Command code	Parameter 1	Parameter 2	Parameter 3
$22			

Suspend Frame Transmission (SUTD)

Command code	Parameter 1	Parameter 2	Parameter 3
$23			

Resume Frame Transmission (RETD)

Command code	Parameter 1	Parameter 2	Parameter 3
$24			

Establish Link (DESR)

Command code	Parameter 1	Parameter 2	Parameter 3
$25			

Release Link (DRLR)

Command code	Parameter 1	Parameter 2	Parameter 3
$26			

Set Local Station to Busy State (SSBY)

Command code	Parameter 1	Parameter 2	Parameter 3
$27			

Release Local Station from Busy State (RSBY)

Command code	Parameter 1	Parameter 2	Parameter 3
$28			

Remote Station Link Establish Wait (DESW)

Command code	Parameter 1	Parameter 2	Parameter 3
$29			

Reestablish Link (RESR)

Command code	Parameter 1	Parameter 2	Parameter 3
$2A			

Figure 2-7 Commands (cont)

Table 2-3 Commands

Command	Symbol	Code	Parameters	Description	Operation Mode: Protcol	Operation Mode: Trans-parent
Set area code	STAC	$00	AC0, AC1, AC2	Specifies area code (AC) for HD64541 memory access	✓	✓
Reset	RSET	$00	SYSPT starting address	Clears internal state, then reads and latches SYSPT saved in external memory	✓	✓
Set operation mode	OMDS	$02	M2-M0	Specifies operating conditions (loopback test, off-line operation, etc.)	✓	✓
Control peripheral output pin level	CPOL	$10	EN1, EN0, PO1, PO0	Sets level of peripheral output pins	✓	✓
Mask peripheral input information	MPIS	$11	PI2-PI0	Masks HD64541 status depending on level of peripheral input pins	✓	✓
Dump system parameter table	DSPT	$12	Dump address	Dumps system parameter table to memory area	✓	✓
Dump statistical information	DERC	$13	Dump address	Dumps monitor information to external memory	✓	✓
I-frame transmission 1	DDR1	$14	P, FN	Transmits I-frame data; after link is set, DDR2 is used	✓	✓
I-frame transmission 2	DDR2	$21	P, FN	Transmits first I-frame after DESI status	✓	✓
U and X frame transmission	MUDR	$22	—	Transmits UI , XID and TEST frames	✓	—
Suspend frame transmission	SUTD	$23	—	Temporarily suspends I-, UI, XID, and TEST frame transmission	✓	✓
Resume frame transmission	RETD	$24	—	Resumes I-, UI, XID and TEST frame transmission	✓	✓
Establish link	DESR	$25	—	Establishes link	✓	—

Table 2-3 Commands (cont)

Command	Symbol	Code	Parameters	Description	Operation Mode	
					Protcol	Trans-parent
Release link	DRLR	$26	—	Releases link	✓	—
Set local station to busy state	SSBY	$27	—	Sets local station into busy state	✓	—
Release local station from busy state	RSBY	$28	—	Releases local station from busy state	✓	—
Remote station link establish wait	DESW	$29	—	Waits for link establishment from remote station	✓	—
Reestablish link	RESR	$2A	—	Reestablishes link	✓	—

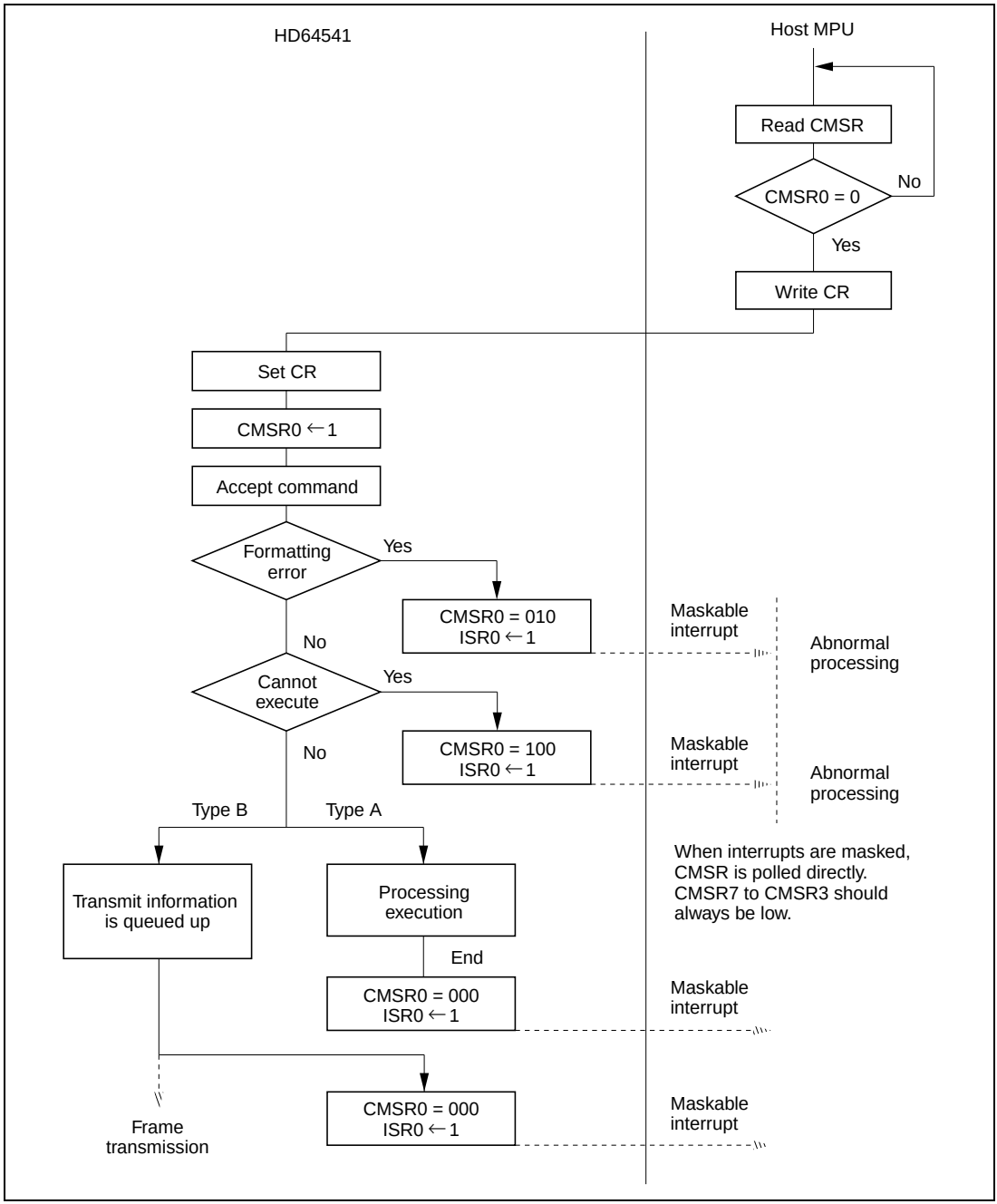


Figure 2-8 Command Processing Flow

2.4 Status

The HD64541 notifies the external microprocessor of the results of command execution or protocol processing by means of status codes passed through the status register (SR).

Table 2-4 lists the valid status codes. See appendix B for more details.

Interrupt source register bit 1 (ISR1) set to 1 indicates that valid status information is available in the SR. ISR1 = 0 or all zeros in the SR indicate the absence of valid status.

Note: When two or more status conditions are pending and an ISR1 = 1 interrupt is generated, the driver software clears ISR1, and reads the SR and processes the status repeatedly until an SR read gets all zeros, indicating no more status.

However, because of the HD64541's internal timing, it is possible for the driver software to read an all-zero SR even though valid status is pending. In this case, the driver software mistakenly concludes that no more status is pending and exits the interrupt. When the HD64541 firmware sets the next status into SR, it also sets ISR1 to 1 to request another status interrupt, so that no pending status conditions are lost.

Figure 2-10 is the status read flowchart.

Either of two methods may be used by the external microprocessor to read the status: interrupt and polling.

2.4.1 Interrupt Method

When interrupt mask register bit 1 (IMR1) = 0, status available interrupts are allowed.

When valid status becomes available in the SR, an interrupt request is generated and the interrupt source register bit 1 (ISR1) is set to 1. The interrupt service routine determines that it is a status available interrupt by noting the value of ISR1 and clearing it before reading the SR. (Clearing ISR1 after reading SR may cause additional pending status available interrupts to be lost.) Because multiple status conditions may be stacked up, the interrupt service routine must re-interrogate ISR1 after reading SR to determine if any more are to be read.

2.4.2 Polling Method

When interrupt mask register bit 1 (IMR1) = 1, status available interrupts are disabled.

The external microprocessor must periodically read the SR to determine whether status is available. In this case the external microprocessor should first read SR-H (or SR-HH) because SR-L (or SR-LL) read indicates the completion of the full SR read. All zeros in the SR indicate the absence of status.

Establish Link (DESI)

Status code	Parameter 1	Parameter 2	Parameter 3
$01			

Release Link (DRLI)

Status code	Parameter 1	Parameter 2	Parameter 3
$02			

Verify I-Frame (ACIF)

Status code	Parameter 1	Parameter 2	Parameter 3
$03			

Indicate Remote Station Busy (SRBY)

Status code	Parameter 1	Parameter 2	Parameter 3
$04			

Indicate Remote Station Busy Release (RRBY)

Status code	Parameter 1	Parameter 2	Parameter 3
$05			

Peripheral Input Pin Level (PITL)

Status code	Parameter 1	Parameter 2				Parameter 3			
$06			PI2	PI1	PI0		PT2	PT1	PT0

Terminate Frame Transmission (TAIF)

Status code	Parameter 1	Parameter 2	Parameter 3
$07		SIIN	

Figure 2-9 Status

Terminate U and X Frame Transmission (TAUF)

Status code	Parameter 1	Parameter 2	Parameter 3
$09		SUXIN	

Receive Frames (FREC)

Status code	Parameter 1	Parameter 2	Parameter 3
$0A		RBIN	

Idle Detection (IDET)

Status code	Parameter 1	Parameter 2	Parameter 3
$10			

System Recovery Request 1 (SRC1)

Status code	Parameter 1	Parameter 2	Parameter 3
$11			

System Recovery Request 2 (SRC2)

Status code	Parameter 1	Parameter 2	Parameter 3
$12			

Remote Station System Recovery Request (YRCV)

Status code	Parameter 1	Parameter 2	Parameter 3
$13			

Flag Synchronization (FSYC)

Status code	Parameter 1	Parameter 2	Parameter 3
$14			

Reset Link (LRST)

Status code	Parameter 1	Parameter 2	Parameter 3
$16			

Figure 2-9 Status (cont)

Table 2-4 Status

Command	Symbol	Code	Parameters	Description	Operation Mode	
					Protcol	Trans-parent
Establish link	DESI	$01	—	Responded to request from remote station by trying to establish link	✓	—
Release link	DRLI	$02	—	Released or prohibited link establishment by remote station	✓	—
Verify I-frame	ACIF	$03	ASIIN	Verifies that I-frame has been transmitted to remote station	✓	—
Remote station busy	SRBY	$04	—	Indicates that remote station is busy	✓	—
Remote station busy release	RRBY	$05	—	Indicates that remote station is released from busy state	✓	—
Peripheral input pin level	PITL	$06	PI2-PI0, PT2-PT0	Level of peripheral input changed	✓	✓
Terminate frame transmission	TAIF	$07	SIIN	Completed frame transmission	—	✓
Terminate U and X frame transmission	TAUF	$09	SUXIN	UI, XID and TEST frames terminated	✓	—

Table 2-4 Status (cont)

Command	Symbol	Code	Parameters	Description	Operation Mode	
					Protcol	Trans-parent
Receive frames	FREC	$0A	RBIN	I, UI, XID ,and TEST frames received correctly	✓	✓
Idle detection	IDET	$10	—	Detected idle pattern for more than T3	✓	✓
System recovery request 1	SRC1	$11	—	FRMR response received	✓	—
System recovery request 2	SRC2	$12	—	T1 runout occurred N2 times	✓	—
Remote station system recovery request	YRCV	$13	—	Unrecoverable frame by retransmission received and FRMR response sent	✓	—
Flag synchronization	FSYC	$14	—	Flag sequence received	✓	✓
Reset link	LRST	$16	—	Starts link reset by local station	✓	—

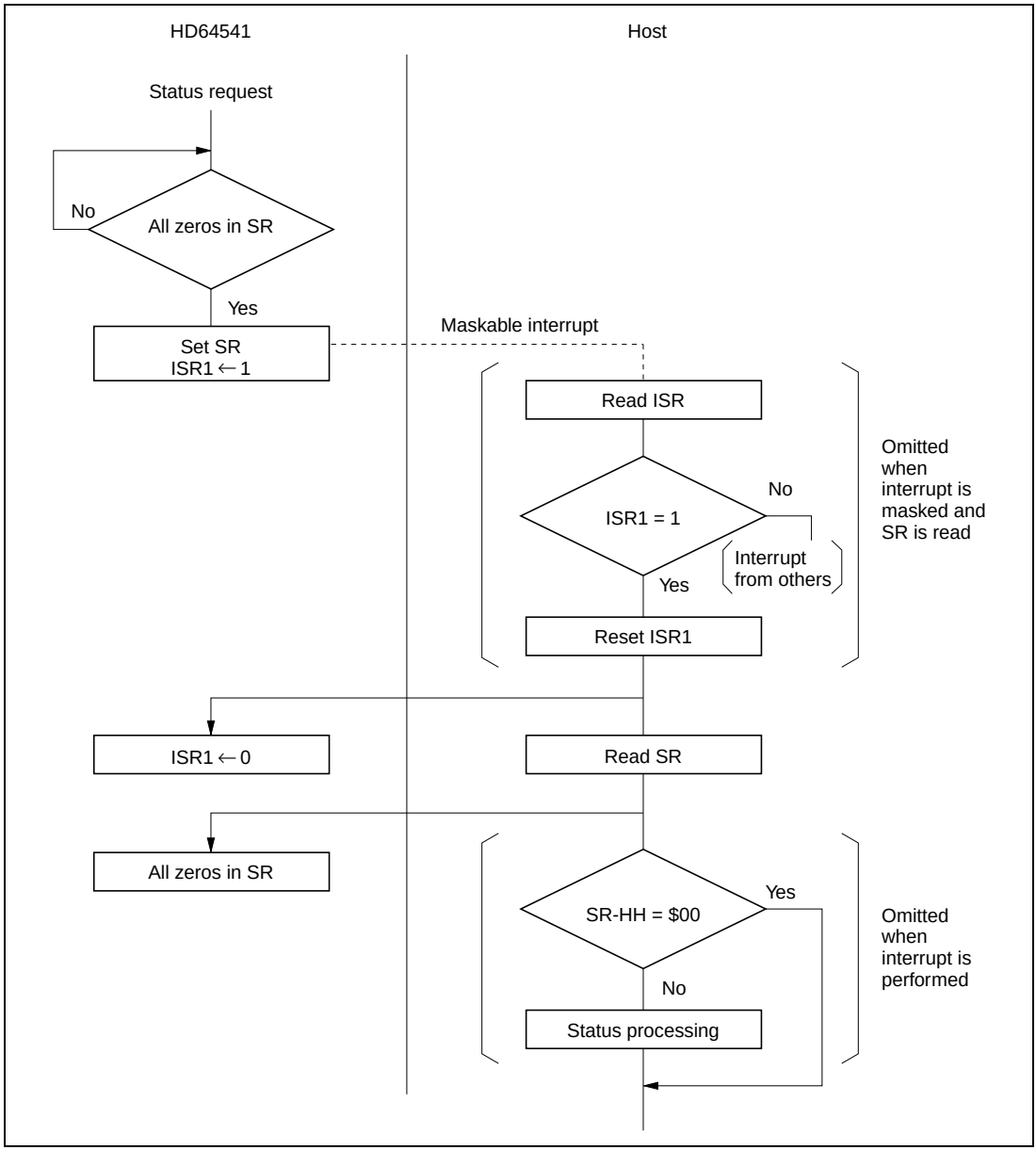


Figure 2-10 Status Read Flow

2.5 Tables Implemented In External Memory

The HD64541 operates on command issued from the external microprocessor. And the HD64541 reports the results of execution or operation state to the external microprocessor if necessary.

Figure 2-11 shows nine types of tables provided in external memory and their logical interfaces with the HD64541. The tables are listed in table 2-5.

Table 2-5 External Memory Table List

Abbrev.	Name	Size	Contents
SYSPT	System parameter table	32	Overall operating parameters for the HD64541 (For example: protocol mode, N1, N2, K, T1, T2,T3)
REJIT	Reject frame information table	16	Rejected frame buffer descriptor
SIIT	Sending I-frame information table	2 + (16 × NSI) (see note)	Transmit I-frame buffer descriptors
SUXIT	Sending U, X frame information table	2 + (8 × NSUI) (see note)	Transmit UI, XID, and TEST frame buffer descriptors
SDB	Transmit data buffer	—	I-field to be transmitted
RBIT	Receive buffer information table	16 × NRBI (see note)	Receive I-, UI, XID, and TEST frame buffer descriptors
RDB	Receive data buffer	—	I-field received
SYSDT	System parameter dump table	32	Logout area for current system parameters. Layout is same as SYSPT. Written by the HD64541 on command from the external microprocessor.
LOGT	Statistical information logging table	20	Logout area for statistical information. Written by the HD64541 on command from the external microprocessor.

Note: NSI, NSUI, and NRBI are specified within SYSPT (see 2.5.1, System Parameter Table)

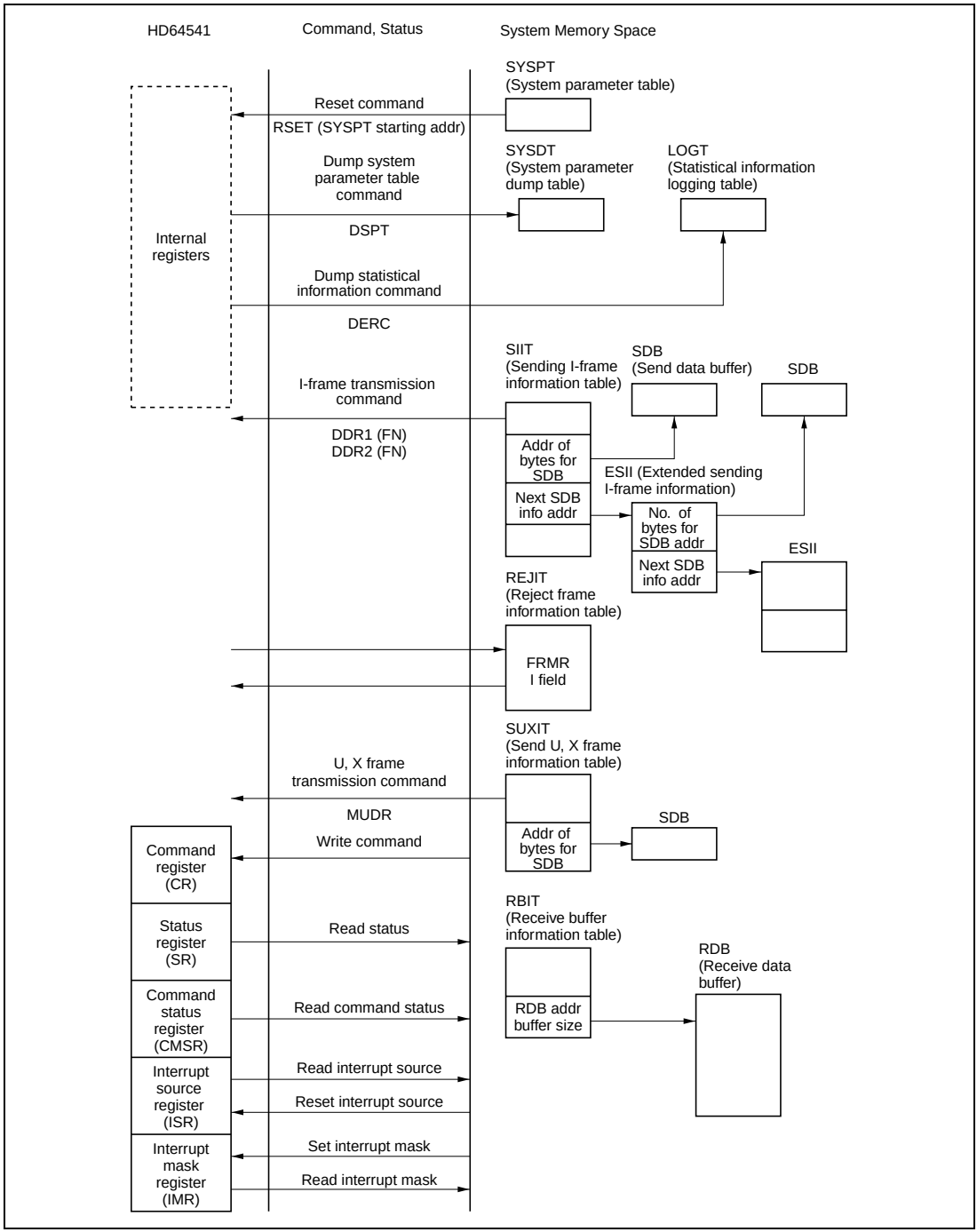


Figure 2-11 External Memory Tables

2.5.1 System Parameter Table (SYSPT)

The SYSPT table passes the values of various parameters that determine operating conditions. Figure 2-12 shows the structure of the SYSPT. Table 2-6 lists the information assigned to each byte of the SYSPT.

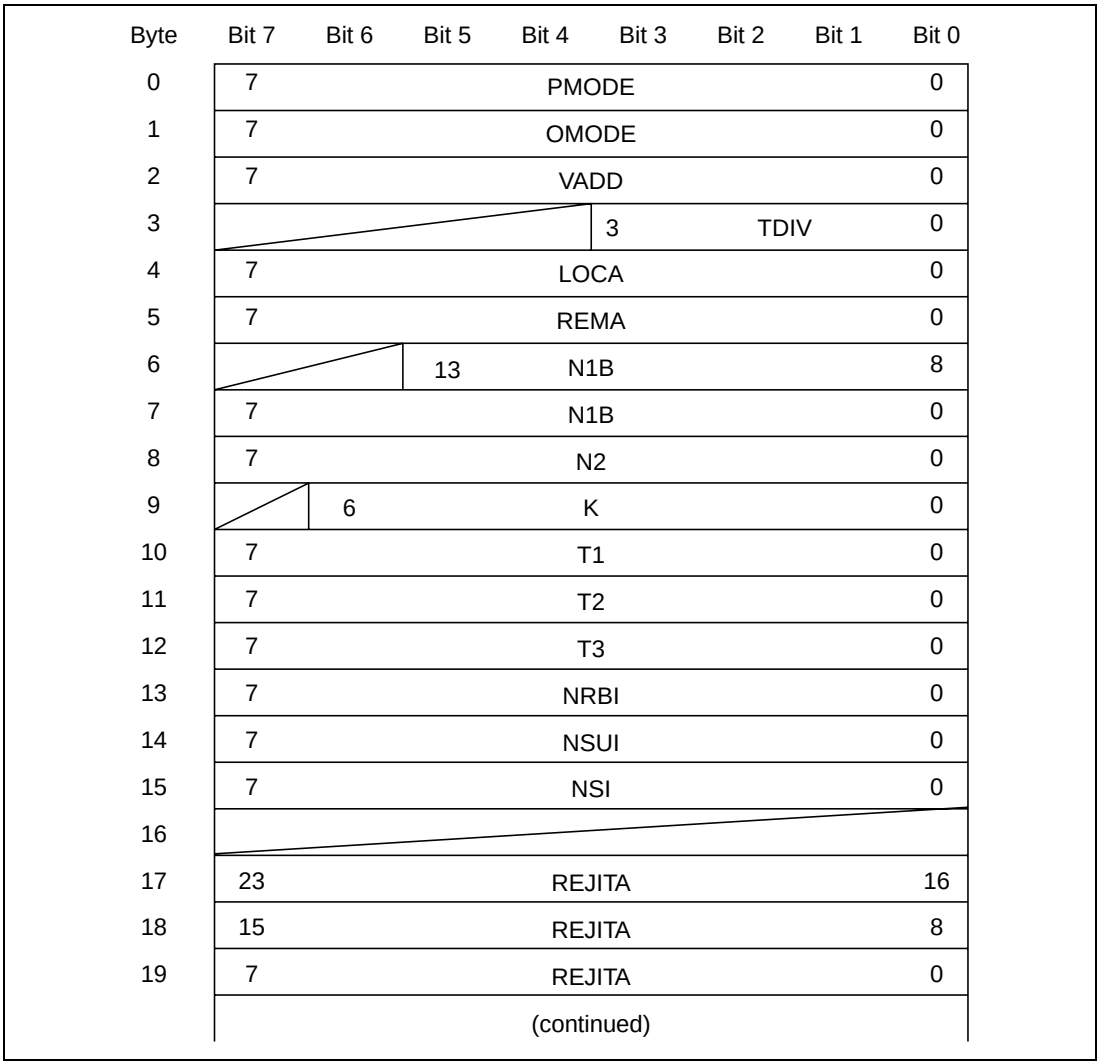


Figure 2-12 System Parameter Table

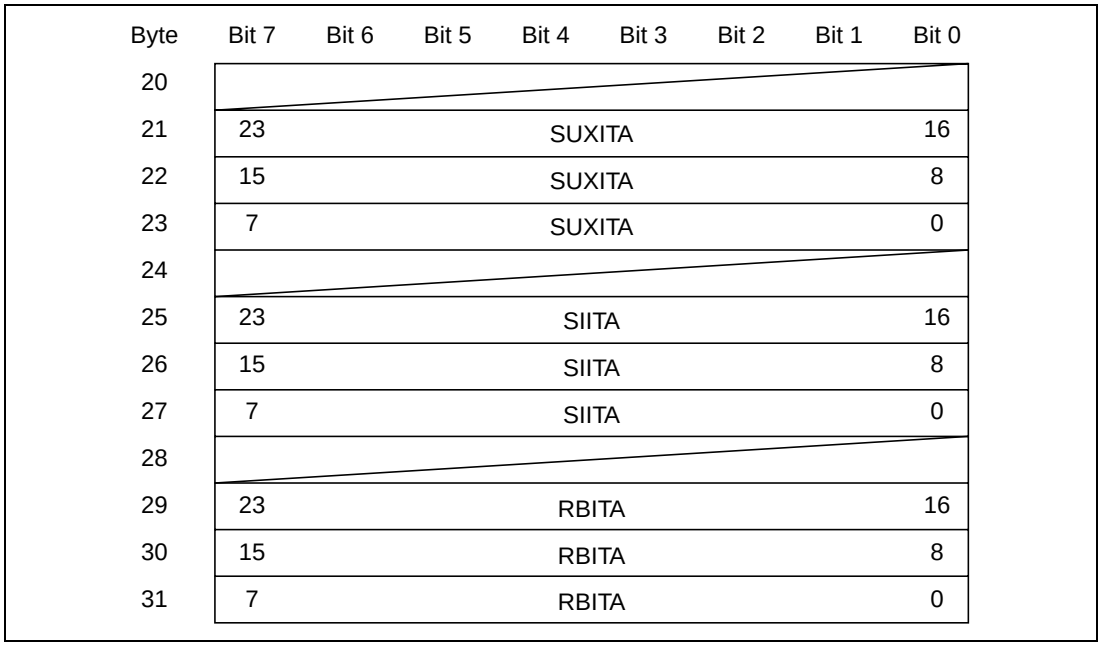


Figure 2-12 System Parameter Table (cont)

Table 2-6 System Parameter Table Assignments

				Operation Mode		
				Protocol Mode		
Name	**Byte**	**Bit**	**Description**	**U, X not Allowed**	**U, X Allowed**	**Trans-parent**
PMODE	0	7	0: Protocol, 1: Transparent		✓ (0)	✓ (1)
		6	0: modulo 8 1: modulo 128		✓	—
		5	Reserved (should be set to 0)		—	—
		4	Delay function for response transmit with T2 0: Transmits response immediately 1: Waits for a duration equal to T2		✓	—
		3	Link disconnection supervisory function with T3 0: Reports link disconnection immediately 1: Waits for a duration equal to T3		✓	✓
		2	Specifies whether to accept U, X frame (UI, TEST, XID) or not. 0: Receive or transmit inhibit 1: Accept	✓ (0)	✓ (1)	—
		1	Timestep for T3 0: 0.1 sec step, 0.1 to 25.5 sec 1: 1 sec step, 1 to 255 sec		✓	✓
		0	Interframe timefill 0: Flag 1: Mark		✓	✓
OMODE	1	5 to 7	Reserved (should be set to 0)		✓	✓
		4	Minimum frame interval when transmitting multiple-frame by one command 0: approx. 80 µs 1: approx. 300 µs (system clock 6 MHz)		✓	✓

Table 2-6 System Parameter Table Assignment (cont)

				Operation Mode		
				Protocol Mode		
Name	Byte	Bit	Description	U, X not Allowed	U, X Allowed	Trans-parent
OMODE	1	1 to 3	Protocol mode bit3 bit2 bit1 0 0 0 X.25 layer 2 0 0 1 X.75 layer 2 0 1 0 T.90 layer 2		✓	—
		0	0: Reserved 1: Normal mode (should be set to 1)		✓	✓
VADD	2	0 to 7	Vector address issued when interrupt acknowledge is received after an interrupt request		✓	✓
TDIV	3	0 to 3	Specify the basic timer frequency with the internal operating clock frequency by MHz unit. 2 to 6 is valid. Note: For the double frequency mode, specify one half of the frequency of the CLK input. (only for the HD64541S)		✓	✓
LOCA	4	0 to 7	Local station address		✓	—
REMA	5	0 to 7	Remote station address		✓	—
N1B	6	0 to 5	Number of bytes in the largest			
	7	0 to 7	I-frame information field. (Do not set to 0)		✓	— (See note)
N2	8	0 to 7	Maximum allowable number of transmit retries (Do not set to 0)		✓	—
K	9	0 to 6	Maximum number of outstanding I frames (Shoud be set in 0< K< modulo value)		✓	—
T1	10	0 to 7	Limit value for receive confirmation timer set in units of 0.1 seconds (Do not set to 0)		✓	—
T2	11	0 to 7	Limit value for the delayed acknowledgement timer set in units of 0.1 seconds (Do not set to 0)		✓	—

Table 2-6 System Parameter Table Assignment (cont)

				Operation Mode		
				Protocol Mode		
Name	**Byte**	**Bit**	**Description**	**U, X not Allowed**	**U, X Allowed**	**Trans-parent**
T3	12	0 to 7	Limit value for the link disconnection supervisory timer set in units of 0.1 or 1 seconds (Do not set to 0) It is selected by PMODE bit1		✓	✓
NRBI	13	0 to 7	Number of RBIs (Should be set to NRBI ≥ 3)		✓	✓
NSUI	14	0 to 7	Specifies the number of SUXI (Should be set to NSUI ≥ 1)	—	✓	—
NSI	15	0 to 7	Number of SII (Should be set to NSI ≥ 1)		✓	✓
Reserved	16	0 to 7	Reserved (should be set to 0)		—	—
REJITA	17	0 to 7	Address of REJIT		✓	—
		18	0-7			
		19	0-7			
Reserved	20	0 to 7	Reserved (should be set to 0)		—	—
SUXITA	21	0 to 7	Specifies the address of SUXIT	—	✓	—
	22	0 to 7				
	23	0 to 7				
Reserved	24	0 to 7	Reserved (should be set to 0)		—	—
SIITA	25	0 to 7	Address of SIIT		✓	✓
		26	0-7			
		27	0-7			
Reserved	28	0 to 7	Reserved (set to 0)		—	—
RBITA	29	0 to 7	Address of RBIT		✓	✓
		30	0-7			
		31	0-7			

Note: In transparent mode, any frame received with a frame length exceeding 2^{14} bytes (excluding frame start/end frag and FCS) will be discarded.

2.5.2 Reject Frame Information Table (REJIT)

The REJIT table stores the FRMR frame information field.

The HD64541 performs both read and write access to this table. REJIT can be read from but cannot be written to by the external microprocessor. The external microprocessor only needs to reserve an area in memory by specifying the address of this table in REJITA of the SYSPT; it does not have to specify table values.

This table is not used in transparent mode.

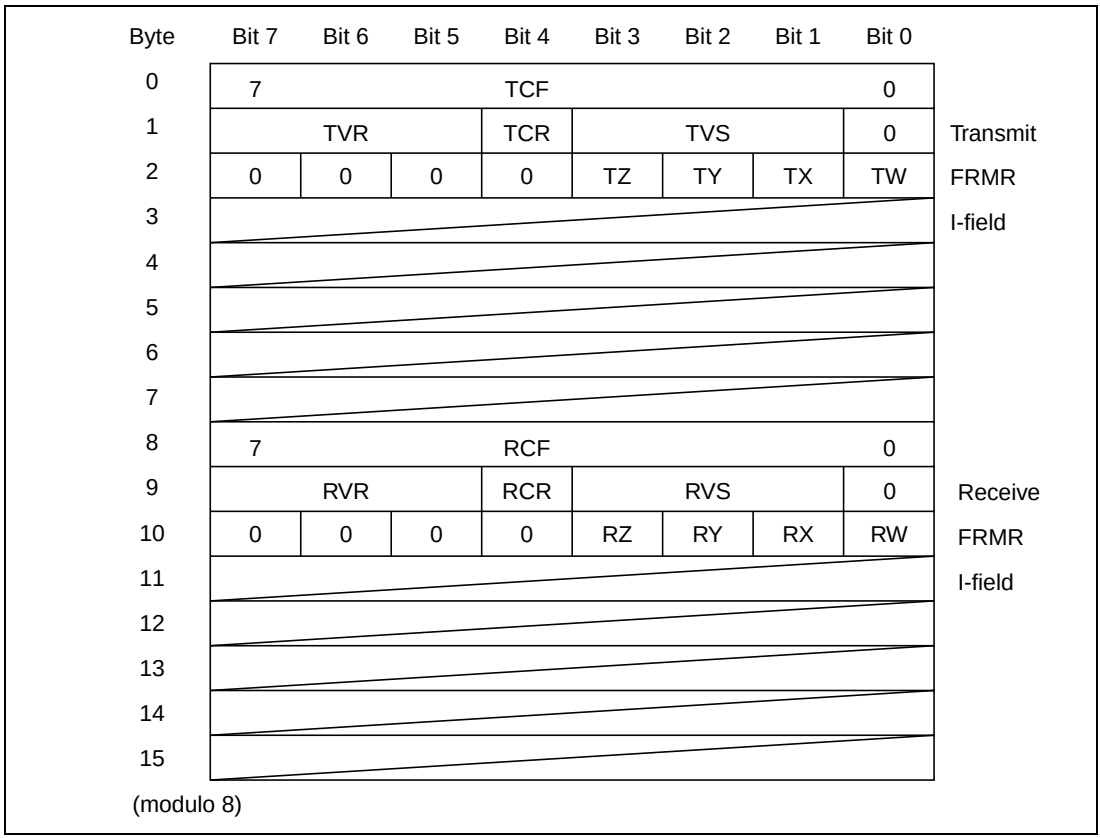


Figure 2-13 Reject Frame Information Table

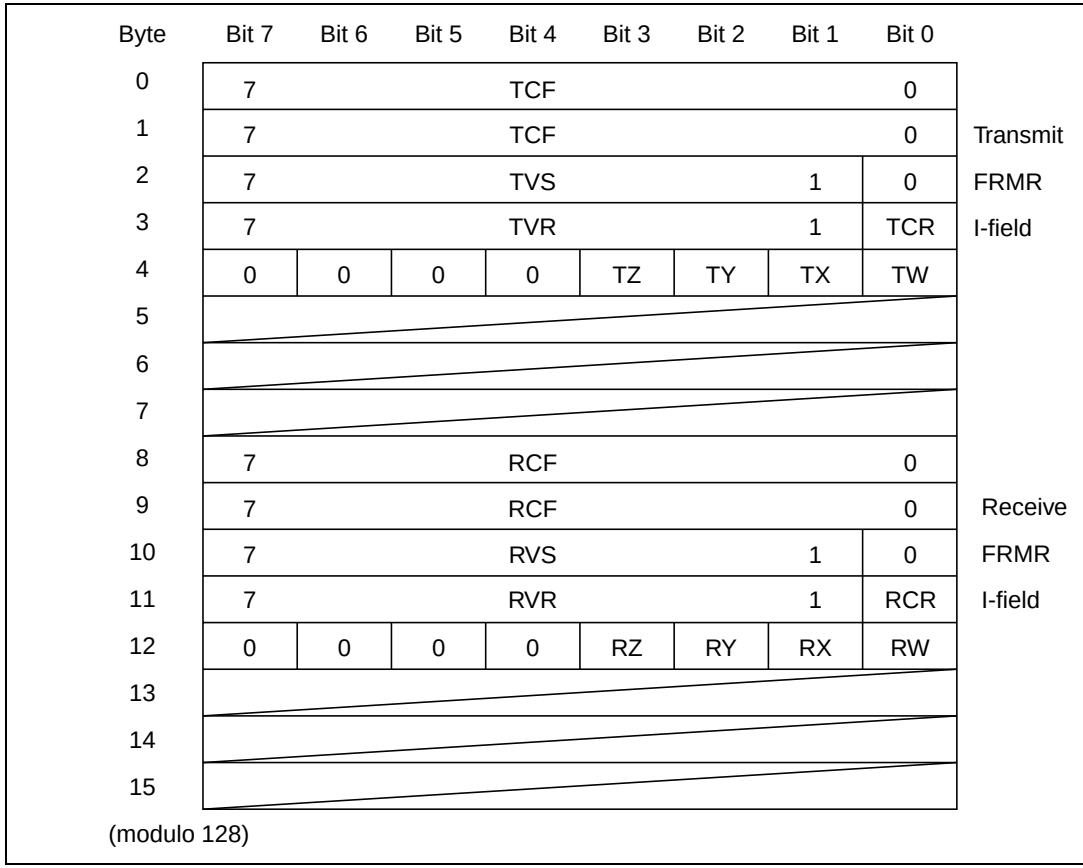


Figure 2-13 Reject Frame Information Table (cont)

Table 2-7 Reject Frame Information Table Assignments

	Modulo 8		Modulo 128		
Name	**Byte**	**Bit**	**Byte**	**Bit**	**Description**
TCF	0	0 to 7	0	0 to 7	Control field of rejected frame.
			1	0 to 7	
TVS	1	1 to 3	2	1 to 7	Send state variable of local station during FRMR transmission.
TCR	1	4	3	0	If the rejected frame is response,TCR is set to 1; if the rejected frame is command, to 0.
TVR	1	5 to 7	3	1 to 7	Receive state variable of local station during FRMR transmission.
TW	2	0	4	0	If the control field of received frame is undefined, TW is set to 1.
TX	2	1	4	1	TX set to 1 indicates that received frame contains an information field which is not permitted in this frame. TX is also set to 1 if the length of received S or U frame is invalid. TW must be set to 1 together with this bit.
TY	2	2	4	2	If the length of the information field in the received I-frame is longer than N1, TY is set to 1. TY and TW are not set to 1 concurrently.
TZ	2	3	4	3	TZ is set to 1 if received N(R) value is invalid. TZ and TW are not set to 1 concurrently.
—	3 to 7		5 to 7		Reserved
RCF	8	0 to 7	8	0 to 7	Control field of rejected frame.
			9	0 to 7	
RVS	9	1 to 3	10	1 to 7	Send state variable of remote station when transmitting FRMR.
RCR	9	4	11	0	If the rejected frame is response, RCR is set to 1; if the rejected frame is command, to 0.
RVR	9	5 to 7	11	1 to 7	Receive state variable of remote station when transmitting FRMR.
RW	10	0	12	0	RW is set to 1 if the control field of a frame received at the remote station is undefined.
RX	10	1	12	1	RX set to 1 indicates that the frame received at the remote station contains an information field which is not permitted in this frame. RX is also set to 1 if the length of S or U frame received at the remote station is invalid. If RX is set to 1, RW is also set to 1.

Table 2-7 Reject Frame Information Table Assignments (cont)

	Modulo 8		Modulo 128		
Name	**Byte**	**Bit**	**Byte**	**Bit**	**Description**
RY	10	2	12	2	RY is set to 1 if the length of the information field of an I frame received at the remote station is longer than N1. RY and RW are not set to 1 concurrently.
RZ	10	3	12	3	RZ is set to 1 if N(R) received at the remote station is invalid. RZ and RW are not set to 1 concurrently.
	11 to 15		13 to 15		Reserved

2.5.3 Sending I-Frame Information Table (SIIT)

The SIIT (figure 2-14) is a specifiable length table that holds data buffer descriptors for I-frames to be transmitted. It contains one entry per I-frame (each entry is known as an SII). The starting address of SIIT is kept in the SYSPT. The size of the SIIT (NSI) is expressed in terms of the number of SIIs it contains. Table 2-8 describes the SIIT contents.

The SIIT is also used in transparent made.

Table 2-8 Sending I-Frame Information Table Assignments

Name	Byte	Bit	Description
NSIIN	0	0 to 7	Index to the next active buffer descriptor (SII), which specifies the next I-field to be transmitted when the transmit I-frame command is received from the external microprocessor
SBC	2 3	0 to 4 0 to 7	Length in bytes of buffer data to be transmitted. When buffers are chained together using the CD indicator and ESII descriptors, SBC specifies only the length of the current buffer. An SBC field in the ESII specifies the length of the buffer associated with that ESII. (see note 1)
SAD	5 to 7	0 to 7	Starting address of the transmission buffer
CD	8	0	Indicates chained data (frame overlaps with the next buffer) 0: Data not chained 1: Data chained
CTAD	11 to 13	0 to 7	Indicates starting address of the ESII table, which stores information for the next chained data buffer (ESII has the same format as the SII (see note 2))

Notes:
1. A value of 0 in the SBC field of the SII causes the I-frame to be transmitted without an I-field. A value of 0 in the SBC of an ESII causes the I-frame to be aborted when that ESII is fetched to continue the chained buffer I-frame transmission.
2. The ESII has the same format as the SII. The ESII need not be allocated storage in memory contiguous with the SII.

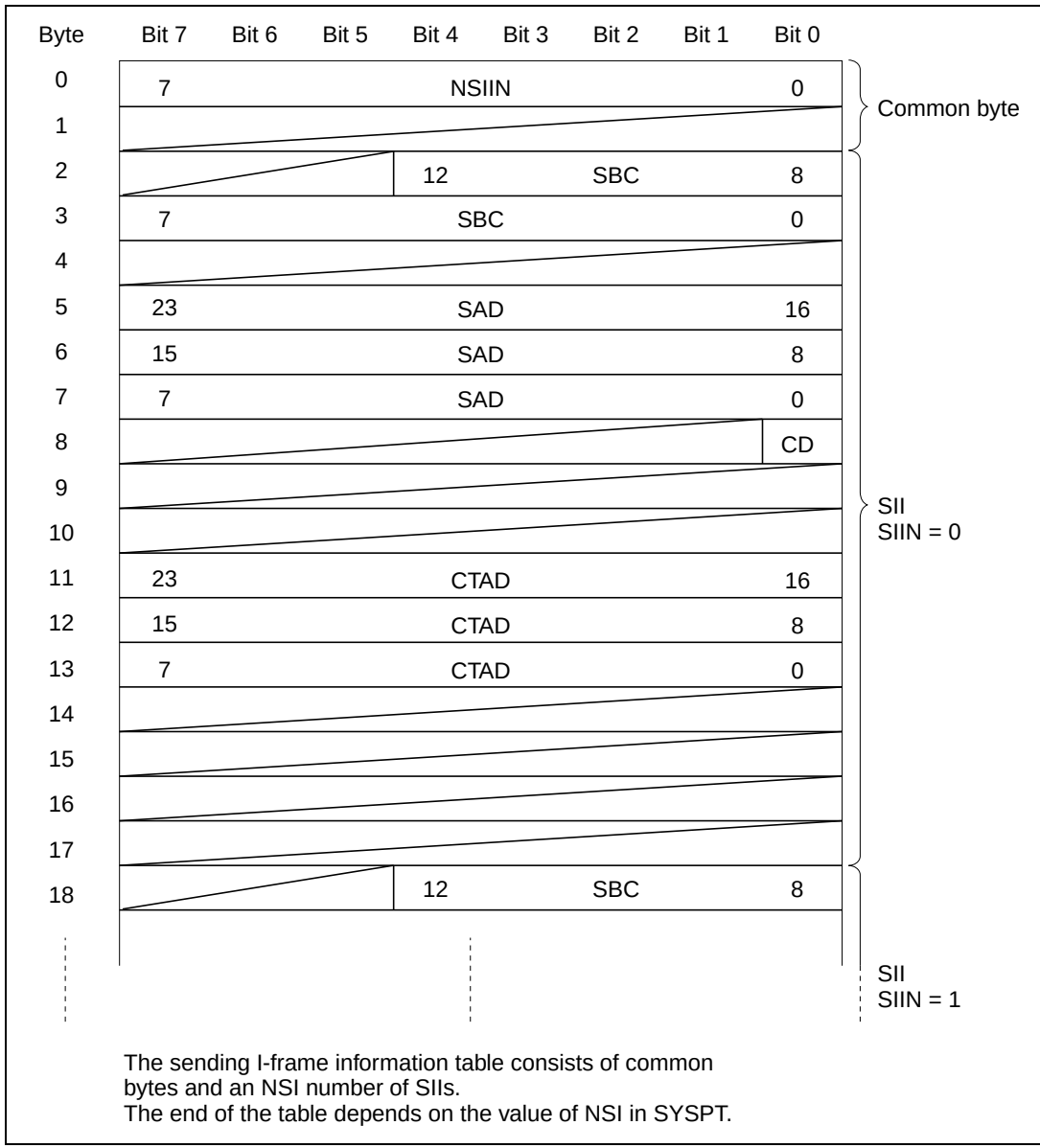


Figure 2-14 Sending I-Frame Information Table

2.5.4 Sending U, X Frame Information Table (SUXIT)

The SUXIT (figure 2-15) is a specifiable length table that holds output data buffer descriptors for UI, XID and/or TEST frames to be transmitted. It contains one entry per frame (each entry is known as an SUXI). There is only one SUXIT for the HD64541. The starting address of the SUXIT is kept in the SYSPT, as is its size, expressed as the number of SUXIs in the table.

Table 2-9 describes the SUXIT contents.

Note that the HD64541 does not allow for data chaining on transmit UI, XID and TEST frames. If PMODE bit 2 of the SYSPT is set to 0, the SUXIT cannot be used. Moreover, in transparent mode, the SUXIT is not used.

Table 2-9 Sending U, X Frame Information Table Assignments

Name	Byte	Bit	Description
NSUXIN	0	0 to 7	Index to the next active buffer descriptor (SUXI), which specifies the next I-field to be transmitted when the MUDR command to transmit UI, TEST or XID is received from the external microprocessor
TYP	2	5 to 7	Bits: 765 Type of frame 010: TEST command 011: TEST response 100: UI command 101: UI response 110: XID command 111: XID response
G	2	0	Setting G to 1 specifies global address
PF	3	7	Value of the P/F bit for in the control field of the frame to be transmitted (See section 3.1.3)
SBC	4	0 to 4	Length in bytes of the I-field of the frame to be transmitted
	5	0 to 7	
SAD	7	0 to 7	Starting address of SDB
	8	0 to 7	
	9	0 to 7	

Note: If SBC is set to 0, the UI, XID, or TEST frame is sent without an I field.

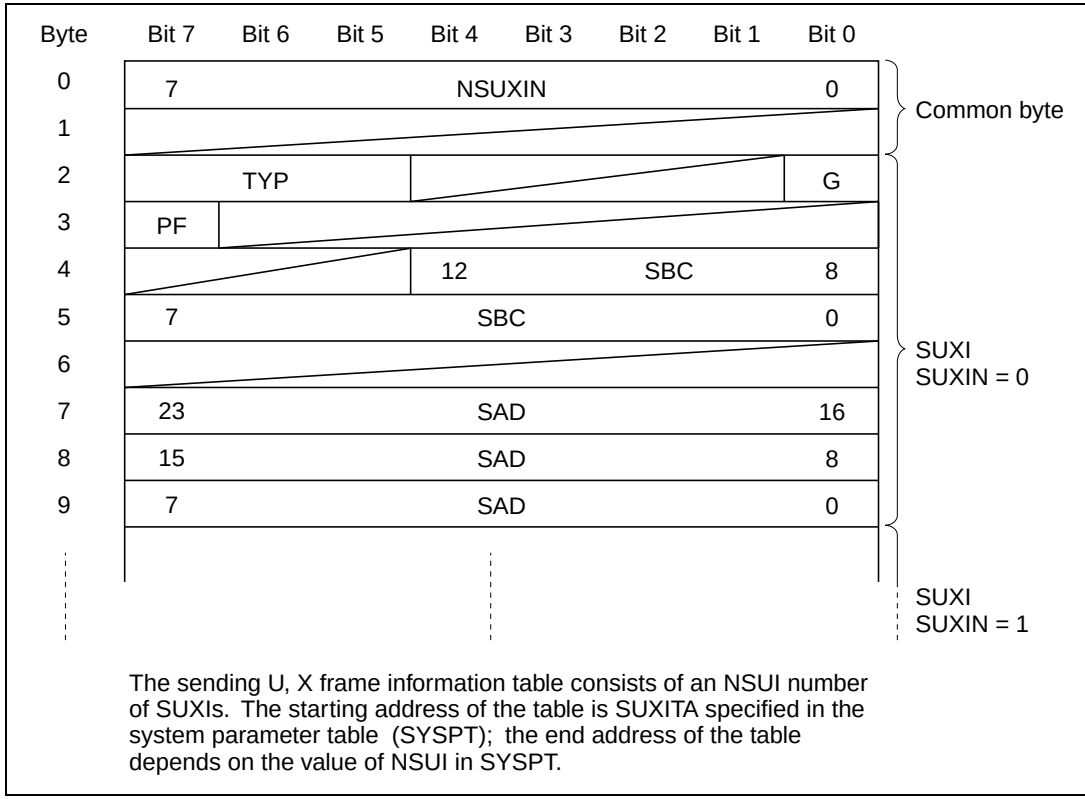


Figure 2-15 Sending U, X Frame Information Table

2.5.5 Transmit Data Buffer (SDB)

The SDB (figure 2-16) holds all or part of an I-field for transmission in an I-, UI, XID, or TEST frame. The SDB address and byte count are stored in the SII or ESII buffer descriptors. Long I-fields may be constructed from multiple SDBs by means of the SII/ESII chaining mechanism.

The SDB data are transmitted in bytes 0,1,2,etc. of SDB from bit 0 to 7 for each byte. The SDB is also used in transparent mode.

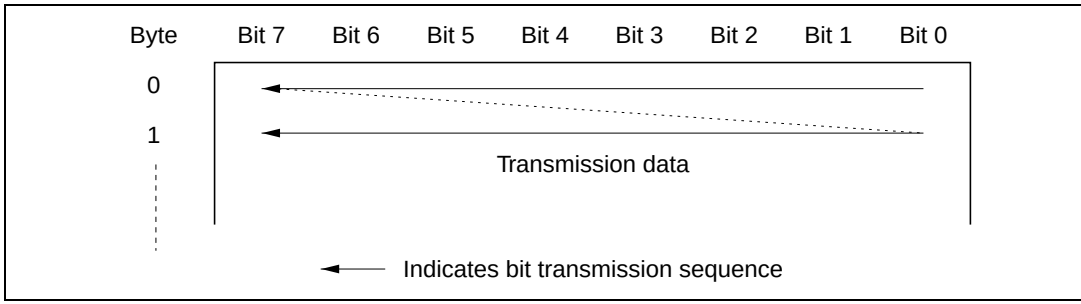


Figure 2-16 Transmit Data Buffer

2.5.6 Receive Buffer Information Table (RBIT)

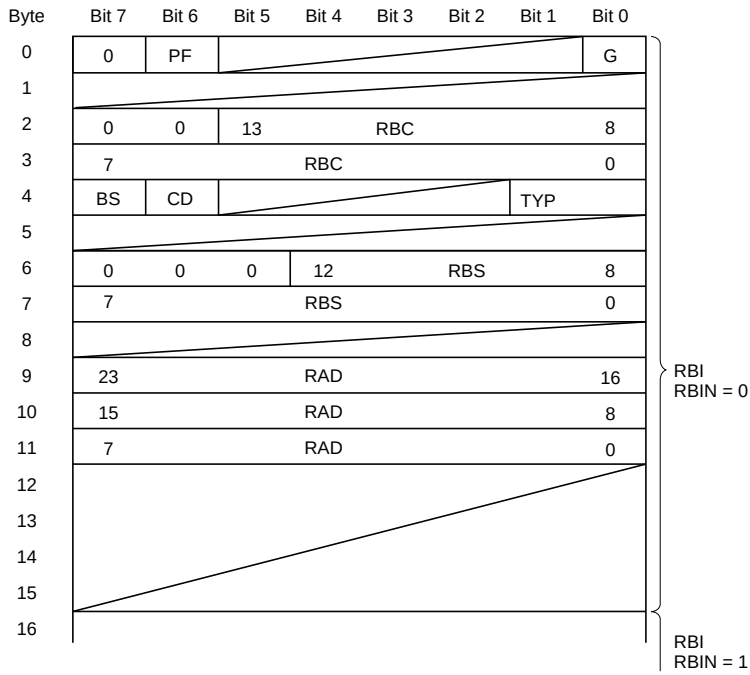
The RBIT (figure 2-17) is a specifiable length table that holds input data buffer descriptors for I-fields that may be received from the remote station. The I-fields may be carried in I-, UI, XID, or TEST frames. It is up to the external microprocessor's software to sort out the received I-fields.

The RBIT contains one entry per input buffer (each entry is known as an RBI). There is only one RBIT for the HD64541. The starting address of the RBIT is kept in the SYSPT, as is the size of the RBIT, expressed in number of descriptor entries. Table 2-10 describes the RBIT contents.

When a frame is received whose I-field does not fit into one buffer, the HD64541 takes the next RBI in the table and continues the receive operation, setting the chained data indicator in the previous RBI. For I-fields chained together in this manner, only the starting RBI contains frame header information.

Table 2-10 Receive Buffer Information Table Assignments

				Operation Mode		
				Protocol Mode		
Name	Byte	Bit	Description	U, X not Allowed	U, X Allowed	Trans-parent
PF	0	6	PF bit value of received frame, invalid in transparent mode or if TYP is 000.		✓	—
G	0	0	Set to 1 when a frame having a global address is received; invalid in transparent mode or if TYP is 000.	—	✓	—
RBC	2 3	0 to 5 0 to 7	Actual byte count of the received I-field–if the I-field spilled over into chained buffers, the RBC field is valid only in the first RBI and is the total byte count across all of the buffers that were chained together to hold the complete I-field. Received byte count excluding flags and the FCS in transparent mode.		✓	✓
BS	4	7	Buffer status–Set high by the external microprocessor when the buffers are ready to receive data and set low by HD64541 after transmission and setting required information in RBI.		✓	✓
CD	4	6	Chained data–Indicates when frames longer than the receive buffer are received (frame will overlap into next buffer). 0: Not chained 1: Chained		✓	✓
TYP	4	0 to 2	Bits: 210 Type of frame received 000: I command 010: TEST command 011: TEST response 100: UI command 101: UI response 110: XID command 111: XID response		✓	—
RBS	6 7	0 to 4 0 to 7	Length in bytes of the receive data buffer (RDB).		✓	✓
RAD	9 to 11	0 to 7 0 to 7 0 to 7	Starting address of RDB.		✓	✓



1. The table consists of RBI sections. The number of RBI sections is NRBI.
2. The starting address of the table is RBITA specified in the system parameter table.
3. The end address of the table depends on the value of NRBI in the system parameter table.
4. Bytes 4 and 5 of an RBI are read and written by both the external microprocessor and HD64541.
5. Bytes 0 to 3 of an RBI are written by the HD64541 and read by the external microprocessor.
6. Bytes 6 to 11 of an RBI are written by the external microprocessor and read by the HD64541.
7. If an I-frame (UI, XID or TEST frame) is stored extending over two or more buffers, TYP, RBC, PF, and G of the frame will appear only in the RBI corresponding to the first buffer.
8. PF, G and TYP are invalid in transparent mode.
9. Global address is valid only for UI, XID and TEST frames. Specification of a global address for frames other than UI, XID and TEST will cause an address field error.
10. If a frame with a global address is received, TYP will show only commands; however, if the frame is received in loopback mode, it will show only responses.

Notes: 1. With chained data, only the values set in the first RBI are valid.
2. When the HD64541 is placed in on-line mode from off-line mode, the LSI starts reading the buffer from the first RBI; consequently, RBIT must be initialized before entering on-line mode.

Figure 2-17 Receive Buffer Information Table

2.5.7 Receive Data Buffer (RDB)

The receive data buffer passes I-field information contained in received frames (I-, UI, XID or TEST frame) to the external microprocessor. The HD64541 accesses the RDB to perform write operations. Figure 2-18 shows the buffer structure .

The received frames are stored in bytes 0, 1, 2, etc. of RDB from bit 0 to bit 7 for each byte. The RDB is also used in transparent mode.

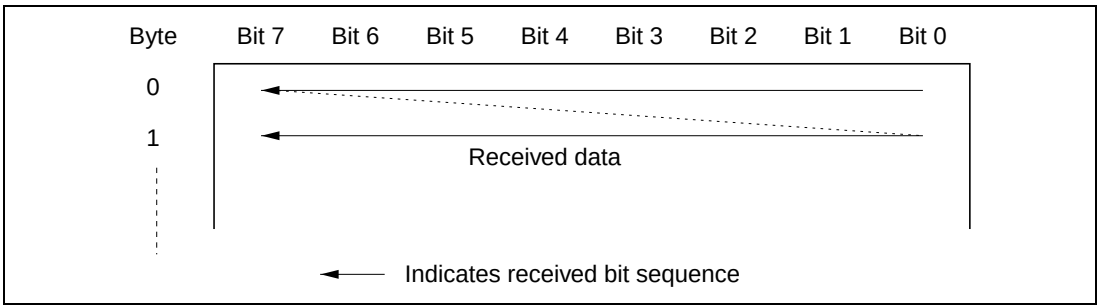


Figure 2-18 Receive Data Buffer

2.5.8 System Parameter Dump Table (SYSDT)

The SYSDT is the logout area used by the HD64541 to dump a copy of its currently active operating parameters on a DSPT command from the external microprocessor. SYSDT's layout is identical to SYSPT's. A 0 is written in each column corresponding to a slash in SYSPT. The SYSDT can also be used in transparent mode.

2.5.9 Statistical Information Logging Table (LOGT)

The LOGT (figure 2-19) is the logout area in external memory into which the HD64541 dumps certain statistical information on command (DERC) from the microprocessor. LOGT consists of one-byte binary counters that freeze when the count reaches 255. DERC resets all of the counters in LOGT.

Figure 2-19 and table 2-11 show table structure and description of each counter, respectively.

Byte No.	
LOGT +0	FCS error
1	Short frame
2	Residual bit frame
3	Abort frame
4	Address field error
5	Overrun error
6	Idle
7	Underrun error
8	Procedure error
9	T1 timer runout
10	Remote station busy
11	Local station busy
12	Retransmission procedure start
13	REJ transmission
14	REJ reception
15	FRMR transmission
16	FRMR reception
17	00
18	00
19	00

Figure 2-19 Statistical Information Logging Table

Table 2-11 Statistical Information Logging Table Assignments

Byte No.	Counter Name	Receive Item Counted	Counter Length (bytes)	Protocol	Trans-parent
0	FCS error	FCS error frame	1	✓	✓
1	Short frame	In modulo 8, short frame is a frame in which the length between flags is less than 4 octets; in modulo 128, the length is less than 5 octets in I, S frames or 4 octets in U frame.	1	✓	✓
2	Residual bit frame	Frames not constructed in units of octets	1	✓	✓
3	Abort frame	Frames that contains a bit string consisting of more than seven consecutive 1s	1	✓	✓
4	Address field error	Frames having an undefined address field including G frame except optional frames	1	✓	—
5	Overrun error	Overrun error in receive buffer	1	✓	✓
6	Idle	Line state transition from flag to idle (not the number of times idle detection status is reported; idle detection status is reported only when T3 timer runout occurs)	1	✓	✓
7	Underrun error	Underrun errors in the transmission buffer	1	✓	✓
8	Procedure error	Number of unexpected frames received except undefined C field frame	1	✓	—
9	T1 timer runout	T1 timer runout	1	✓	—
10	Remote station busy	Remote station busy (not the number of times RNR is received)	1	✓	—
11	Local station busy	Local station busy on established link (Include is both the number of Set Local Station To Busy State commands from the external microprocessor and the number of internal busy occurrences)	1	✓	—
12	Retransmission procedure start	Retransmission start due to check pointing or reception of REJ frame (not number of retransmission I frames)	1	✓	—
13	REJ transmission	REJ command / response transmission	1	✓	—

Note: ✓: Counted
—: Not counted

Table 2-11 Statistical Information Logging Table Assignments (cont)

Byte No.	Counter Name	Receive Item Counted	Counter Length (bytes)	Protocol	Trans-parent
14	REJ reception	REJ command/response reception	1	✓	—
15	FRMR transmission	FRMR response transmission	1	✓	—
16	FRMR reception	FRMR response reception	1	✓	—
17	(reserved)		1	—	—
18	(reserved)		1	—	—
19	(reserved)		1	—	—

Note: ✓: Counted
—: Not counted

Notes: 1. Counters 0 to 5 have higher priority than 8 to 16.

2. If a frame with two or more errors in counters 0 to 5 is received, only one item is counted per frame according to the following priority order:

High	5	Overrun
↑	3	Abort frame
	1	Short frame
	0	FCS error
↓	2	Residual bit
Low	4	Address format error

3. Counter 8 (procedure error) counts received frames with good address field, but which are not expected on protocol procedure.
4. A counter that counts nothing reads 0.
5. The following shows the idle count conditions by counter 6.

IDET status reporting condition

- Receive continuous 1s for a period of at least 15 bit times when line rate is up to 1.5 Mbps.
- Receive continuous 1s for a period of at least 18 bit times when line rate is more than 1.5 Mbps.

Since the HD64541 is designed under the guidelines set forth in CCITT recommendation T.90 layer 2 ('88), X.75 layer 2 ('88), X.25 layer 2('88), you should become familiar with the recommendation before reading this chapter. The HD64541 does not support the multilink operation, only the single link operation of the recommendation. T.90 mode supports information transfer phase in exchange mode of ISDN. (DTE-DTE)

3.1 Frame Structure

Figure 3-1 and 3-2 show the structure of frames transmitted and received by the HD64541.

Transmit bit sequence

12345678	12345678	12345678	16-1	12345678
Flag	Address	Control	FCS	Flag
F 01111110	A 8 bits	C 8 bits	FCS 16 bits	F 01111110

FCS frame check sequence

Transmit bit sequence

12345678	12345678	12345678		16-1	12345678
Flag	Address	Control	Information	FCS	Flag
F 01111110	A 8 bits	C 8 bits	I N bits	FCS 16 bits	F 01111110

FCS frame check sequence

Figure 3-1 Frame Format in Modulo 8

Transmit bit sequence

12345678	12345678	1-*	16-1	12345678
Flag	Address	Control	FCS	Flag
F 01111110	A 8 bits	C * bits	FCS 16 bits	F 01111110

FCS frame check sequence

Transmit bit sequence

12345678	12345678	1-*		16-1	12345678
Flag	Address	Control	Information	FCS	Flag
F 01111110	A 8 bits	C * bits	I N bits	FCS 16 bits	F 01111110

FCS frame check sequence

*: For frame formats containing a sequence number, there are 16 bits.
For frame formats containing no sequence number, there are 8 bits.

Figure 3-2 Frame Format in Modulo 128

3.1.1 Flag

All frames are delimited by a start and end FLAG sequence, which consists of one or more repetitions of the bit pattern 01111110. For frames received by the HD64541, the closing FLAG of one frame may also serve as the opening FLAG of the next successive frame. On transmit, however, the HD64541 always sends at least two flags between successive frames.

7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	0

Figure 3-3 Flag Format

3.1.2 Address Field

Figure 3-4 shows the address field of a frame. The address of the receiving station is written into the command. The address of the sending station is written into the response. The address shown in figure 3-4 is set in SYSPT's LOCA and REMA fields.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A	0	0	0	0	0	0	1	1
B	0	0	0	0	0	0	0	1

Figure 3-4 Address Field Format

3.1.3 Control Field

Table 3-1 and table 3-2 show the bit assignments for the control field of frames transmitted and received by the HD64541. The control field identifies the frame type. Depending on the frame type, it may also carry a receive sequence number N(R), a transmit sequence number N(S), or both. All frames carry a poll/final (P/F) bit.

The N(S) sequence number tags I-frames transmitted by the HD64541. Each successive I-frame gets an N(S) value one higher than the previous, modulo 8 or 128. The N(R) sequence number is the receiver's acknowledgement that transmitted I-frames have been received without error and in proper sequence.

Command frames carry a POLL bit, which may be either 0 or 1, in the POLL/FINAL bit position. Response frames carry a FINAL bit. POLL/FINAL bits are generally used in conjunction with timers to perform checkpointing procedures for transmission error recovery.

3.1.4 Information Field

The contents of the information field consist of an integer number of octets. The HD64541 imposes no limit on the size of the information field that it can transmit. It is up to the user to assure that the maximum I-field transmitted is compatible with the receiver's capability. The HD64541 can receive I-fields up to 16,383 bytes long, representing the maximum value that can be loaded into the SYSPT's 14-bit wide N1B parameter.

3.1.5 FCS (Frame Check Sequence)

The 16-bit FCS sequence is the complement of the sum (modulo 2) of 1 and 2 described below:

1. The remainder of X^K ($X^{15} + X^{14} + ... + X + 1$) divided (modulo 2) by the generator polynomial $X^{16} + X^{12} + X^5 + 1$, where K is the number of bits between the last bit of the opening flag and the first bit of FCS.
2. The remainder of the division (modulo 2) by the generator polynomial $X^{16} + X^{12} + X^5 + 1$, of the product of X^{16} by the content of the frame between the last bit of the opening flag and the first bit of FCS.

Table 3-1 Control Field Bit Configuration in Modulo 8

Control Selection Format	Frame Name	Abbrev.	7	6	5	4	3	2	1	0
Information format (I-frame)	Information	I		N(R)		P		N(S)		0
Supervisory format (S frame)	Receive Ready	RR		N(R)		P/F	0	0	0	1
	Receive Not Ready	RNR		N(R)		P/F	0	1	0	1
	Reject	REJ		N(R)		P/F	1	0	0	1
Unnumbered format (U frame)	Set Asynchronous Balanced Mode	SABM	0	0	1	P	1	1	1	1
	Disconnect Mode	DM	0	0	0	F	1	1	1	1
	Frame Reject	FRMR	1	0	0	F	0	1	1	1
	Disconnect	DISC	0	1	0	P	0	0	1	1
	Unnumbered Acknowledge	UA	0	1	1	F	0	0	1	1
	Unnumbered Information	UI	0	0	0	P/F	0	0	1	1
	Exchange Identification	XID	1	0	1	P/F	1	1	1	1
	Test	TEST	1	1	1	P/F	0	0	1	1

Table 3-2 Control Field Bit Configuration in Modulo 128

Control Selection Format	Frame Name	Abbrev.	7	6	5	4	3	2	1	0
Information format (I-frame)	Information	I				N(S)				0
						N(R)				P
Supervisory format (S frame)	Receive Ready	RR	0	0	0	0	0	0	0	1
						N(R)				P/F
	Receive Not Ready	RNR	0	0	0	0	0	1	0	1
						N(R)				P/F
	Reject	REJ	0	0	0	0	1	0	0	1
						N(R)				P/F
Unnumbered format (U frame)	Set Asynchronous Balanced Mode	SABM	0	1	1	P	1	1	1	1
	Disconnect Mode	DM	0	0	0	F	1	1	1	1
	Frame Reject	FRMR	1	0	0	F	0	1	1	1
	Disconnect	DISC	0	1	0	P	0	0	1	1
	Unnumbered Acknowledge	UA	0	1	1	F	0	0	1	1
	Unnumbered Information	UI	0	0	0	P/F	0	0	1	1
	Exchange Identification	XID	1	0	1	P/F	1	1	1	1
	Test	TEST	1	1	1	P/F	0	0	1	1

3.1.6 Interframe Time Fill

Interframe time fill is accomplished using sequential transmission of flags according to CCITT recommendation. HD64541, however, provides a selection between flags and marks for interframe time fill. The optional selection (marks) is useful during system development debugging. Interframe time fill is selected using PMODE 0 bit (0 = flag; 1 = mark) in the SYSPT. Figure 3-5 shows an example of link setting by remote station and I-frame receipt when mark is selected for interframe time fill.

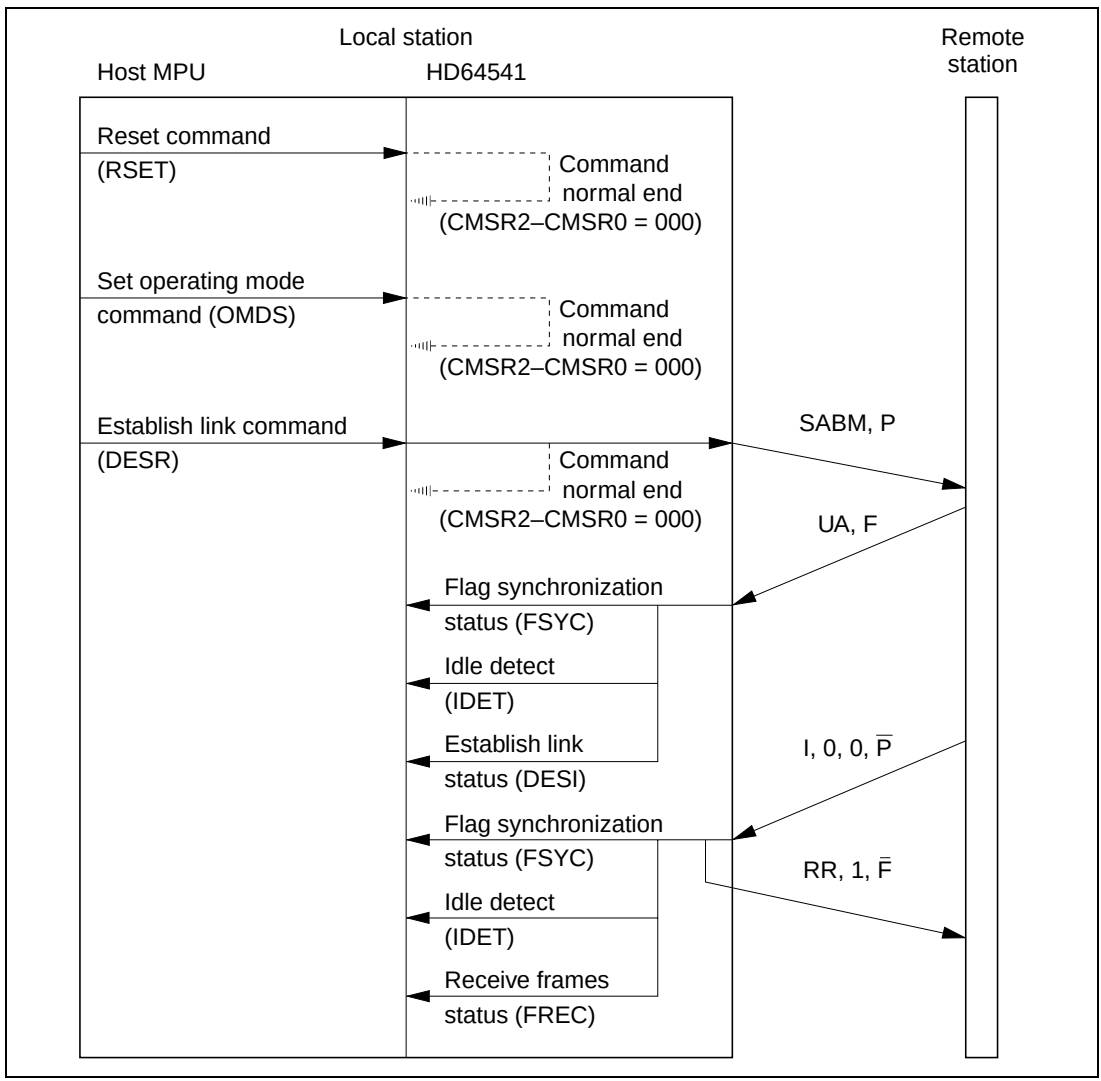


Figure 3-5 Example of Sequence for Interframe Time Fill as Mark

3.2 Frame Type

The types of frames transmitted and received by the HD64541 are classified into command and response as shown in table 3-3.

Table 3-3 Command and Response

Command	Response
I	
RR	RR
RNR	RNR
REJ	REJ
SABM/SABME	
	DM
	FRMR
DISC	
	UA
UI	UI
XID	XID
TEST	TEST

Note: A blank entry indicates an undefined frame.

3.2.1 I Command (Information)

The information (I) command carries higher layer data in its I-field across a logical link. I commands are protected by sequence numbers and are subject to retransmission error recovery and flow control procedures. I-frame transmission is not allowed until a successful SABM/UA (or SABME/UA) exchange has been completed. The HD64541 transmits I-frames on command (DDR1 or DDR2) from the external microprocessor.

3.2.2 SABM Command (Set Asynchronous Balanced Mode) and SABME Command (Set Asynchronous Balanced Mode Extended)

The SABM(in modulo 8)/SABME(in modulo 128) command establishes a logical link for the sequenced exchange of I-frames. SABM/SABME carries no I-field and requires a UA response to complete the handshake. The HD64541 transmits SABM/SABME on command (DESR) from the external microprocessor and waits for a UA response. It automatically transmits a responding UA on reception of SABM/SABME.

3.2.3 DISC Command (Disconnect)

The DISC command takes down a logical link previously established by a SABM/UA (SABME/UA) exchange. DISC carries no I-field and requires a UA response to complete the handshake. Following reception or transmission of DISC, further I-frame transmission on the logical link is prohibited. The HD64541 transmits DISC on command (DRLR) from the external microprocessor and waits for a UA response, but will also accept a DM response. The HD64541 automatically sends a UA response on reception of DISC.

3.2.4 RR Command/Response (Receive Ready)

The RR supervisory frame is used for the following purposes:

1. To indicate that the station sending the RR is ready to receive I-frames.
2. To clear a busy condition set by a previously transmitted RNR.
3. To carry the N(R) acknowledgement sequence number. N(R) = z indicates that all I-frames with N(S) less than z (modulo 8 or 128) have been correctly received.
4. To carry P/F bit = 1 for checkpointing.

RR frames are generated in the normal course of protocol operation by the HD64541, but are also sent on command (RSBY) from the external microprocessor. RSBY release the local station from a busy condition established earlier by SSBY.

3.2.5 REJ Command/Response (Reject)

The REJ supervisory frame explicitly requests retransmission of I-frames starting with the one that carries an N(S) value equal to the N(R) in the REJ. This implicitly acknowledges all I-frames with N(S) less than N(R) (modulo 8 or 128). REJ is transmitted whenever an I-frame is received out of sequence, indicating that the missing frame(s) were likely to have been corrupted by transmission errors and discarded immediately after failing an FCS check.

3.2.6 RNR Command/Response (Receive Not Ready)

The RNR supervisory frame indicates a local busy condition. The transmitter of an RNR is temporarily unable to accept additional I-frames and requests that the receiver of RNR suspend its transmission until further notified by RR. The N(R) sequence number carried in the RNR acknowledges I-frames as normally expected .

RNR frames are generated in the normal course of protocol operation by the HD64541 but are also sent on command (SSBY) from the external microprocessor. SSBY places the local station into a busy condition.

3.2.7 UA Response (Unnumbered Acknowledgement)

The UA frame is the expected response to the SABM/SABME command and the DISC command. For logical link bringup, the SABM/SABME is repeated at T1 timeout intervals until UA is received. For logical link takedown, after a certain number of DISC retransmissions without receiving UA, the logical link is simply declared disconnected.

3.2.8 DM Response (Disconnected Mode)

The DM response reports that the logical link is in disconnected mode and that the SABM/UA (SABME/UA) exchange is required before I-frames may be exchanged. If DM is received in response to SABM/SABME, it indicates that the station receiving SABM/SABME is currently unable to comply with the link establishment request. An unsolicited DM with F = 0 is considered an invitation to transmit SABM/SABME to set up the logical link.

3.2.9 FRMR Response (Frame Reject)

Receipt of FRMR indicates that the station transmitting FRMR has detected an error that is not recoverable by retransmission, such as the following:

1. A frame was received that contained an undefined or not implemented control field value. (which are not indicated in table 3-1 or table 3-2)
2. A supervisory or unnumbered frame with incorrect length was received.
3. A frame was received that carried an invalid N(R) value (one that acknowledges more I-frames than are outstanding on the logical link). N(R) in the range [V(A) ≤ N(R) ≤ V(S)] is valid.
4. An I-frame was received that carries an I-field exceeding a preestablished maximum.
5. An unexpected supervisory frame with F = 1 was received.
6. An unexpected UA, or DM response was received.
7. A frame with an invalid N(S) was received.

An information field holds the reason for an FRMR response. Figure 3-5 shows the format of the information field.

After FRMR is transmitted, the HD64541 goes into error recovery state. It returns to the data link setting state, when in X.25 or X.75 mode, after reception of SABM/SABME from the remote state or after transmitting SABM/SABME after T1 timer runout occurs N2 times.

In the X.75 mode, FRMR response frame is transmitted to notify other error states as follows. In this case, W in the I-field is set to 1.

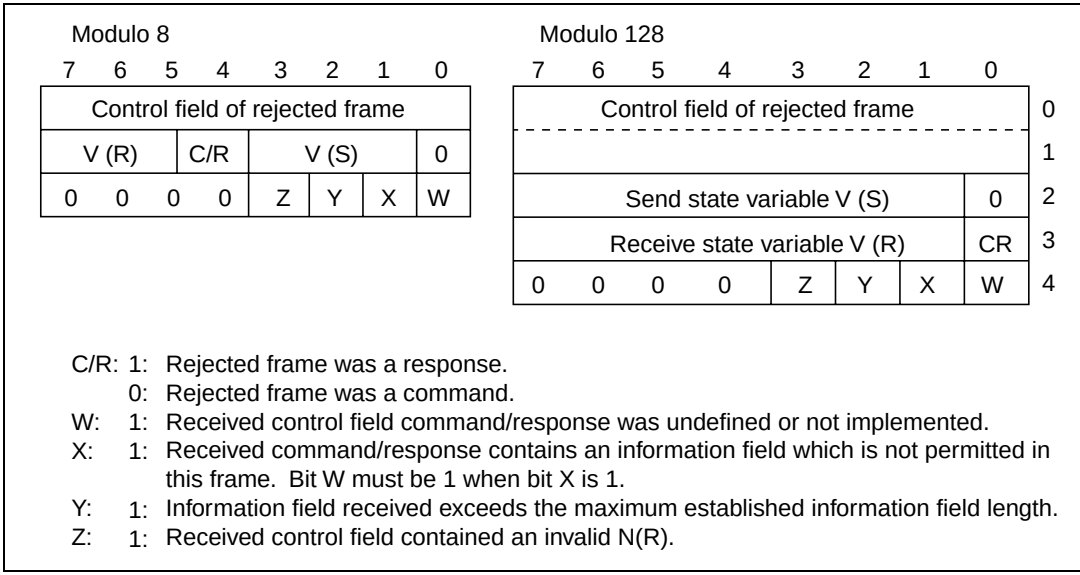


Figure 3-6 FRMR Information Field

3.2.10 UI Command/Response (Unnumbered Information)

The UI frame carries higher layer data in its I-field across a logical link as does the I command described earlier. UI, however, is not subject to sequence numbering, flow control, or transmission error detection or recovery. UI frames may be exchanged over a logical link without a successful SABM/UA(SABME/UA) handshake. Transmission and reception of the UI frame does not affect operation mode or state variables. The HD64541 transmits UI on command (MUDR) from the external microprocessor.

Though CCITT recommendation T.90, X.75, and X.25 do not include UI frames, the HD64541 does provide them. The use of this frame is specified by bit 2 of PMODE in SYSPT. If UI frame use is not specified, the received UI frame will be treated as an undefined frame.

3.2.11 TEST Command/Response

The TEST frame perform is basic testing data link of: TEST frames may be exchanged over a logical link without a successful SABM/UA SABME/UA handshake. Transmission and reception of the TEST frame does not affect operation mode or state variables. The HD64541 transmits TEST on command MUDR from th external microprocessor.

Though CCITT recommendation T.90, X75, and X.25 do not include TEST frames, the HD64541 does provides them. The use of this frame is specified by bit 2 of PMODE in SYSPT. If TEST frame use is not specified, the received TEST frame will be treated as an undefined frame.

3.2.12 XID Command/Response (Exchange Identification)

XID frames are used to exchange system parameter values. XID frames may be exchanged over a logical link without a successful SABM/UA SABME/UA handshake. Sending or receiving an XID frame has no effect on the operational mode or state variables. The HD64541 transmits XID on command MUDR from the external microprocessor.

Though CCITT recommendation T.90, X75, and X.25 do not include XID frames, the HD64541 does provides them. The use of this frame is specified by bit 2 of PMODE in SYSPT. If XID frame use is not specified, the received XID frame will be treated as an undefined frame.

3.3 Frame Transmission

3.3.1 Bit Transmission Order

Transmission of the address field, control field, and information field begins with the LSB (bit 0), while transmission of the FCS field begins with the MSB (bit 15).

3.3.2 Invalid Frames

The HD64541 discards the following frames as an invalid frame without notifying the sender:

1. A frame that is not properly bounded by a starting flag and an ending flag.
2. In modulo 8, a frame whose length between flags is less than 32 bits. In modulo 128, a frame whose length including a sequence number between flags is less than 40 bits; if it does not have a sequence number, a frame whose length is less than 32 bits.
3. A frame that does not contain an integral number of octets prior to zero-bit insertion or following zero-bit deletion.
4. A frame containing an FCS error
5. A frame having an address other than those shown in figure 3-4.

3.3.3 Abort (Frame Discard)

The HD64541 interprets a string of seven or more 1s as an abort and ignores the frame currently being received.

3.3.4 Transparency

Zero-bit insertion and deletion is used to achieve transparency.

All data link control bit patterns contain at least six consecutive 1 bits. The zero insertion process inserts a 0 bit into the transmit data stream following five consecutive 1 bits, so that no random data patterns will be mistaken for a data link control bit pattern.

The inserted bits are removed at the receiver. Zero insertion and deletion operates between the opening and closing flags of a frame.

3.4 System Parameters and State Variables

3.4.1 System Parameters

The external microprocessor can be set the following system parameters:

Timer T1: The maximum time the receiver is allowed for sending back a required response. T1 can be set in the system parameter table (SYSPT) in increments of 0.1 second up to a maximum of 25.5 seconds.

Timer T2: A timer for delayed acknowledgement. T2 can be set in the system parameter table (SYSPT) in increments of 0.1 second up to a maximum of 25.5 seconds.

Timer T3: The maximum time allowed without flags being exchanged. T3 can be set in the system parameter table (SYSPT) in increments of 0.1 seconds up to a maximum of 25.5 seconds or in increments of 1 second up to a maximum of 255 seconds.

Maximum Number of Outstanding I-Frames K (window size): The number of I-frames that can be successively sent without acknowledgement from the remote station. The maximum value of K that can be set in the system prameter table (SYSPT) is 7 in modulo 8, and 127 in modulo 128.

Maximum Number of Bits (or Octets) in an Information Field N1 (N1B): The maximum number of octets allowed in a received I-field. The maximum value of N1B that can be set in the system parameter table (SYSPT) is 16,383. According to CCITT recommendation, N1 is the length of N1B + address field + control field + FCS field (in bits).

Maximum Number of Retransmissions N2: The maximum number of retransmissions of a frame. The maximum value of N2 that can be set in the system parameter table (SYSPT) is 255.

3.4.2 State Variables

Internal state variables managed by the HD64541 are described below. In modulo 8 all of them range in value from 0 to 7 and are incremented modulo 8. In modulo 128 all of them range in value from 0 to 127 and are incremented modulo 128. The variables cannot be written by the external microprocessor.

Send State Variable V(S): The sequence number of the next I-frame to be transmitted. Initialized to 0 after the SABM/UA(SABME/UA) exchange, V(S) is incremented by one after each I-frame is transmitted.

Acknowledge State Variable V(A): The sequence number of the oldest unacknowledged I-frame still outstanding on the logical link. V(A) is updated whenever an N(R) is received from the remote station that acknowledges additional frames.

Send Sequence Number N(S): The sequence number of a transmitted I-frame. As each I-frame is prepared for transmission, its N(S) field is set to the current value of V(S). V(S) is then incremented by one for the next I-frame.

Receive State Variable V(R): The sequence number of the next I-frame to be received. If the N(S) carried in the next received I-frame does not equal V(R), then a sequence number error has occurred on the logical link and a REJ frame is transmitted with N(R) = V(R). When the next I-frame received carries N(S) = V(R), V(R) is incremented by one.

Receive Sequence Number N(R): The receive sequence number carried in all supervisory and I-frames. N(R) acknowledges reception of all I-frames whose N(S) values are less than N(R). The value of N(R) is equal to the value of V(R) when the carrying frame is prepared for transmission.

Section 4 Communication Control Operation

4.1 Initialization

The external microprocessor must perform the following initialization sequences in order to operate the HD64541.

4.1.1 Reset Operation

Hardware Reset: Reset the HD64541 by applying a low level to input pin $\overline{RES}$ for at least 24 clock cycles. Table 4-1 shows the initial values of the registers immediately following reset. After hardware reset, HD64541 enters "waiting for RSET command" state, and accepts only STAC or RSET commands.

Table 4-1 Register Value at Reset

Register	Value
CR	Cannot be reset
SR	$00000000
ISR	$00
IMR	$3F
CMSR	$00

External Memory Area Codes: An area code is a two-bit value that is placed on the system bus by the HD64541 during DMA operations when the external microprocessor is the H16. HD64541 external memory tables are classified into three storage types that may be segregated by area code. Using the STAC command, the external microprocessor informs the HD64541 of the values to be associated with AC0, AC1, and AC2. This must be done after hardware reset and before software reset. Table 4-2 shows which tables are accessed with which ACn value.

Table 4-2 Area Codes and Tables

Area Code	Read Access	Write Access
AC0	SYSPT, REJIT	SYSDT, LOGT, REJIT
AC1	SIIT, ESII, RBIT, SUXIT	SIIT, SUXIT, RBIT
AC2	SDB	RDB

Software RESET Command: On a RESET command from the external microprocessor, the HD64541 is given the external memory address of the SYSPT table, which it then immediately reads. SYSPT contains system operating parameters that apply to the logical link supported by the HD64541. Changes made to SYSPT after a RESET have no effect until the next RESET.

4.1.2 Establishment of Operating Mode

Three bits, M0, M1, and M2, control the operating mode of the HD64541. They are set by command (OMDS) from the external microprocessor. The three bits individually specify online/offline, local loopback, and auto echo functions. In combination, these bits provide for eight operating modes, as described in table 4-3. Figure 4-1 compares local loopback and local loopback with auto echo. If a flag sequence is received when HD64541 aceepts OMDS command for an online mode, it reports flag synchronization (FSYC) status to the external microprocessor.

Table 4-3 Operation Mode Description

Mode					
M2	**M1**	**M0**	**Line Interface**	**Host MPU**	**Application**
Normal		Online	Frame transmission/reception is possible		Normal operation
		Offline	T: Transmits 1s (mark) continuously R: Receive operation stops	No frame transmit/receive operations performed (Valid commands for this mode are shown in appendix D)	Network operation stops
Local loopback mode		Online	T: Transmits 1s (mark) continuously R: Receive operation stops	Transmitter is internally looped back to the receiver so that the transmit bit stream is not sent to the physical line. Frames received from the external microprocessor by the HD64541 for transmission to the remote are looped back internally and given back to the external microprocessor as though received from the remote. These looped-back frames are processed by inverting command/response and recalculating the FCS. In local loopback, all 1s are transmitted over the physical line to the remote and any bits received over the physical line from the remote are discarded. (TXC is provided.)	Internal loopback test
		Offline		No frames are transmitted/received (Valid commands for this mode are shown in appendix D)	

Table 4-3 Operation Mode Description (cont)

Mode					
M2	**M1**	**M0**	**Line Interface**	**Host MPU**	**Application**
Auto echo mode		Online	The receiver is automatically looped back to the transmitter.	Goes to offline condition	
		Offline	(In this case, RXC is not used. TXC is used as RXC. Phase relation between RXD and TXC satisfies that between RXD and RXC shown in figure 5-7)	No frames are transmitted/received (Valid commands for this mode are shown in appendix D)	Remote loopback test from remote station to local station
Local loopback and auto echo		Online		Transmitter is internally looped back to the receiver so that the transmit bit stream is not sent to the physical line. Frames received from the remote are transmitted back to the remote with no change.	• Internal loopback test • Remote loopback test from remote station to local station
		Offline		No frames are transmitted/received (Valid commands for this mode are shown in appendix D)	

Notes:
1. In loopback mode, frames presented to the HD64541 by the external microprocessor for transmission to the remote have their C/R bits reversed, FCS calculated, and then are processed as though they had been received from the remote.
2. Precautions for modifying the line loop state: When the loopback control bits M1 and M2 are changed while M0 continues to specify online, only the loopback state is changed. The HD64541's internal states are not changed and may result in unpredictable protocol behavior after the loopback states are restored to normal operation. To prevent this, if the loopback modes are entered while online, the external microprocessor must reset the HD64541's internal states by forcing M0 through a transition to offline and then back online. See note 3 concerning the implications of doing this on receive data buffer handling.
3. Locating the next receive data buffer: The RBIT table contains a list of descriptors (RBIs) of empty receive data buffers that the HD64541 may use. It normally steps through the RBIs in order, keeping track of which one is next through an index value saved at the beginning of the RBIT. If the HD64541 goes through an offline to online transition, the index is reinitialized to zero so that the next receive data buffer used will be the one whose RBI appears first in the RBIT. This means that the external microprocessor must rebuild the RBIT before effecting an offline to online transition. A mode change command (OMDS) that does not make an online/offline transition does not reset the RBIT index.

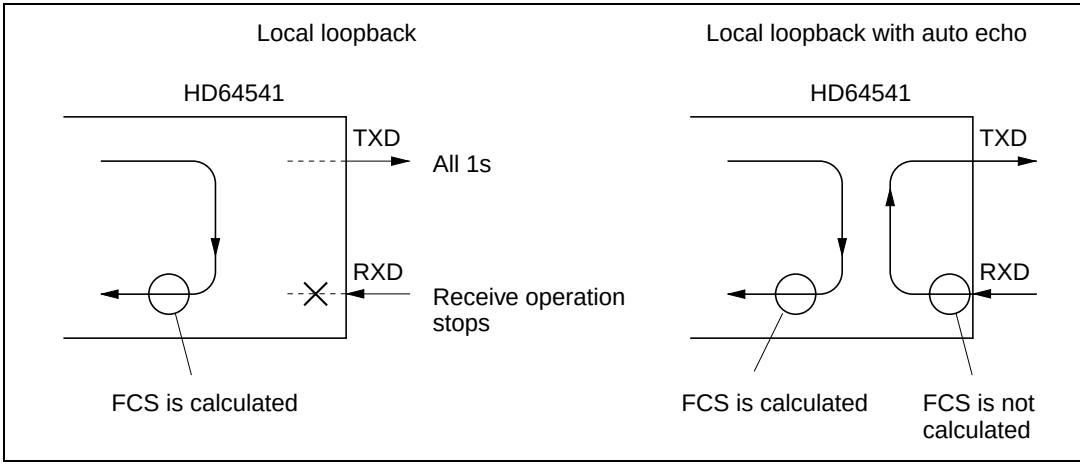


Figure 4-1 Local Loopback and Local Loopback with Auto Echo

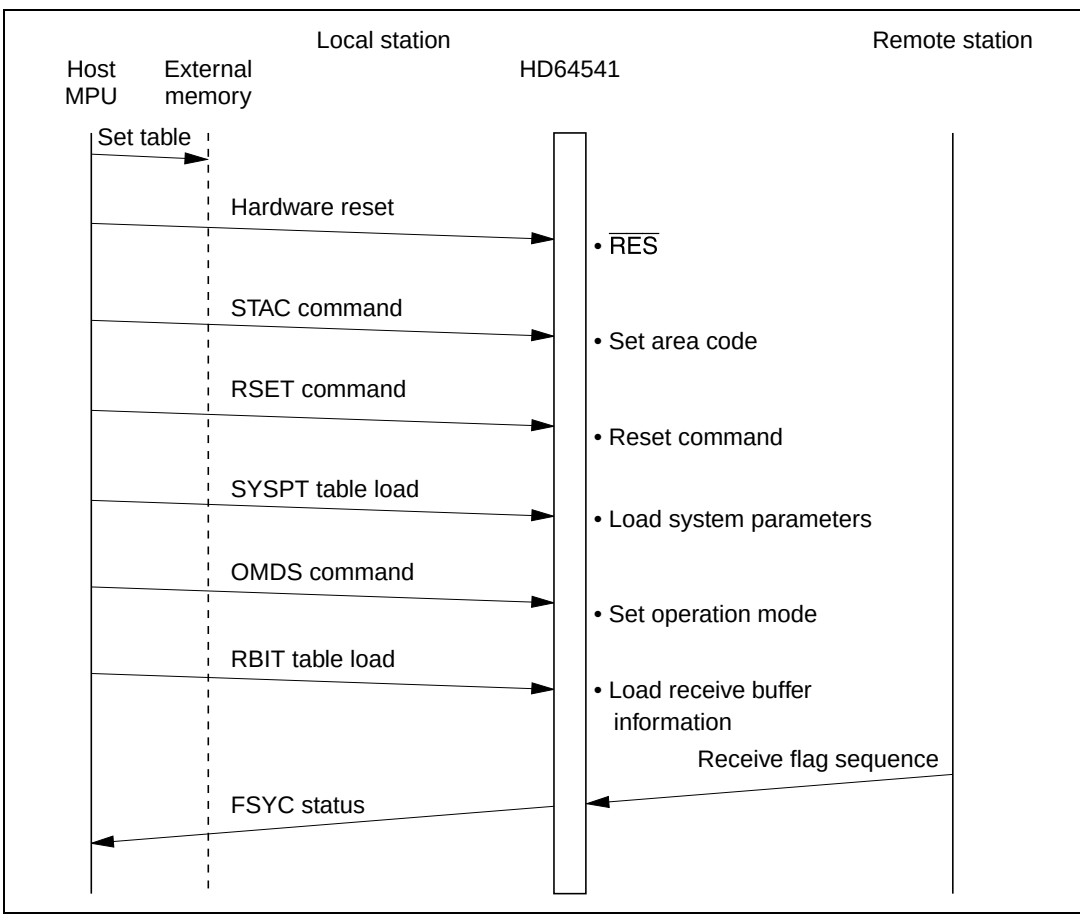


Figure 4-2 Initialization Routine

Figure 4-2 illustrates the process described in this section. Figure 4-3 shows the HD64541's state transitions during initialization.

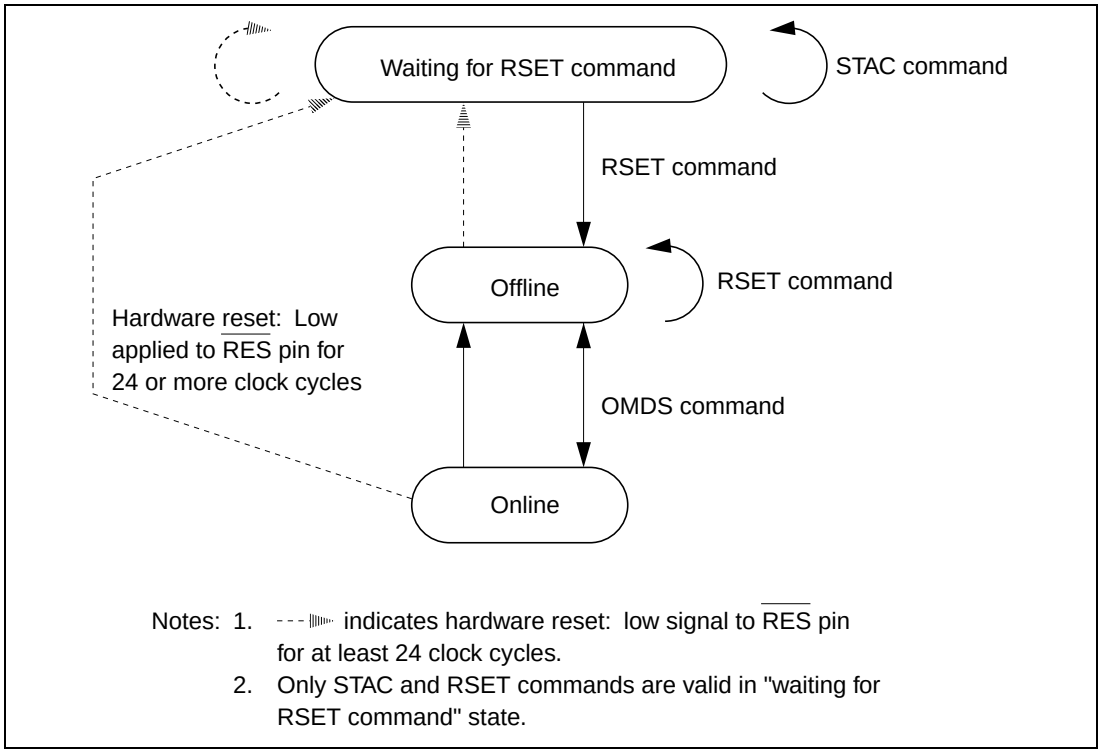


Figure 4-3 HD64541 Initialization State Transitions

4.2 Establishment and Release of Logical Link

The LAPB elements of the procedure described below are illustrated by the sequence diagrams in appendix C. Refer to CCITT recommendations.

4.2.1 Establishing a Logical Link

A logical link is established by a SABM/UA exchange or a SABME/UA exchange. Either the local or remote station can initiate the procedure by transmitting SABM/SABME.

Transmission of SABM/SABME by the Local Station: To establish a logical link, the external microprocessor sends a DESR command to the HD64541.

For each DESR command, the HD64541:

1. Transmits a SABM/SABME (P = 1) command frame to the remote
2. Resets the logical link's internal state machine
3. Resets the logical link's retransmission counter
4. Starts timer T1
5. Posts normal command completion (CMSR2-CMSR0 = 000) to the external microprocessor

On reception of a UA (F = 1) response frame from the remote station, the HD64541 does the following:

1. Stops timer T1
2. Resets internal state variables V(R), V(S), and V(A) to 0
3. Posts DESI status to the external microprocessor (see figure C-2 of appendix C)

Receipt of SABM/SABME by the Local Station: First, the external microprocessor sends a DESW command to the HD64541. On reception of a SABM/SABME (P = 1/0) command frame from the remote station, the HD64541:

1. Transmits a UA (F = P = 1/0) response frame to the remote station
2. Resets internal state variables V(R), V(S), and V(A) to 0
3. Posts DESI status to the external microprocessor (see figure C-3 of appendix C)

Receipt of DM Response by the Local Station (F = 0 for X.25 mode only):

First, the external microprocessor sends a DESW command to HD64541. On the reception of a DM response to request link-set, the HD64541 does the following:

1. Transmits a SABM/SABME (P = 1) command frame to the remote station
2. Resets the logical link's internal state
3. Resets the logical link's retransmission counter
4. Starts timer T1

On reception of the DM (F = 0) response frame from the remote station, the HD64541 does the following:

1. Stops timer T1
2. Resets internal state variables V(R), V(S), and V(A) to 0.
3. Posts DESI status to the external microprocessor (see figure C-3 in appendix C)

4.2.2 Logical Link Release

A logical link is released by a DISC/UA exchange. Either the local or remote station can initiate the procedure by transmitting DISC.

Transmission of DISC by the Local Station: On command (DRLR) from the external microprocessor, the HD64541 does the following:

1. Transmits the DISC (P = 1) command frame to the remote station
2. Starts timer T1
3. Resets the retransmission counter to 0
4. Posts normal command completion (CMSR2-CMSR0 = 000) to the external microprocessor

On reception of the UA (F = 1) or DM (F = 1) response frame from the remote station, the HD64541 does the following:

1. Stops timer T1
2. Returns the logical link to the link release state
3. Posts DRLI status to the external microprocessor (see figure C-2 in appendix C)

Receipt of DISC by the Local Station: On reception of a DISC (P = 1/0) command frame from the remote station, the HD64541 does the following:

1. Transmits a UA (F = P = 1/0) response frame to the remote station
2. Posts DRLI status to the external microprocessor (see figure C-3 of appendix C)

4.2.3 Timer T1 Runout

T1 Runout on Transmission of SABM/SABME: When the HD64541 initiates the logical link establishment procedure by transmitting SABM/SABME (P = 1) to the remote station, it expects the UA (F = 1) or DM (F = 1) response within time interval T1. If the response frame does not arrive before T1 runs out, SABM/SABME (P = 1) is retransmitted. The T1 runout/SABM(or SABME) retransmit cycle is permitted to continue for N2 times before the HD64541 gives up and posts system recovery request 2 (SRC2) status to the external microprocessor. See figure C-4 of appendix C.

T1 Runout on Transmission of DISC: When the HD64541 initiates the logical link release procedure by transmitting DISC (P = 1) to the remote station, it expects the UA (F = 1) or DM (F = 1) response within time interval T1. If the response frame does not arrive before T1 runs out, DISC (P = 1) is retransmitted. The T1 runout / DISC retransmit cycle is permitted to continue for N2 times before the HD64541 gives up and posts system recovery request 2 (SRC2) status to the external microprocessor. See figure C-5 of appendix C.

4.2.4 Independent Link Disconnection

If, after establishing a link, there is no response from the remote station to the transmission of an I-frame (for I-frame transmission, see section 4.3.1), the HD64541 transmits to the remote station a RR frame (P = 1) after occurrence of a T1 runout.

If T1 runout occurs N2 times in T.90 mode, HD64541 notifies the external microprocessor of system recovery request 2 status (SRC2) and releases the link.

If T1 runout occurs N2 times in X.25 or X.75 mode, the HD64541 transmits a SABM/SABME frame (P = 1) to the remote station and at the same time notifies the external microprocessor of system recovery request 2 (SRC2) status and reset link (LRST) status.

If after an SABM/SABME frame transmission timer T1 runout occurs N2 times, the HD64541 notifies the external microprocessor of system recovery request 2 status (SRC2). See figure C-6 of appendix C.

4.3 Data Transmit and Receive

4.3.1 I-Frame Transmission

The external microprocessor prepares an information field for transmission to the remote station by placing it in a transmit data buffer (SDB) in external memory and loading its buffer descriptor entry into the SIIT (for I-frames) or the SUXIT (for UI, XID and TEST frames). A subsequent DDR1 or DDR2 (for I-frames) or MUDR (for UI, XID and TEST frames) command from the external microprocessor directs the HD64541 to transmit.

The external microprocessor specifies the number of I-frames to be transmitted as a parameter in the DDR1 or DDR2 command. The HD64541 manages I-frame sequence numbering, acknowledgement handling, error detection, and retransmission without further intervention from the external microprocessor.

Figure 4-4 shows the structure and interrelationship of the tables that participate in the transmission process.

Preparing I-Fields for Transmission in I-Frames: I-fields to be carried in I-frames transmitted to the remote station are prepared by the external microprocessor in transmit data buffers (SDBs). The addresses and byte counts of the SDBs are stored into consecutive buffer descriptor entries (SIIs) in the SIIT table in the order they are to be transmitted. The first SII that may be used by the external microprocessor to do this is identified by the index NSIIN, which is the first byte of the SIIT.

Each buffer descriptor also contains a data chaining indicator and a pointer to an extension buffer descriptor (ESII). If data chaining is active, then the SDB identified by ESII contains a continuation of the I-field. The format of the ESII is identical to that of the SII, containing the address and byte count of a data buffer, a chaining indicator, and a pointer to another ESII. I-fields of arbitrary length may then be composed of any number of noncontiguous SDBs and chained together for transmission.

Using NSIIN: NSIIN is the first byte of the SIIT. It is an index to the buffer descriptor (SII) entries. Updated by the HD64541 and referenced by the external microprocessor, NSIIN is used to manage the list of outbound I-fields to be transmitted in I-frames to the remote station.

1. When the external microprocessor has additional I-frames that it wants transmitted, the value of NSIIN identifies the first SII buffer descriptor entry that it may use to store the addresses and byte counts of the transmit data buffers (SDBs). The external microprocessor is not allowed to change the value of NSIIN and must use some other means to keep track of the SII entries when more than one frame is added to the transmit list.

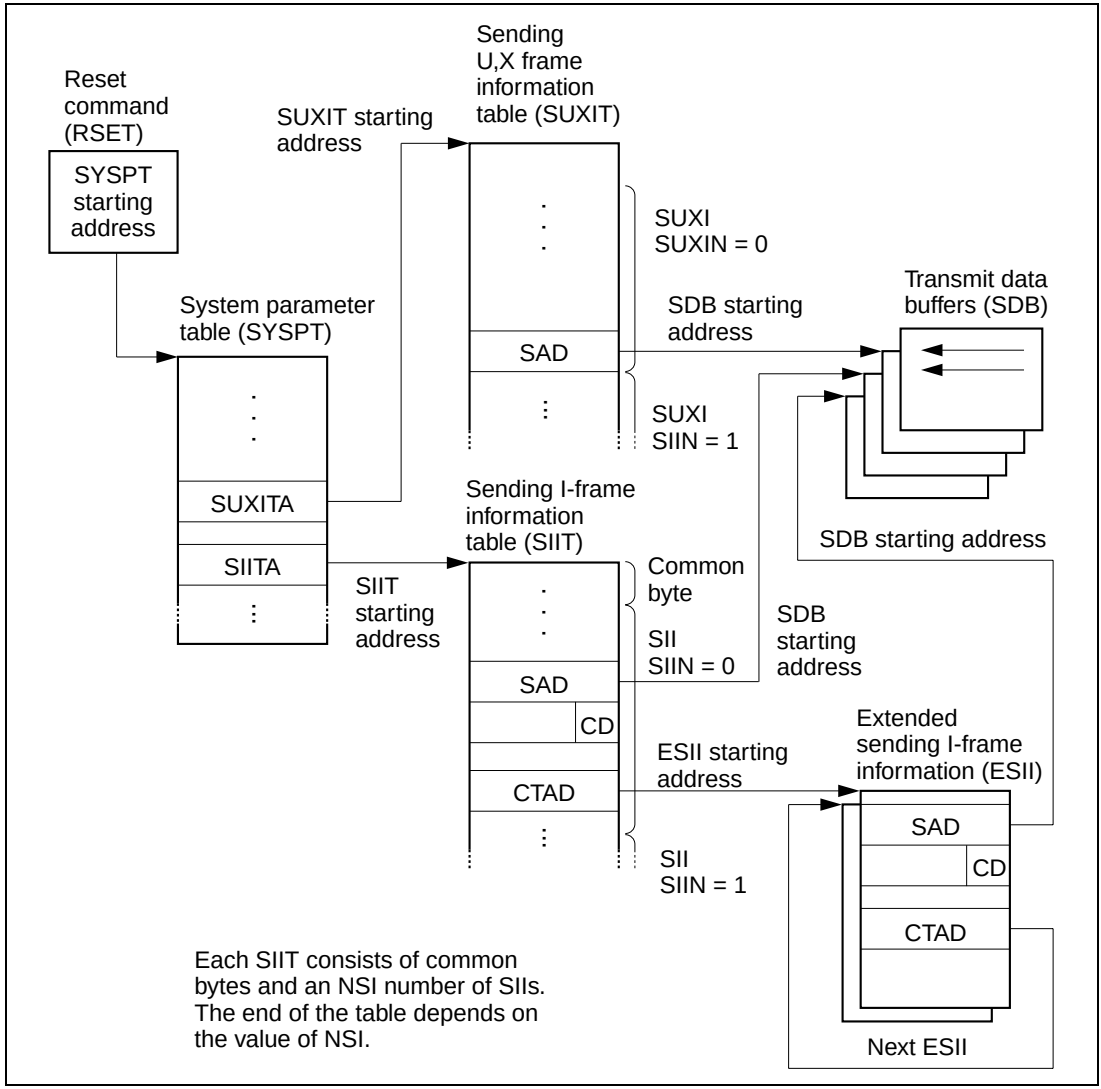


Figure 4-4 Relation between Transmission Tables

2. NSIIN is updated by the HD64541 as follows:
   a. NSIIN is initialized to 0 when:
      i. The HD64541 changes from offline to online mode on a OMDS command from the external microprocessor
      ii. The logical link is established and DESI status is posted
      iii. The logical link is released and DRLI status is posted
   b. NSIIN is incremented by FN on a valid DDR1 or DDR2 command from the external microprocessor. DDR1 and DDR2 direct the HD64541 to transmit the next FN buffers whose descriptors start at the one identified by NSIIN. CMSR = 000 status is posted after NSIIN is incremented.
   c. NSIIN remains unchanged if the DDR1 or DDR2 commands turn out to be invalid and CMSR ≠ 000 status is posted.

   SIIT is effectively a circular buffer containing SIIs and uses NSIIN as its index.
3. While the value of NSIIN is automatically incremented by FN, the number of additional I-frames to be transmitted on the DDR1 or DDR2 command, in case of errors, the external microprocessor should check that the command completion status is CMSR = 000 before generating the next DDR1 or DDR2.

Releasing the Data Buffers of Acknowledged Frames: When acknowledgement is received from the remote station for transmitted I-frames, the HD64541 notifies the external microprocessor by posting status ACIF. The ASIIN value in the SIIT is then the index of the buffer descriptor (SII) for the last acknowledged frame. The external microprocessor then, by comparing the current value of ASIIN with the value at the time of the previous ACIF status, implicitly knows how many frames have been acknowledged. Because the SII entries in the SIIT behave like a circular buffer, a modulo value equal to the number of SIIs must be considered when comparing ASIIN values.

The value of ASIIN accompanying ACIF status may be used to determine the number of newly acknowledged I-frames. The difference between the ASIIN posted with the current ACIF is the number of I-frames acknowledged since the previous ACIF.

If the current ACIF status is the first one since the logical link was (re)established, then ASIIN + 1 is the number of I-frames acknowledged.

Transmit data buffers may be released and their corresponding descriptor entries (SIIs) may be reused in the following cases:

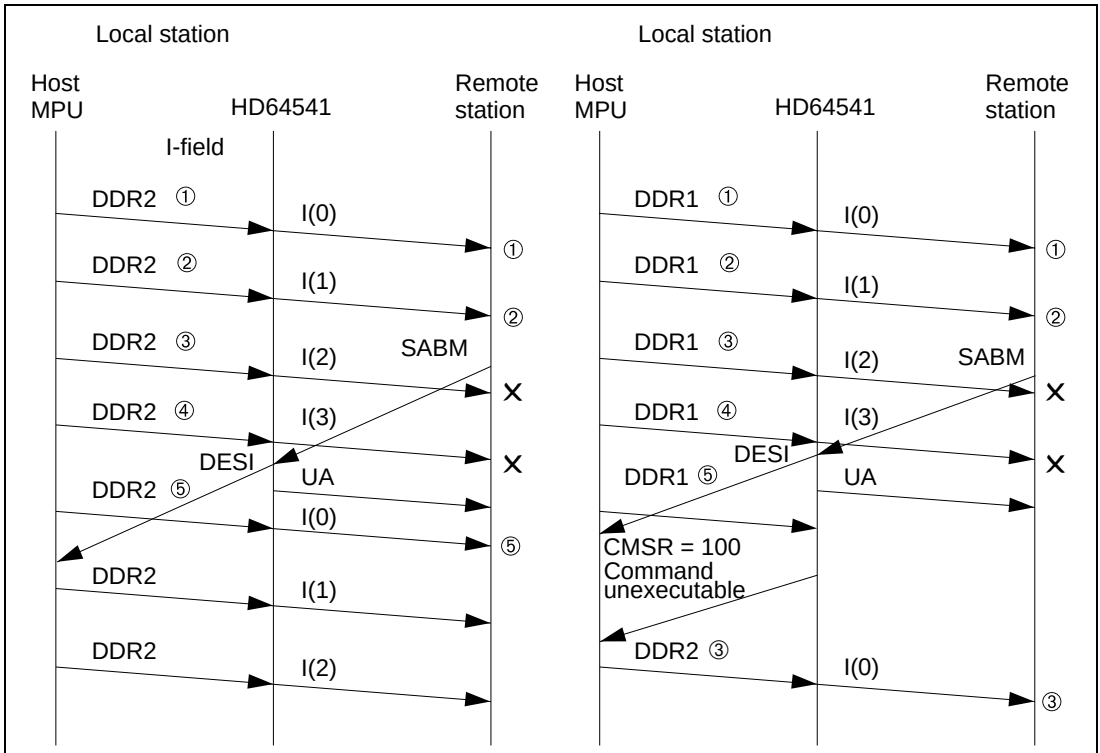
1. Buffers identified by the ACIF status as having been acknowledged by the remote station.
2. All active buffers on a RSET or OMDS command which instructs the HD64541 to go to the offline mode from the online mode.
3. All active buffers when the logical link is released before it receives acknowledgement and DRLI status is posted.

4. All active buffers when the logical link is reestablished and DESI status is posted.

Differences between DDR1 and DDR2 Commands: The DESI status posted following logical link reestablishment will report whether any unacknowledged I-frames were outstanding so that the external microprocessor can reschedule them for transmission. If the external microprocessor chooses to ignore DESI, it will not know of the unacknowledged frames, which are then lost.

DDR1 and DDR2 provide a convenient way of preventing this. The DDR1 command is invalid immediately following the posting of DESI status while DDR2 is not restricted. DDR1 and DDR2 are identical otherwise.

If the DESI status is ignored, the next DDR1 command results in the posting of CMSR = 100 status, forcing the external microprocessor's attention to the fact that DESI was posted. At least one DDR2 command must then be executed before DDR1 becomes a valid command again (figure 4-5).



a) I(2) and I(3) were unacknowledged when the logical link was reestablished. Because the external microprocessor chooses to ignore the DESI status, it does not know enough to reschedule them for transmission.

b) Situation is identical to a) except that DDR1 is used instead of DDR2. The DDR1 command immediately following DESI is rejected by the HD64541 as invalid. The external microprocessor is thereby forcibly notified that DESI was posted and is given the opportunity to reschedule the unacknowledged frames for transmission in the newly established session. One execution of DDR2 makes DDR1 valid again.

Figure 4-5 Use of DDR1 to Force Notice of DESI Status

4.3.2 Transmitting UI, XID, and TEST Frames

Transmittable Frames: The external microprocessor may request the transmission of UI, XID, or TEST commands or responses and arbitrarily set the values of the P/F bit.

Bit 2 of the PMODE in the SYSPT must be set to 1 for transmitting these frames.

Preparing I-Fields for Transmission in UI, XID, and TEST Frames: I-fields to be carried in UI, XID or TEST frames transmitted to the remote station are prepared by the external microprocessor in transmit data buffers (SDBs). The addresses and byte counts of the SDBs are stored into consecutive buffer descriptor entries (SUXIs) in the SUXIT table in the order they are to be transmitted. The first SUXI that may be used by the external microprocessor to do this is identified by the index NSUXIN, which is the first byte of the SUXIT.

The frame type, command/response indicator, P/F bit value, and G bit value are specified for each frame in the SUXI.

Unlike I-frames, UI, XID, and TEST frame I-field data chaining is not supported by the HD64541. The entire I-field to be transmitted must fit within one SDB.

NSUXIN is the first byte of the SUXIT and is an index to the buffer descriptor (SUXI) entries. Updated by the HD64541 and referenced by the external microprocessor, NSUXIN indicates to the external microprocessor which SUXI may be used next to load a descriptor for an outgoing UI, XID, or TEST frame.

NSUXIN is updated by the HD64541 as follows:

1. NSIIN is initialized to 0 when the HD64541 changes from offline to online mode on an OMDS command from the external microprocessor.
2. NSIIN is incremented by 1 on a valid MUDR from the external microprocessor. MUDR directs the HD64541 to transmit the buffer whose descriptor is identified by NSUXIN. CMSR = 000 status is posted after NSUXIN is incremented. Note that unlike DDR1 and DDR2, which initiate a specifiable number of I-frame transmissions, MUDR initiates only one UI, XID or TEST frame transmission per execution.
3. NSUXIN remains unchanged if the MUDR command turns out to be invalid and non-zero CMSR status is posted.

SUXIT is effectively a circular buffer containing SUXIs that uses NSUXIN as its index.

Releasing the Data Buffers of Transmitted UI, XID, and TEST Frames: UI, XID, and TEST frames are unnumbered and therefore not subject to the acknowledgement and retransmission procedures performed on I-frames. As soon as the UI, XID, or TEST frame has cleared the transmitter, its buffer may be released. HD64541 posts status TAUF to notify the external microprocessor of this.

Global Address: A global address can be assigned to UI, XID, and TEST frames by setting G=1.

4.3.3 Receiving Frames that Contain I-Fields

The procedures specified here apply to frames that may carry I-fields, regardless of whether such a frame actually carries one or not in a particular case. Frames in which an I-field is not permitted are not explicitly made available to the external microprocessor.

Receive procedures for I-fields use a table (RBIT) containing some configurable number (NRBI) of input data buffer descriptors (RBIs) that specify the address and size of receive data buffers (RDBs). These memory locations are prepared by the external microprocessor for use by the HD64541. Figure 4-6 shows the structure.

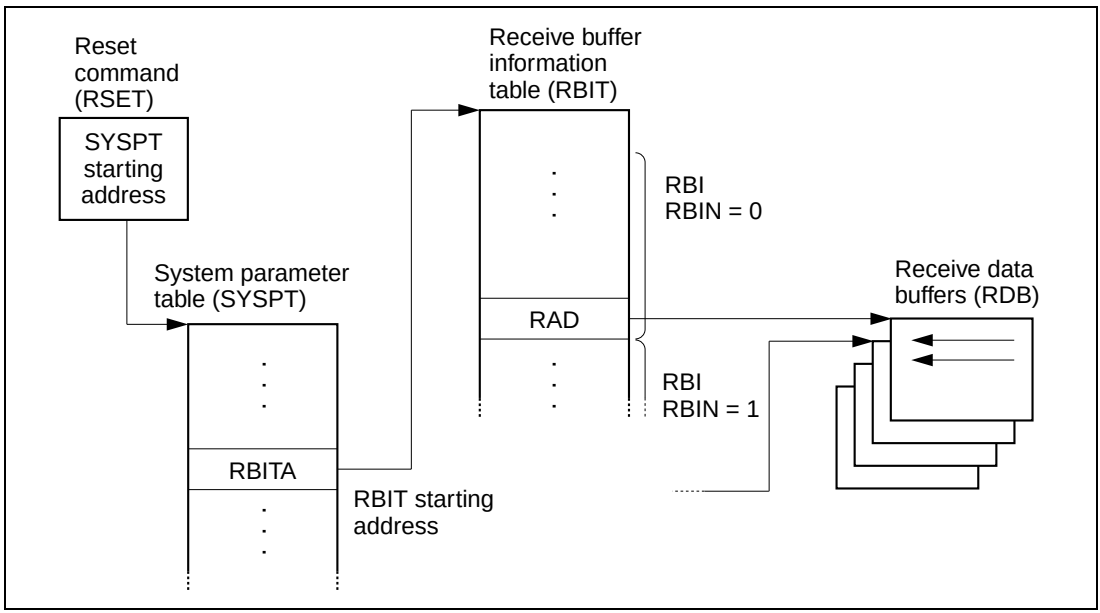


Figure 4-6 (a) Relation between Reception Tables

Note that only one RBIT exists for the HD64541. All I-frames, UI frames, XID frames, and TEST frames are received through the one RBIT. This means that the external microprocessor has to sort the frames by type after they have been received.

Preparation of Receive Data Buffers: The external microprocessor allocates empty receive data buffers (RDBs) and loads their addresses and sizes into receive data buffer descriptors (RBIs). A flag (BS) in each RBI indicates to the HD64541 whether the RBI describes an empty buffer. The flag is toggled when the associated buffer is filled by the HD64541. The RBIT is a table containing some configurable number of RBIs.

Index RBIN in the RBIT specifies the next RBI that the HD64541 will examine when looking for an empty buffer to hold an incoming I-field. The HD64541 increments RBIN as it fills each buffer, so that the RBIs are used sequentially from the lowest number. RBIN is initialized to 0 on a transition from offline to online mode.

After the last RBI in the RBIT has been used, the HD64541 cycles back to the RBI in RBIN = 0. The buffer status bit prevents a buffer from being reused before the external microprocessor has unloaded it.

Frame Receive Operation: When a valid frame containing an I-field is received, the HD64541 locates the next empty receive data buffer and fills it by DMA. Header information (frame type, P/F) is written into octets 0 to 4 of the RBI when the frame has been completely received. FREC status is posted once per frame to notify the external microprocessor (see figure 4-6 (b)).

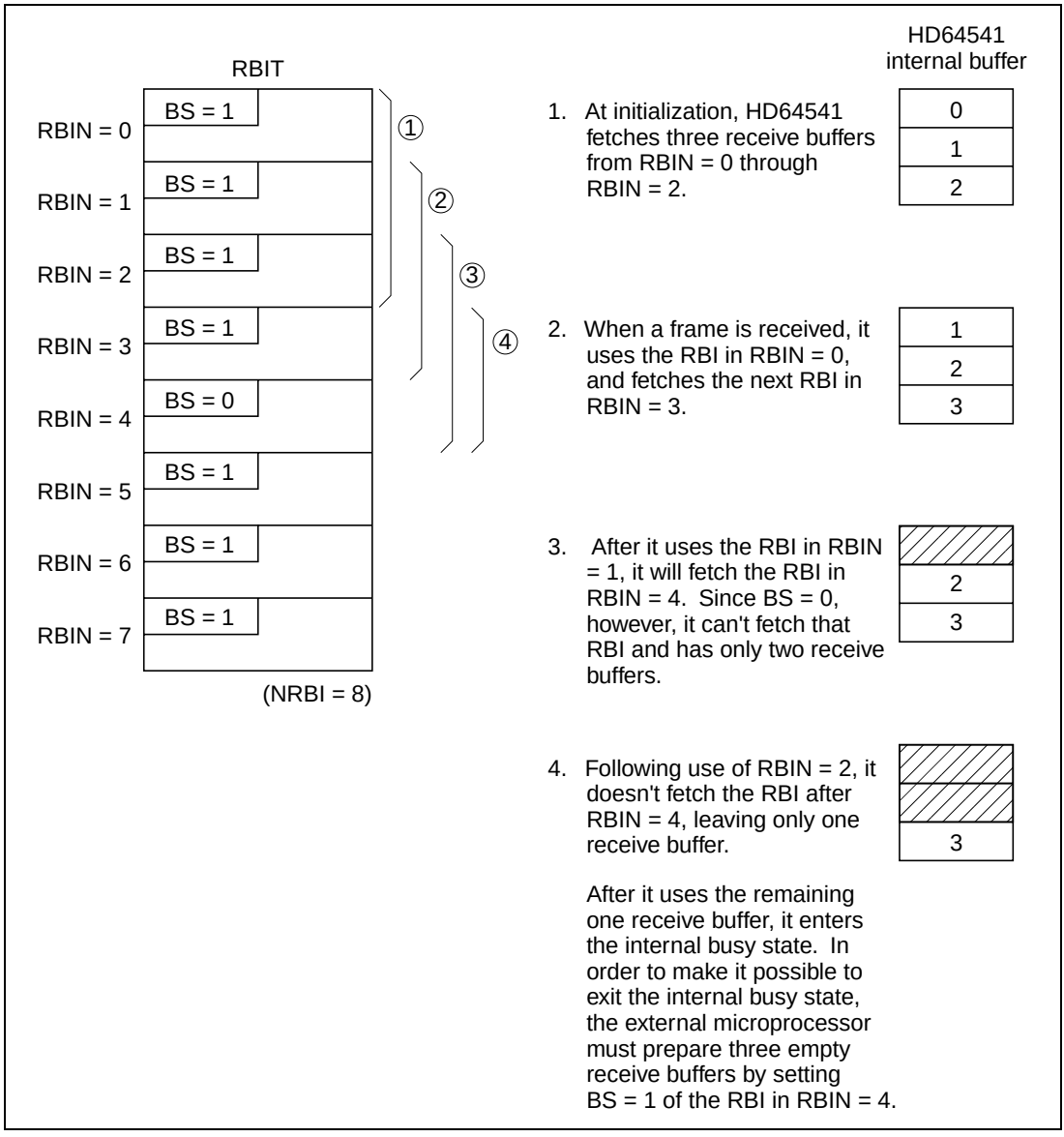


Figure 4-6 (b) Example to Fetch the Receive Buffer

If the received frame does not fit into a single buffer, data chaining is invoked. The HD64541 automatically steps to the next RBI and continues filling the new buffer. Data chaining can continue up to the maximum I-field size permitted or until no more buffers are available. For data chained frames, header information is written into the RBI of the starting buffer only. Successive RBIs contain only BS and CD indicators. FREC status is posted once for the entire chain (see figure 6-4 (c)).

If the received frame has a bad FCS, the buffers are reused and RBIN is not updated.

If the HD64541 receives any I-, UI, XID, or TEST frame whose I-field length is 0 byte, it will normally proceed by using a single receive data buffer (RDB).

When No Empty Receive Data Buffer is Available: If the HD64541 cannot locate an empty receive data buffer when an I-field is received, it is automatically placed in busy state. The HD64541 sends RNR to notify the remote of its inability to receive and post an internal busy interrupt to the external microprocessor (ISR4 = 1).

The HD64541's internal buffer handling mechanism requires at least three empty receive buffers to avoid an internal busy condition. During the internal busy condition, receipt of an I-, UI, XID, or TEST frame is processed as follows:

1. If receive buffer length ≥ I-field length of received frame
   a. The I-frame is discarded in accordance with protocol (See note). If the I-field length of the received frame is longer than N1B, N1 error occurs.
   b. UI, XID or TEST frame will be received normally. However, if the I-field length of the received frame is longer than N1B, N1 error occurs.
2. If receive buffer length < I-field length of received frame
   I-, UI, XID, or TEST frames are discarded and ISR3 (receive buffer overflow) is set. However, if receive buffer length is equal to or longer than N1B, N1 error occurs and ISR3 is not set.

Note: If an I-frame is received when the HD64541 is not busy but only one receive buffer is available, it is placed in busy state after the receive buffer is used up; consequently, it receives the I-frame correctly.

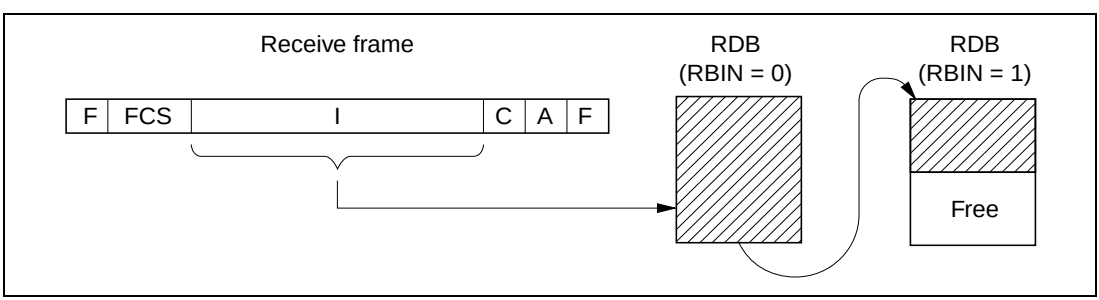


Figure 4-6 (c) Receive Buffer Chain

4.3.4 Transmitting and Receiving I-Frames

Transmitting I-Frames: On reception of a valid DDR1 or DDR2 command from the external microprocessor, the HD64541 queues the specified number of I-frames (FN) for transmission. It immediately posts normal command completion with status CMSR0-CMSR2 = 000.

It actually transmits the I-frames in queue sequence as the flow control state allows. Frames that have been queued earlier but not yet transmitted go first. If the transmit window has closed, the remote station has signaled RNR busy, or transmitter timer recovery or REJ procedures are in progress, the new I-frames are held pending. As each frame comes up for transmission, the current values of the state variables V(S) and V(R) are assigned as the outgoing frame's N(S) and N(R), respectively. Timer T1 is started or restarted as each frame is sent.

As acknowledgements are received from the remote station, state variable V(A) is updated to the latest N(R) received and timer T1 restarted. T1 stops when no more unacknowledged transmitted frames are outstanding on the logical link. The HD64541 conveys the acknowledgements to the external microprocessor as they come in by posting ACIF status. Each ACIF specifies an index value ASIIN that identifies the SII transmit buffer descriptor corresponding to the last frame acknowledged. See figure C-7 of appendix C.

If FN (number of I-frames) is set to value greater than or equal to 2 and either I-frame transmission command DDR1 or DDR2 is issued, or FN number of I-frames can be continuously sent. Here, the interval between frames is set with bit 4 of OMODE in SYSPT.

Receiving I-Frames: When a valid I-frame is received from the remote station, the HD64541 writes its I-field into the current receive data buffer (RDB). The current RDB is the one whose descriptor (RBI) is identified by the index RBIN in the RBIT table. State variable V(R) is incremented by one, and FREC status is posted to notify the external microprocessor of the RBI/RDB that now contains a newly received I-frame.

If the HD64541 is in a local station busy state, the received frame is discarded and nothing is reported to the external microprocessor.

The HD64541 sends a response to the remote station as follows:

1. When P bit is set to 1: If the local station is not in a busy state, it sends an RR response with the F bit set to 1. If it is in a busy state, it sends an RNR response with the F bit set to 1.
2. When P bit is set to 0: If no I-frame is available for transmission, the local station transmits an RR response with the F bit set to 0 after T2 period. If an I-frame is available for transmission, the local station transmits the I-frame with the value of N(R) set to the current value of V(R). If the local station is in a busy state, it transmits an RNR response with the F bit set to 0.

Simultaneous Transmission and Reception of I-Frames: In each direction of transmission, I-frames carry an N(R) that acknowledges reception of I-frames in the opposite direction. See figure C-8 of appendix C. Accordingly, the HD64541 may post ACIF status in addition to FREC on reception of an I-frame.

ACIF is posted only on I-frames that acknowledge previously unacknowledged frames.

4.3.5 Receiving REJ Frames

On reception of a valid REJ supervisory frame from the remote station, the HD64541 sets its state variables V(S) and V(A) to the N(R) value carried in the REJ. It stops timer T1, and retransmits all outstanding I-frames starting with the one identified by the received N(R). See figure C-9 of appendix C.

Outstanding I-frames with N(S) less than the received N(R) are considered acknowledged and ACIF is posted to the external microprocessor.

4.3.6 T1 Runout

Timer T1 limits the amount of time the remote station is allowed in returning an acknowledgement for an I-frame sent to it. T1 is started (or restarted) by the transmitting station as each I-frame is transmitted, and stopped when all outstanding frames have been acknowledged.

If T1 expires, the HD64541 increments its retransmission counter N2, restarts T1, and transmits an RR (P = 1) command to solicit a response. RR (P = 1) is retransmitted on every T1 expiration until either the retransmission count has reached the maximum value specified in SYSPT or when a valid supervisory response frame with F = 1 is received.

In X.25 and X.75 mode if N2 reaches the maximum value without receiving the required response, SRC2 and LRST status are posted to the external microprocessor and an attempt is made to reestablish the logical link by sending SABM/SABME (P = 1). See figure C-6 of appendix C.

The timer recovery condition is cleared when a valid supervisory frame is received from the remote station with F = 1. The N(R) carried in that frame identifies the last I-frame that the remote station correctly received. If that N(R) is less than the HD64541's V(S), it means that frames were lost and need to be retransmitted. In this case, the HD64541 sets its V(S) to the received N(R).

In T.90 mode if N2 reaches the maximum value SRC2 status is posted to the external microprocessor and the HD64541 releases the logical link.

4.3.7 T3 Runout

When the HD64541 is in on-line mode and the receive data changes to idle pattern from flag sequence, timer T3 starts. If a T3 runout then occurs, the HD64541 reports idle detection status (IDET) to the external microprocessor. However, if the receive data returns to flag sequence before T3 runs out, the HD64541 stops timer T3 without notifying the external microprocessor.

Figure 4-7 shows the relation between the set operating mode command, receive data state, and status to be reported.

The HD64541 processes a command issued from the external microprocessor in the same manner as a flag sequence even if the receive data is the idle pattern.

The T3 timer can be also used in transparent mode. The value of T3 is set by T3 of SYSPT and the timestep of T3 is set by bit 1 of PMODE in SYSPT.

4.4 Link Reset

The HD64541 automatically reestablishes the data link in any of the following cases (after reestablishing the data link, it notifies the external microprocessor of reset link status (LRST)):

a. When SABM/SABME is sent in return for receiving FRMR
b. When SABM/SABME is sent due to an N2 number of T1 runouts (in X.25 or X.75 mode)
c. When SABM/SABME is sent in return for receiving an unexpected supervisory frame with F = 1 (in X.25 mode)
d. When SABM/SABME is sent in return for receiving an unexpected UA or DM response (in X.25 mode)

Figure C-6 (a) and C-10 (a) in appendix C shows examples of b, c, and d above, respectively.

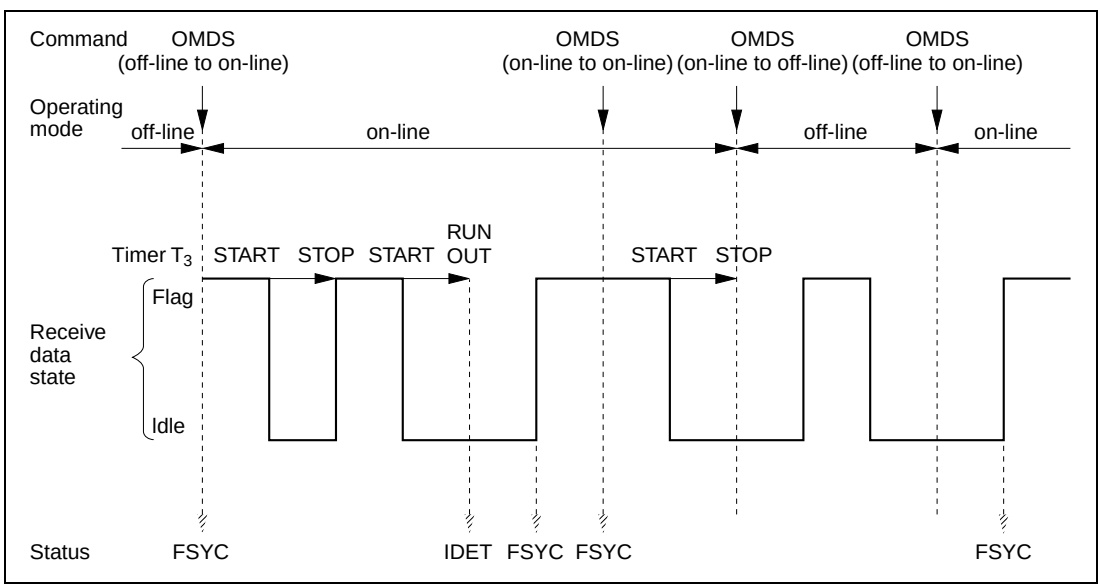


Figure 4-7 Relation between OMDS Command, Receive Data State, and Report Status

4.5 Exception Condition Handling

4.5.1 N(S) Sequence Error

When the HD64541 receives an I-frame that is out of sequence but otherwise valid from the remote station, its I-field is discarded and a REJ frame sent back to solicit the expected I-frame. The I-fields of any subsequent I-frames are similarly discarded until the expected one is received. The N(R) field carried in the out-of-sequence frame is considered a valid acknowledgement, however, and is not discarded. An I-frame is out of sequence when its N(S) does not match the receiving station's V(R) state variable. The REJ frame sent back carries N(R) = V(R). The remote station is obliged to retransmit all outstanding I-frames beginning with the one identified by the N(R) value in the REJ. See figure C-11 of appendix C.

4.5.2 N(R) Sequence Error

When the HD64541 receives an N(R) value from the remote station that acknowledges more I-frames than have been transmitted and are outstanding, the HD64541 posts the remote station system recovery request (YRCV) status to the external microprocessor and transmits FRMR. The N(R) received must be greater than or equal to state variable V(A) and less than or equal to state variable V(S) to be valid. The comparison is done in the specified modulo (8 or 128). See figure C-12 of appendix C.

4.5.3 Busy States

Local Station Busy State: The HD64541 may enter the local station busy state either as a result of its internal protocol processing or on command from the external microprocessor.

Command SSBY sets busy the logical link. Busy state set by SSBY can be released only through RSBY. See figure C-13 of appendix C.

When the HD64541 enters the busy state through internal protocol processing, it notifies the external microprocessor through interrupt ISR4 = 1. When it exits busy state, it posts interrupt ISR4 = 0.

When the HD64541 becomes busy by whatever means, it transmits RNR to the remote station and transmits RR when the busy condition is released.

During busy, frames from the remote station are processed as follows:

1. The I-fields of all I-frames are discarded
2. RNR (F = 1) is transmitted in response to an I-frame with P = 1
3. All supervisory responses and commands with P = 0 are handled normally
4. RNR (F = 1) is transmitted in response to a supervisory command with P = 1

In all four cases, normal acknowledgement processing procedures apply to the received N(R).

Remote Station Busy State: When the HD64541 receives a valid RNR frame from the remote station, it enters the remote station busy state for the logical link and reports it to the external microprocessor by posting SRBY status. In the remote station busy state, the HD64541 does not transmit or retransmit I-frames. It posts RRBY when the remote station exits the busy state and sends a notifying RR frame.

The HD64541 polls the remote station at intervals of T1 to make sure that the remote station reports any change in busy status. As soon as RNR is received, the HD64541 starts timer T1. On the expiration of T1, it transmits RR (P = 1) to demand either RR (F = 1) or RNR (F = 1). See figure C-14 of appendix C.

In T.90 mode, on reception of the RNR (F = 1) while in the timer recovery state, HD64541 remains in this state. If T1 runouts have repeated N2 times and the remote station has not released the remote station busy state, HD64541 posts system recovery request SRC2 and releases the logical link. (see figure C-14 (b) in appendix C)

4.5.4 Receipt of Unexpected Frames

Unexpected frames are defined as follows.

a) Supervisory frames (F = 1) in timer recovery state and supervisory frames which are not responses to command frames (P = 1)
b) UA and DM response frames which should not be sent by the remote station
   (1) Receipt of unexpected frames in X.25 mode

   HD64541 sends an SABM/SABME frame to the remote station and posts LRST status to the host processor. (See figure C-10 (a) in appendix C.)
   (2) Receipt of unexpected frame in X.75 mode

   HD64541 sends an FRMR frame to the remote station and posts YRCV status to the host processor. (See figure C-10 (b) in appendix C.)
   (3) Receipt of unexpected frame in T.90 mode

   HD64541 ignores the frame and discards it. HD64541 counts it as a process error in the statistical information logging table. (See figure C-10(c) in appendix C.)

4.5.5 Receipt of I-frame with Invalid N(S)

N(S) is invalid if it is equal to the receive state variable V(R), and is also equal to the last N(R) transmitted to the remote station plus K, the maximum outstanding I-frame number.

(1) On receipt of frame with invalid N(S) in X.25 mode

Since an invalid N(S) is not defined in the CCITT X.25 recommendation, HD64541 receives the I-frame with an invalid N(S) as a correct frame by acknowledging N(S) as equal to V(R). (See figure C-15 (a) in appendix C.)

(2) On receipt of frame with invalid N(S) in X.75 mode

HD64541 discards the I-frame and transmits an FRMR frame to the remote station and posts YRCV status to the host processor. (See figure C-15 (b) in appendix C.)

(3) On receipt of frame with invalid N(S) in T.90 mode

HD64541 discards the information field of this I-frame and transmits an REJ frame to the remote station and promotes the recovery from this state. (See figure C-15 (c) in appendix C.)

4.6 Transparent Mode

This section describes how to use transparent mode.

Transparent Mode:

- Transmit: Data prepared by the external microprocessor is grouped with flags and FCS and then transmitted.
- Receive: Bit sequence between a flag and FCS is received as data.

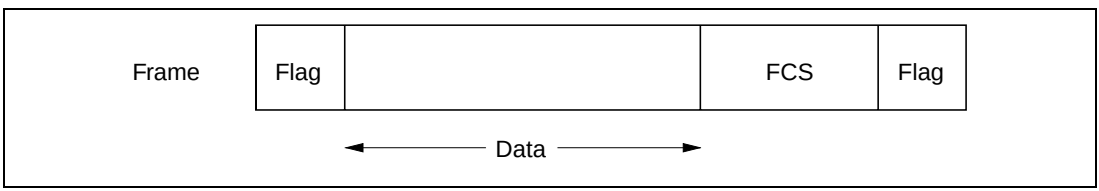


Figure 4-8 Frame in Transparent Mode

Tables

- SYSPT

Table 4-4 shows bytes used in transparent mode. Others are set to 0.

Table 4-4 SYSPT Used in Transparent Mode

Name	Byte	Bit	Description
PMODE	0	3	Set as in normal mode.
		7	Set to 1 (transparent mode)
OMODE	1	0	Set to 1
VADD	2	0 to 7	Set as in normal mode
TDIV	3	0 to 3	
T 3	12	0 to 7	
NRBI	13	0 to 7	
NSI	15	0 to 7	
S I I TA	25,26,27	0 to 7	Set as in normal mode
RB I TA	29,30,31	0 to 7	

- SIIT

  Data is set in the table the same as in normal mode. 0 should not be set for SBC.
- RBIT

  The RBIT used in transparent mode is shown in table 4-5.

Table 4-5 RBIT Used in Transparent Mode

Table	Byte	Bit	Description
RBC	2	0 to 5	Number of bytes in data section of received frame
	3	0 to 7	
BS	4	7	Buffer status used as in normal mode
CD	4	6	Chained data used as in normal mode
TYP	4	0 to 2	0 0 0
RBS	6	0 to 4	Size of receive data buffer
	7	0 to 7	
RAD	9 to 11	0 to 7	Starting address of RDB

- LOGT

  Table 4-6 shows items to be counted.

Table 4-6 LOGT Used in Transparent Mode

No.	Description
0	FCS error
1	Short frame
2	Residual bit frame
3	Abort frame
4	Overrun error
5	Idle
6	Underrun error

Command: Ten types of commands used in transparent mode are shown in table 4-7.

Table 4-7 Commands Used in Transparent Mode

Command	Operation
STAC,RSET,OMDS CPOL,MPIS,DSPT DERC,SUTD,RETD	Same as in normal mode
DDR 2	Frame transmission

Eight types of commands shown below cannot be used in transparent mode; a command format error will occur if their use is attempted.

Inhibited commands in transparent mode: DDR1, MUDR, DESR, DRLR
SSBY, RSBY, DESW, RESR

Status: Five types of status are used in transparent mode: PITL, TAIF, FREC, IDET, and FSYC. Among these, TAIF is valid only in transparent mode. The functions of PITL, FREC, IDET, and FSYC others are the same as in normal mode.

Typical Sequence Example: Figure 4-9 shows a typical sequence diagram.

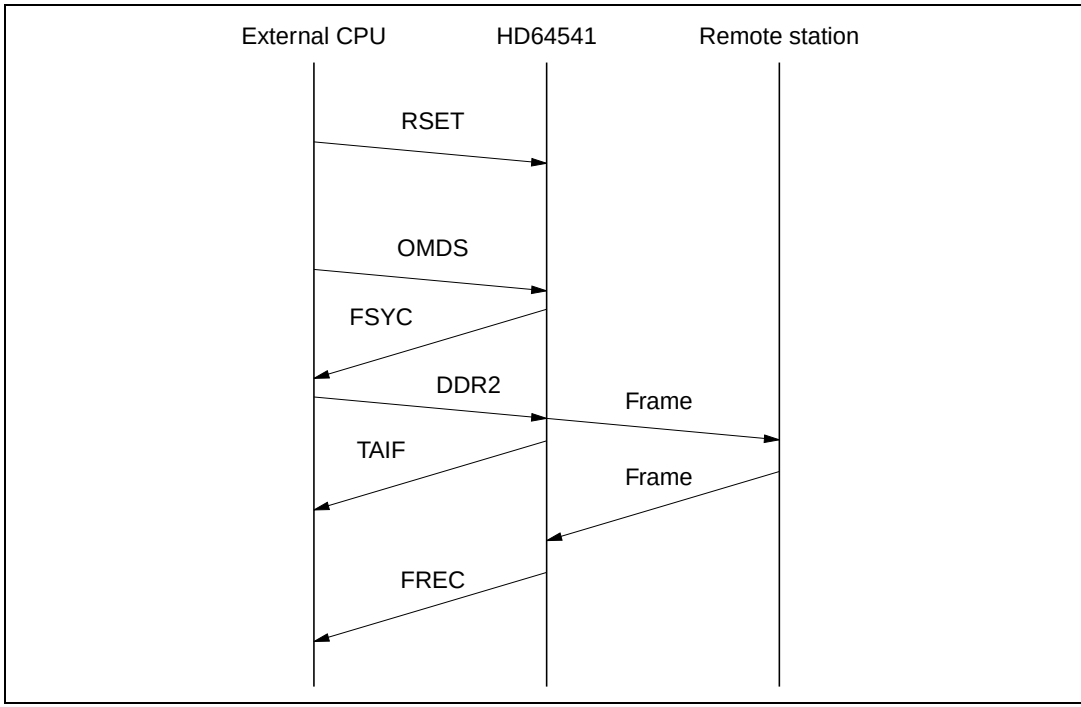


Figure 4-9 Typical Sequence Diagram in Transparent Mode

4.7 Protocol mode (T.90, X.75, X.25)

Protocol mode is selected to T.90, X.75, or X.25 mode by bits 1 to 3 of OMODE on SYSPT.

The difference between protocol operations for each mode is shown in table 4-8.

Table 4-8 Protocol Mode

No	Event	X.25 layer 2	X.75 layer 2	T.90 layer 2	Reference
1	Receive unexpected S-frame (F = 1)	SABM/SABME transmit	FRMR transmit	Ignore (Procedure error)	4.5.4 Figure C-10
	Receive unexpected UA, DM response	SABM/SABME transmit	FRMR transmit	Ignore (Procedure error)	
	Receive I-frame of invalid N(S)	Normal receive	FRMR transmit	REJ transmit	4.5.5 Figure C-15
2	Receive DM response to request link-set	Link-setting	Ignore (Procedure error)		4.2.1 (3) Figure C-3
3	N2-times T1-timeout	Start link-reset		Enter the disconnected phase	4.2.4 4.3.6 Figure C-6
4	Receive RNR (F = 1) in timer recovery condition	End timer recovery condition		Remain timer recovery condition	4.5.3 (2) Figure C-14

4.8 Fast Transfer Speed

The maximum transfer speed of HD64541 is 5 Mbps. However, if the line transmission load to HD64541 is too heavy, such as by receiving short frames continuously, or for reasons due to system architecture, HD64541 will not cover its protocol process.

The following cases are described.

(1) Continuous frame reception
(2) Continuous frame transmission
(3) Chain of data buffer
(4) Data transfer by DMA from external memory

4.8.1 Continuous Frame Reception

When HD64541 receives one frame, it analyzes the frame type and takes appropriate action for state transfer and protocol operation. If during frame processing another frame is on the line, the HD64541 cannot receive this frame correctly and thus ignores it. For normal continuous receipt of frames, HD64541 needs at least approximately 470 µs (see figure 4-9) for one frame period, and approximately 140 µs (see figure 4-9) for flag intervals.

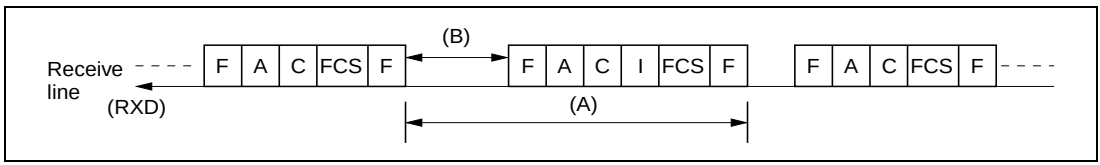


Figure 4-10 Continuous Frame Reception

4.8.2 Continuous Frame Transmission

When HD64541 receives an I-frame transmission command (DDR1, DDR2) with FN ≥= 2, HD64541 can transmit I-frames continuously.

The minimum interval time between a transmitted frame is approximately 80 µs in normal protocol mode and approximately 60 µs in transparent mode.

If the interval of a received flag of the remote station is longer than the interval of a transmitted flag, an error may occur in the remote station. (For example, between two HD64541s, the interval time for reception is approximately 140 µs and the interval for transmission is approximately 80 µs.)

To avoid this situation, the user should select the minimum interval transmit flag time as approximately 80 µs or approximately 300 µs by the 4 bits of OMODE in SYSPT.

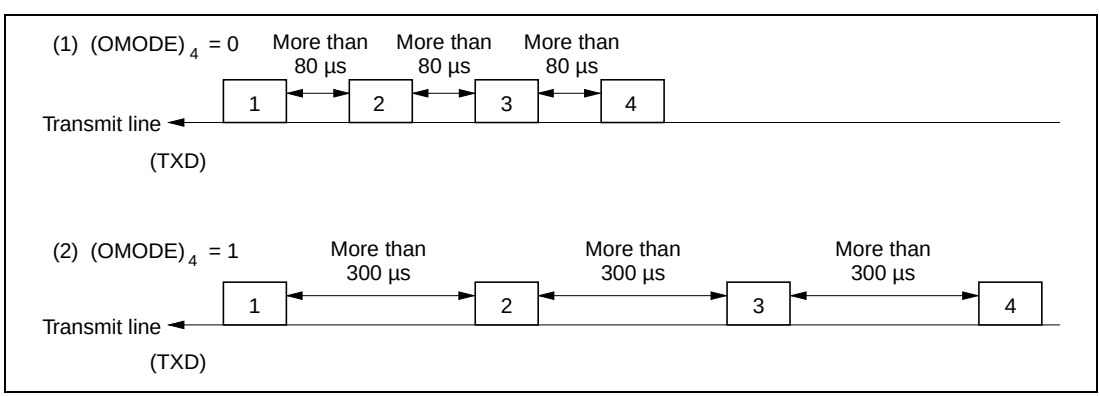


Figure 4-11 Continuous Frame Transmission

4.8.3 Chain of Data Buffers

Chain operation of data buffers is used to store the I-field of one frame in multiple receive data buffers, or to gather the data stored in multiple transmission data buffers and send them in one frame.

When the HD64541 is chaining the data buffer, it prepares the next data buffer after loading to one buffer, which takes about 120 µs. HD64541 has 20 bytes of FIFO for reception and transmission. When the line speed becomes high, if the frames in FIFO become full before the HD64541 can finish the chaining process, a transmission underrun error or receive overrun error will occur. (These errors indicate that the FIFO is empty during transmission or that it is full during transmission.)

Also, the capacity of a data buffer is too small, a buffer overflow error or an internal busy state may occur.

Set the data buffer size as shown in table 4-9 when data chaining is needed.

Table 4-9 Line Speed and Data Buffer Size

Line speed	5 Mbps	4 Mbps	2 Mbps
Data buffer size	More than 75 bytes	More than 60 bytes	More than 30 bytes

4.8.4 External Memory and Data DMA Transfer

The DMA controller in HD64541 needs 4 cycles to read one word and 5 cycles to write one. This cycle time is constant, so the occupation rate of the host bus must become higher when the line speed is high. When HD64541 transmits and receives I-frames, it requests bus authority ($\overline{\text{BREQ}}$ = low) to transfer data by DMA from external memory. If for such reason as the MPU does not get bus authority or if there is some delay, a receive overrun error or transmit underrun error may occur in the HD64541.

Figure 4-11 shows the relationship of the host-bus operation rate and DMA transfer capability.

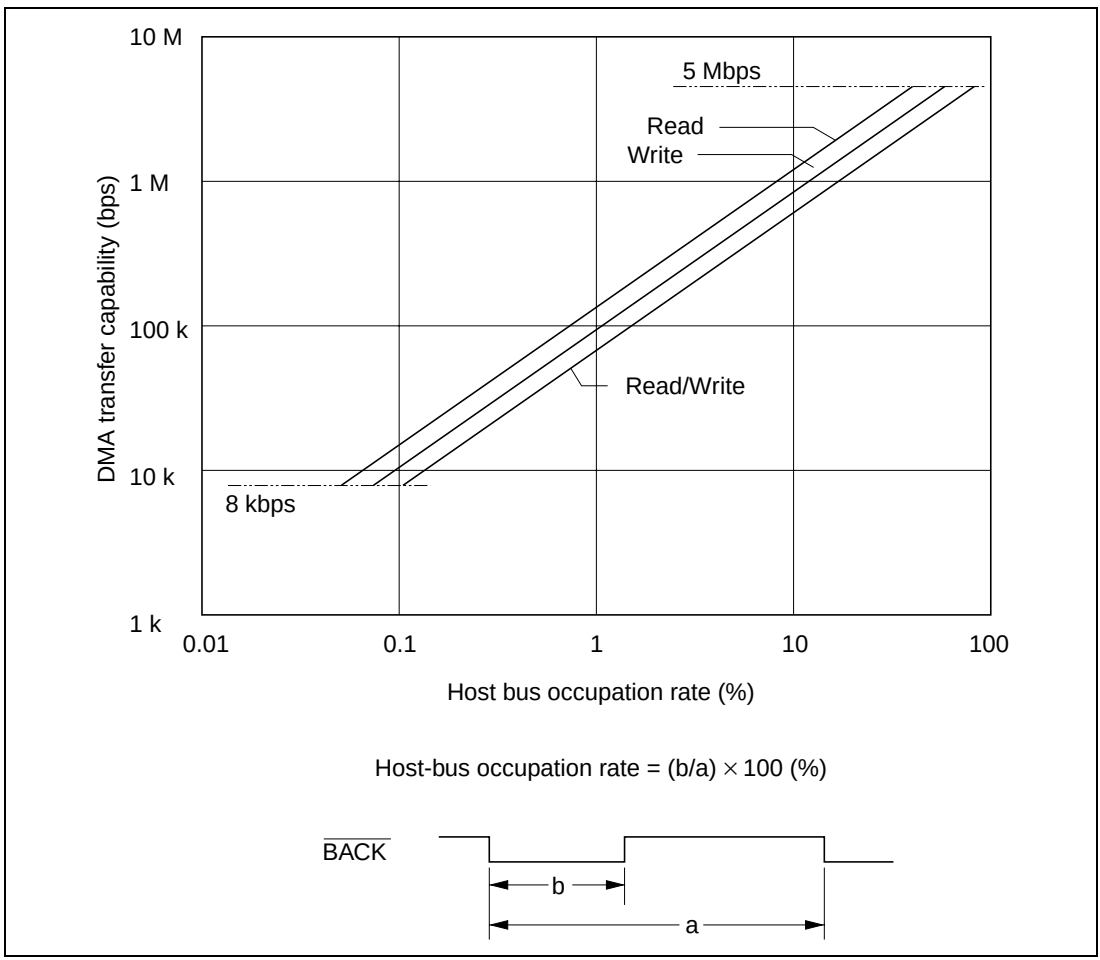


Figure 4-12 Dependency of Host-Bus Occupation Rate on DMA Transfer Capability

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC} (Note 2)	7.0	V
Input voltage	V_{in} (Note 2)	V_{SS} – 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.
2. With respect to V_{SS} (system ground).

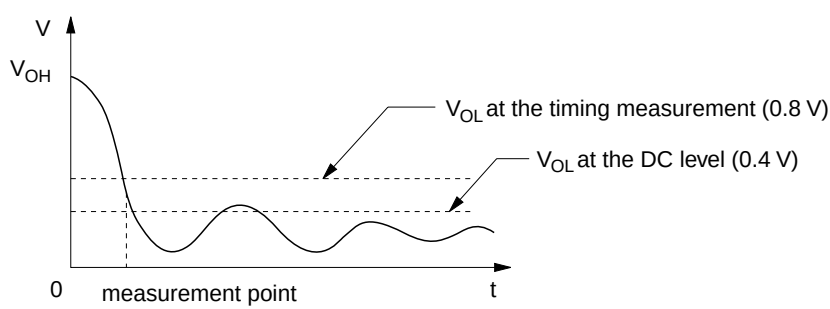
5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC} (Note)	4.75	5.0	5.25	V
Input low level voltage	V_{IL} (Note)	–0.3	—	0.8	V
Input high level voltage	V_{IH} (Note)	2.0	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Note: With respect to V_{SS} (system ground).

Timing measurement: The timing measurement point for the output low level is defined at 0.8 V throughout this specification. The output low level at stable condition (DC characteristics) is defined at 0.4 V.



V_{OL} Reference at Timing Measurement

5.3 Electrical Characteristics

5.3.1 DC Electrical Characteristics

Table 5-3 DC Electrical Characteristics

(V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol		Min	Typ*	Max	Unit	Condition
Input high level voltage	V_{IH}	CLK (clock)	2.4	—	V_{CC}	V	
		Others	2.0	—	V_{CC}	V	
Input low level voltage	V_{IL}		–0.3	—	0.8	V	
Input leakage current	I_{IN}		—	—	2.5	µA	
Output high level voltage	V_{OH}		2.4	—	—	V	I_{OH} = –200 µA
Output low level voltage	V_{OL}		—	—	0.4	V	I_{OL} = 1.6 mA
Output leakage current	I_{LOH}		—	—	10	µA	
Pin capacitance	C_p		—	—	15	pF	V_{in} = 0 V F = 1 MHz Ta = 25°C
Current Consumption	I_{CC}		—	26	50	mA	

* Ta = 25°C, V_{CC} = 5.0 V

5.3.2 AC Electrical Characteristics

Table 5-4 (a) AC Electrical Characteristics

(V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to +70°C, unless otherwise noted)

Normal mode

No.	Parameter	Symbol	Min	Max	Unit
	Operating frequency	f	2	6.25	MHz
1	Clock cycle time	t_{cyc}	160	500	ns
2	Clock width low	t_{CL}	75	250	ns
3	Clock width high	t_{CH}	75	250	ns
4	Clock fall time	t_{cf}	—	10	ns
5	Clock rise time	t_{cr}	—	10	ns
6	Asynchronous input set-up time	t_{ASI}	25	—	ns
7	Set-up time from $\overline{AS}$	t_{ASS}	0	—	ns
8	Clock low to $\overline{READY}$ low	t_{CLR}	—	120	ns
9	Clock high to $\overline{DIN}$, $\overline{DBEN}$, $\overline{A/D}$ valid	t_{CHD}	—	250	ns
10	Clock low to $\overline{DBEN}$ low	t_{CLD}	—	120	ns
11	$\overline{READY}$ low to $\overline{DS}$ high	t_{RLD}	0.5	—	clocks
12	$\overline{AS}$ high to address invalid	t_{AHI}	0	—	ns
13	$\overline{DS}$ high to $\overline{READY}$ high impedance	t_{DHDH}	—	140	ns
14	$\overline{DS}$ high to $\overline{DBEN}$ high impedance	t_{DHBH}	—	140	ns
15	$\overline{DS}$ high to data invalid	t_{DHDI}	0	—	ns
16	$\overline{DS}$ high to $\overline{READY}$ high impedance	t_{DHRH}	—	140	ns
16A	$\overline{READY}$ high to high impedance	t_{RHHI}	10	—	ns
17	Clock high to $\overline{DIN}$ low	t_{CHDL}	—	140	ns
18	Data in to $\overline{DBEN}$ low	t_{DIBL}	25	—	ns
19	Clock low to $\overline{DBEN}$ high	t_{CLBH}	—	100	ns
20	Clock high to $\overline{DIN}$ high	t_{CHDH}	—	140	ns
21	$\overline{READY}$ low to A/D invalid	t_{RLAI}	1.0	—	clocks
22	Clock high to $\overline{BREQ}$ low	t_{CHBL}	—	150	ns
23	$\overline{BACK}$ set-up time from CLK	t_{BSC}	30	—	ns
24	$\overline{BACK}$ low to $\overline{AIN}$ low	t_{BLAL}	2.5	3.5	clocks
25	Clock high to $\overline{BREQ}$ high	t_{CHBH}	—	150	ns
26	Clock high to $\overline{AIN}$ high	t_{CHAH}	—	90	ns
27	Address valid to $\overline{AS}$ low	t_{AVAL}	40	—	ns

Table 5-4 (a) AC Electrical Characteristics (cont)

Normal mode (cont)

No.	Parameter	Symbol	Min	Max	Unit
28	$\overline{ABEN}$ high to address valid	t_{AHAI}	40	—	ns
28A	Address valid to ABEN High	t_{AVEH}	25	—	ns
29	$\overline{READY}$ low to data in	t_{RLDI}	—	150	ns
30	$\overline{DS}$ high to data invalid	t_{DHD}	0	—	ns
31	$\overline{DS}$ high to $\overline{READY}$ high	t_{DHRE}	0	160	ns
32	Data out valid to $\overline{DS}$ low	t_{DVDL}	0	—	ns
33	$\overline{DS}$ high to data invalid	t_{SHDI}	40	—	ns
34	Clock high to address valid	t_{CHAV}	—	250	ns
35	Clock high to $\overline{ABEN}$ low	t_{CHEL}	—	140	ns
36	Clock high to $\overline{DS}$ low	t_{CHSL}	—	150	ns
37	Clock high to $\overline{DIN}$ low	t_{CHNL}	—	150	ns
38	Clock high to $\overline{DIN}$ high	t_{CHNH}	—	140	ns
39	$\overline{DIN}$ low to $\overline{DBEN}$ low	t_{NLBL}	20	—	ns
40	$\overline{DBEN}$ high to $\overline{DIN}$ high	t_{BHNH}	40	—	ns
41	Clock high to S/$\overline{U}$ PF valid	t_{CHPV}	—	150	ns
42	Address valid to R/$\overline{W}$ low	t_{AVWL}	35	—	ns
43	Clock high to R/$\overline{W}$ low	t_{CHWL}	—	150	ns
44	R/$\overline{W}$ low to $\overline{DS}$ low	t_{WLSL}	120	—	ns
45	Clock low to $\overline{DBEN}$ low	t_{CLBL}	—	110	ns
46	Clock low to $\overline{DIN}$ high impedance	t_{CLNI}	—	150	ns
47	Clock low to $\overline{DBEN}$ high impedance	t_{CLBI}	—	140	ns
48	Clock low to , $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	—	100	ns
49	RxD set-up time	t_{RSUT}	20	—	ns
50	RxD hold time	t_{RHT}	20	—	ns
51	RxC cycle time	t_{RCYC}	0.2	125	µs
52	TxC low to TXD valid	t_{TLTV}	—	100	ns
55	TxC cycle time	t_{TCYC}	0.2	125	µs
56	RESET pulse width	t_{RST}	24	—	clocks
57	$\overline{DS}$ high to $\overline{IACK}$ high	t_{DHIH}	0	—	ns
58	Clock high to $\overline{IRQ}$ low	t_{CHRL}	—	140	ns
59	Clock change to $\overline{IRQ}$ high	t_{CCRH}	—	150	ns

Table 5-4 (b) AC Electrical Characteristics

(V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to +70°C, unless otherwise noted)

Double frequency mode

No.	Parameter	Symbol	Min	Max	Unit
	Operating frequency	f	4	12.5	MHz
1	Clock cycle time	t_{CYC}	80	250	ns
2	Clock width low	t_{CL}	35	125	ns
3	Clock width high	t_{CH}	35	125	ns
4	Clock fall time	t_{Cf}	—	5	ns
5	Clock rise time	t_{Cr}	—	5	ns
6	Asynchronous input set-up time	t_{ASI}	25	—	ns
7	Set-up time from $\overline{AS}$	t_{ASS}	0	—	ns
8	Clock low to $\overline{READY}$ low	t_{CLR}	—	120	ns
9	Clock high to $\overline{DIN}$, $\overline{DBEN}$, A/D valid	t_{CHD}	—	250	ns
10	Clock low to $\overline{DBEN}$ low	t_{CLD}	—	120	ns
11	$\overline{READY}$ low to $\overline{DS}$ high	t_{RLD}	1.0	—	clocks
12	$\overline{AS}$ high to address invalid	t_{AHI}	0	—	ns
13	$\overline{DS}$ high to $\overline{DIN}$ high impedance	t_{DHDH}	—	140	ns
14	$\overline{DS}$ high to $\overline{DBEN}$ high impedance	t_{DHBH}	—	140	ns
15	$\overline{DS}$ high to data invalid	t_{DHDI}	0	—	ns
16	$\overline{DS}$ high to $\overline{READY}$ high impedance	t_{DHRH}	—	140	ns
16A	$\overline{READY}$ high to high impedance	t_{RHHI}	10	—	ns
17	Clock high to $\overline{DIN}$ low	t_{CHDL}	—	140	ns
18	Data in to $\overline{DBEN}$ low	t_{DIBL}	25	—	ns
19	Clock low to $\overline{DBEN}$ high	t_{CLBH}	—	100	ns
20	Clock high to $\overline{DIN}$ high	t_{CHDH}	—	140	ns
21	$\overline{READY}$ low to A/D invalid	t_{RLAI}	2.0	—	clocks
22	Clock high to $\overline{BREQ}$ low	t_{CHBL}	—	150	ns
23	$\overline{BACK}$ set up time from CLK	t_{BSC}	30	—	ns
24	$\overline{BACK}$ low to $\overline{AIN}$ low	t_{BLAL}	5.0	7.0	clocks
25	Clock high to $\overline{BREQ}$ high	t_{CHBH}	—	150	ns
26	Clock high to $\overline{AIN}$ high	t_{CHAH}	—	90	ns
27	Address valid to $\overline{AS}$ low	t_{AVAL}	40	—	ns
28	$\overline{ABEN}$ high to address invalid	t_{AHAI}	40	—	ns
28A	Address valid to $\overline{ABEN}$ high	t_{AVEH}	25	—	ns

Table 5-4 (b) AC Electrical Characteristics (cont)

Double frequency mode (cont)

No.	Parameter	Symbol	Min	Max	Unit
29	$\overline{\text{READY}}$ low to data in	t_{RLDI}	—	150	ns
30	$\overline{\text{DS}}$ high to data invalid	t_{DHD}	0	—	ns
31	$\overline{\text{DS}}$ high to $\overline{\text{READY}}$ high	t_{DHRE}	0	160	ns
32	Data out valid to $\overline{\text{DS}}$ low	t_{DVDL}	0	—	ns
33	$\overline{\text{DS}}$ high to data invalid	t_{SHDI}	40	—	ns
34	Clock high to address valid	t_{CHAV}	—	250	ns
35	Clock high to $\overline{\text{ABEN}}$ low	t_{CHEL}	—	140	ns
36	Clock high to $\overline{\text{DS}}$ low	t_{CHSL}	—	150	ns
37	Clock high to $\overline{\text{DIN}}$ low	t_{CHNL}	—	150	ns
38	Clock high to $\overline{\text{DIN}}$ high	t_{CHNH}	—	140	ns
39	$\overline{\text{DIN}}$ low to $\overline{\text{DBEN}}$ low	t_{NLBL}	20	—	ns
40	$\overline{\text{DBEN}}$ high to $\overline{\text{DIN}}$ high	t_{BHNH}	40	—	ns
41	Clock high to S/$\overline{\text{U}}$ PF valid	t_{CHPV}	—	180	ns
42	Address valid to R/$\overline{\text{W}}$ low	t_{AVWL}	30	—	ns
43	Clock high to R/$\overline{\text{W}}$ low	t_{CHWL}	—	150	ns
44	R/$\overline{\text{W}}$ low to $\overline{\text{DS}}$ low	t_{WLSL}	120	—	ns
45	Clock low to $\overline{\text{DBEN}}$ low	t_{CLBL}	—	110	ns
46	Clock low to $\overline{\text{DIN}}$ high impedance	t_{CLNI}	—	150	ns
47	Clock low to $\overline{\text{DBEN}}$ high impedance	t_{CLBI}	—	140	ns
48	Clock low to $\overline{\text{AS}}$ $\overline{\text{DS}}$ high	t_{CLSH}	—	100	ns
49	RxD set up time	t_{RSUT}	20	—	ns
50	RxD hold time	t_{RHT}	20	—	ns
51	RxC cycle time	t_{RCYC}	0.2	125	µs
52	TxC low to TxD valid	t_{TLTV}	—	100	ns
55	TxC cycle time	t_{TCYC}	0.2	125	µs
56	RESET pulse width	t_{RST}	48	—	clocks
57	$\overline{\text{DS}}$ high to $\overline{\text{IACK}}$ high	t_{DHIH}	0	—	ns
58	Clock high to $\overline{\text{IRQ}}$ low	t_{CHRL}	—	140	ns
59	Clock change to $\overline{\text{IRQ}}$ high	t_{CCRH}	—	150	ns

5.4 Timing Diagrams

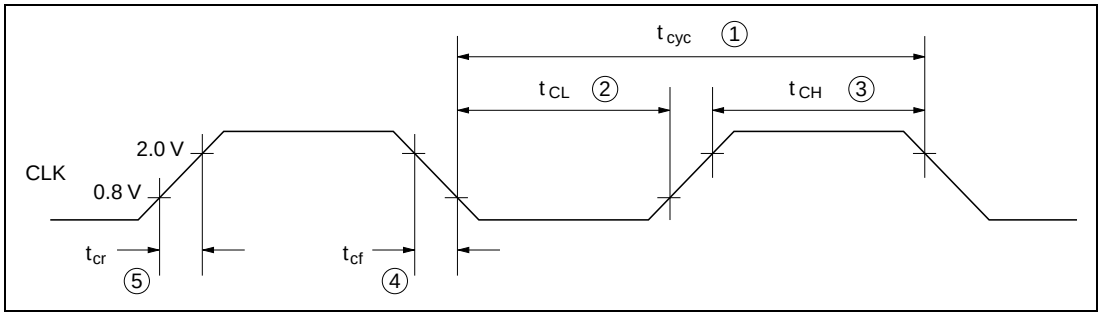


Figure 5-1 Input Clock Waveform

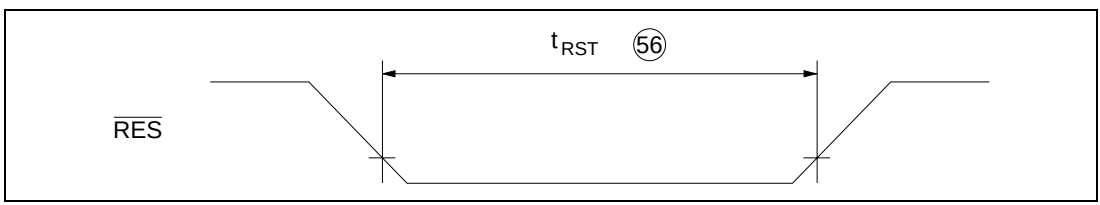


Figure 5-2 Reset Input Timing

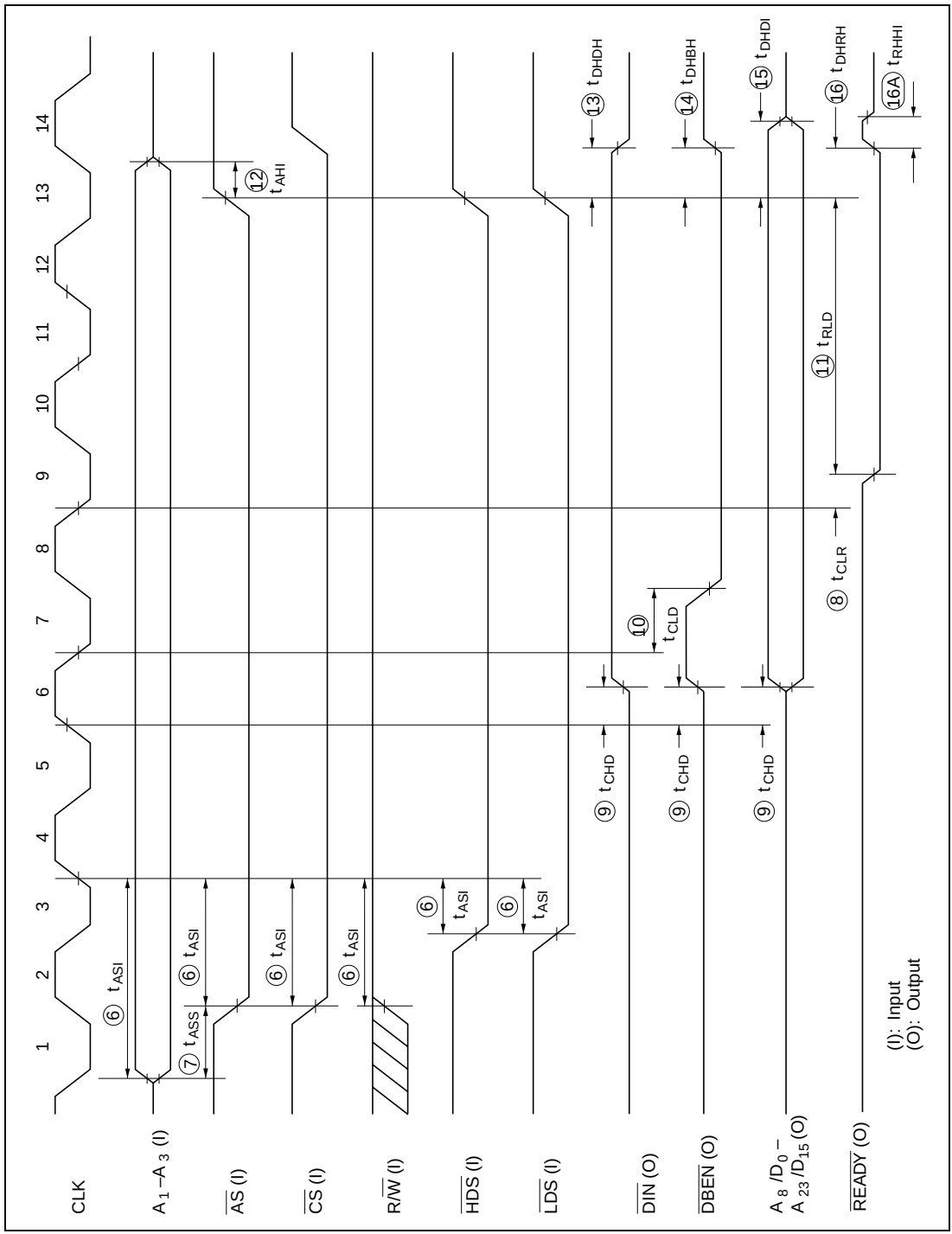


Figure 5-3 Host CPU Read Cycle

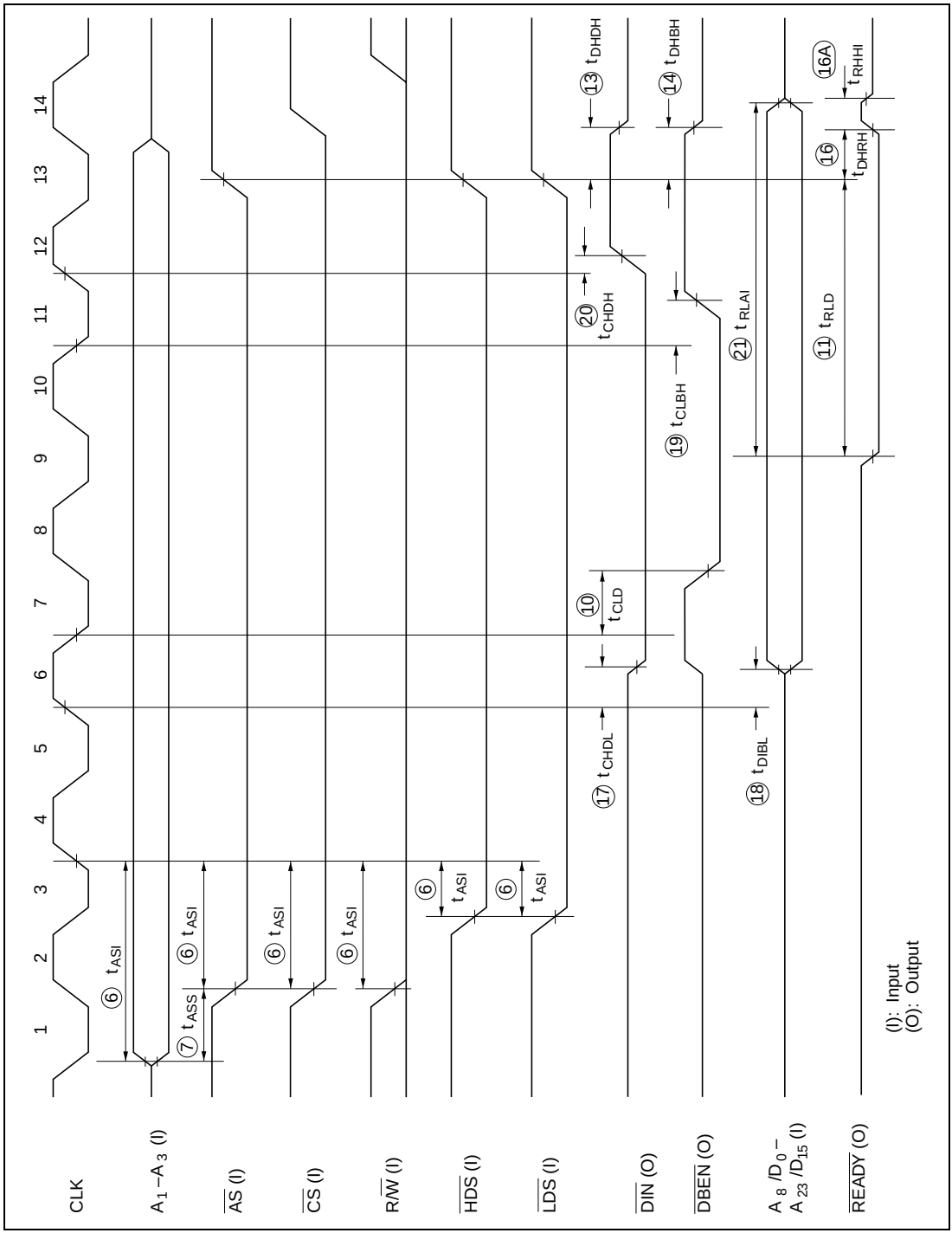


Figure 5-4 Host CPU Write Cycle

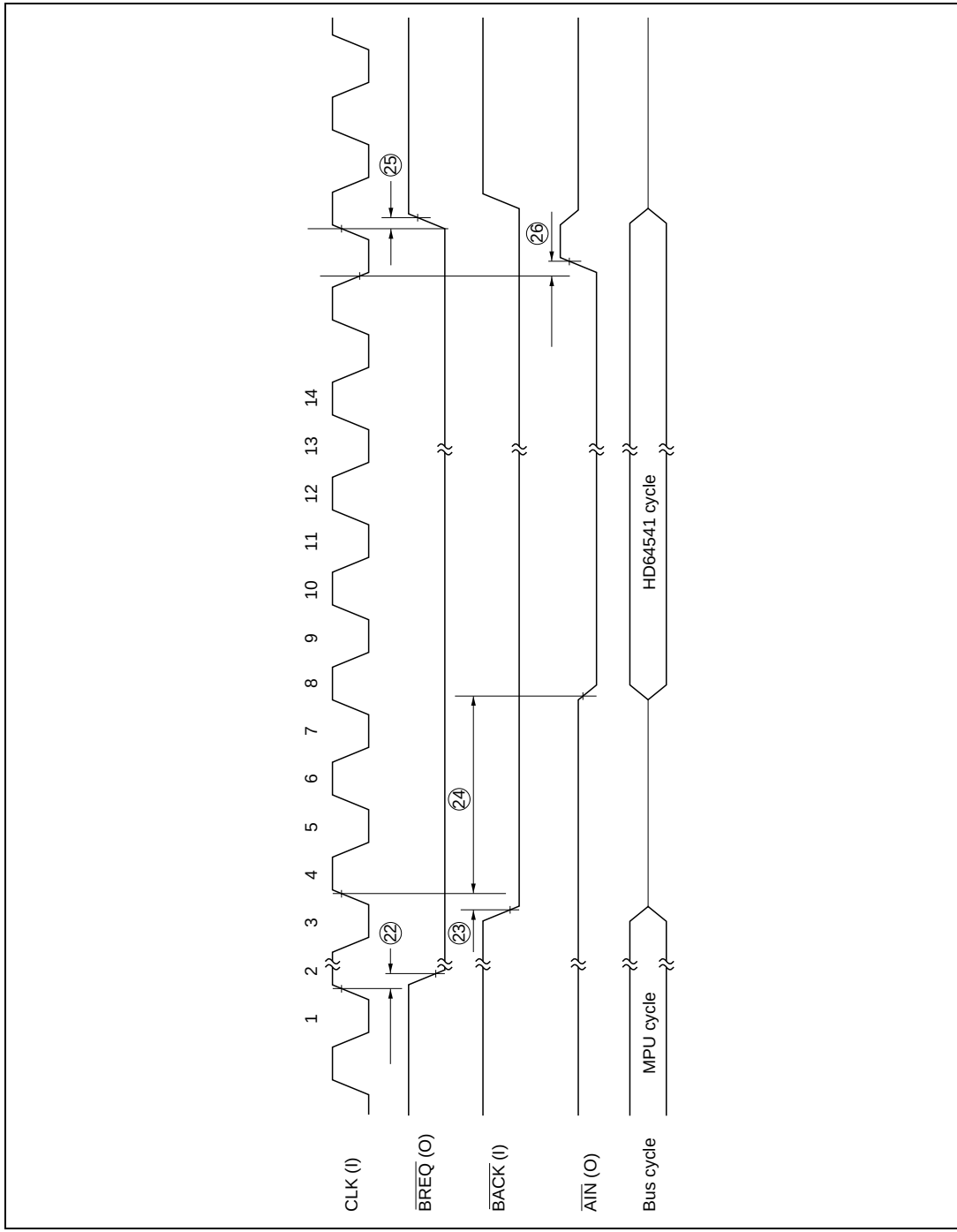


Figure 5-5 Bus Arbitration Timing

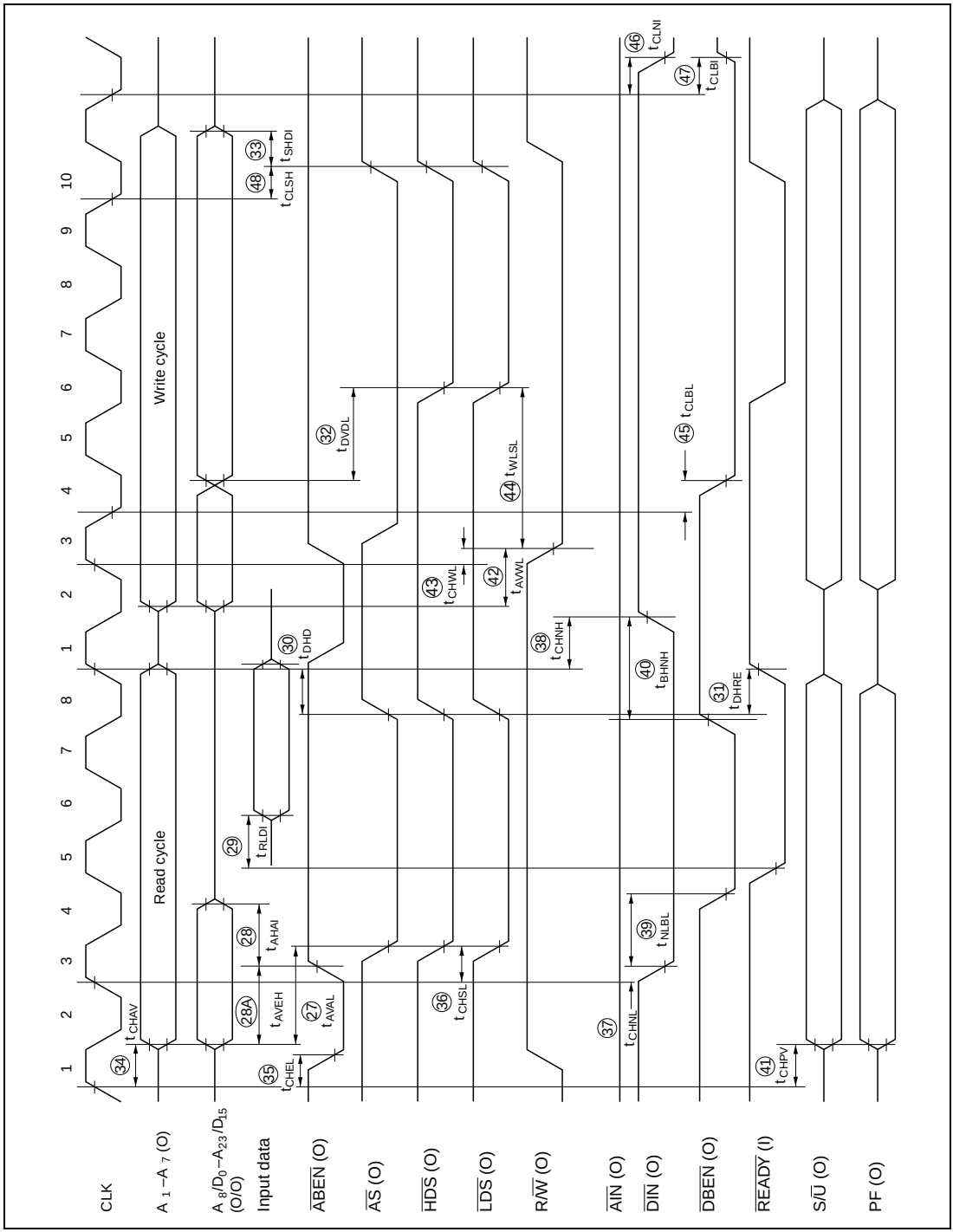


Figure 5-6 DMA Read/Write Timing

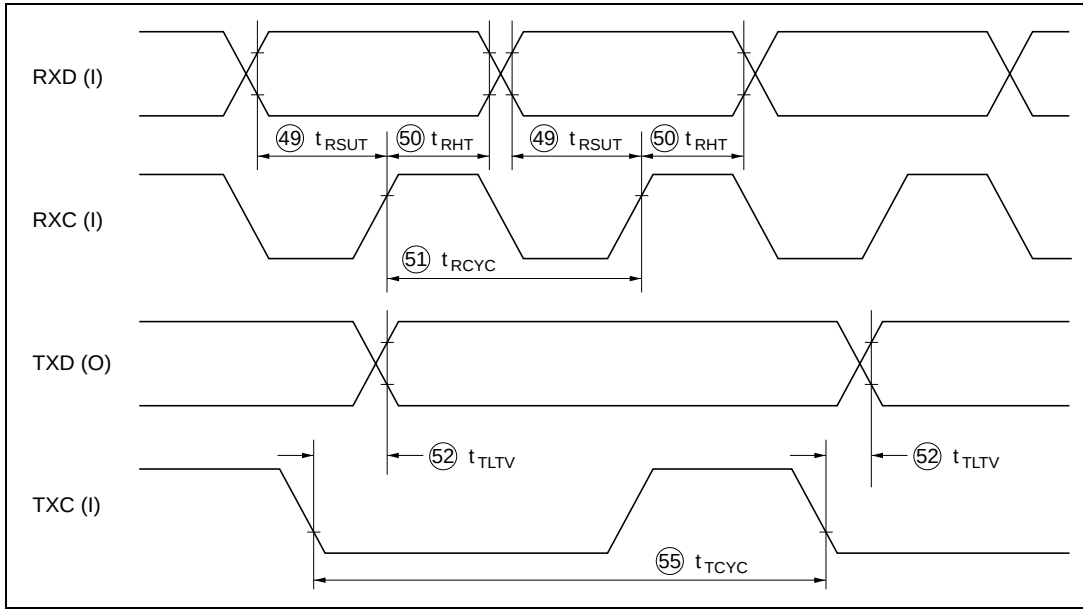


Figure 5-7 Transmit/Receive Timing

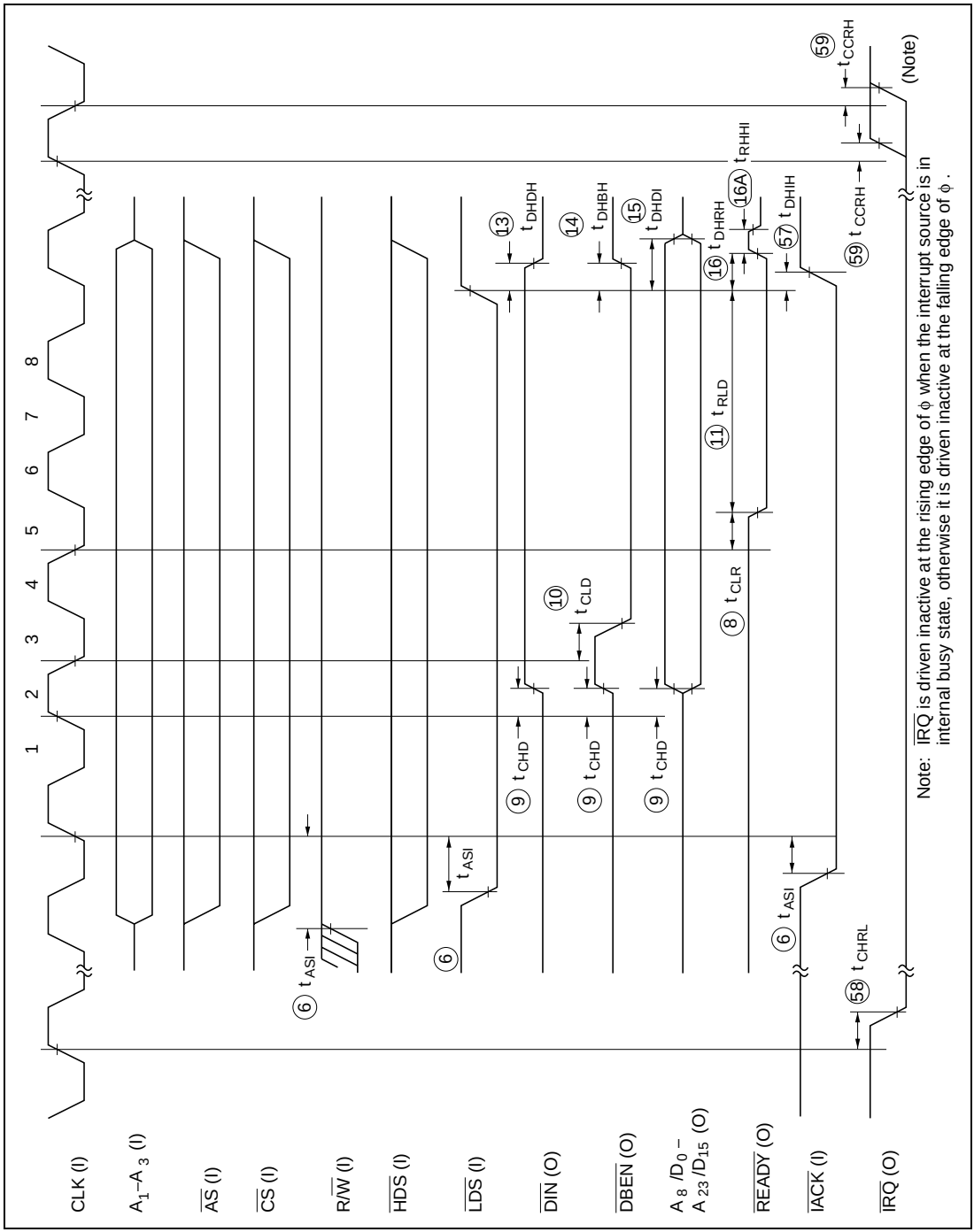


Figure 5-8 Interrupt Acknowledge Cycle

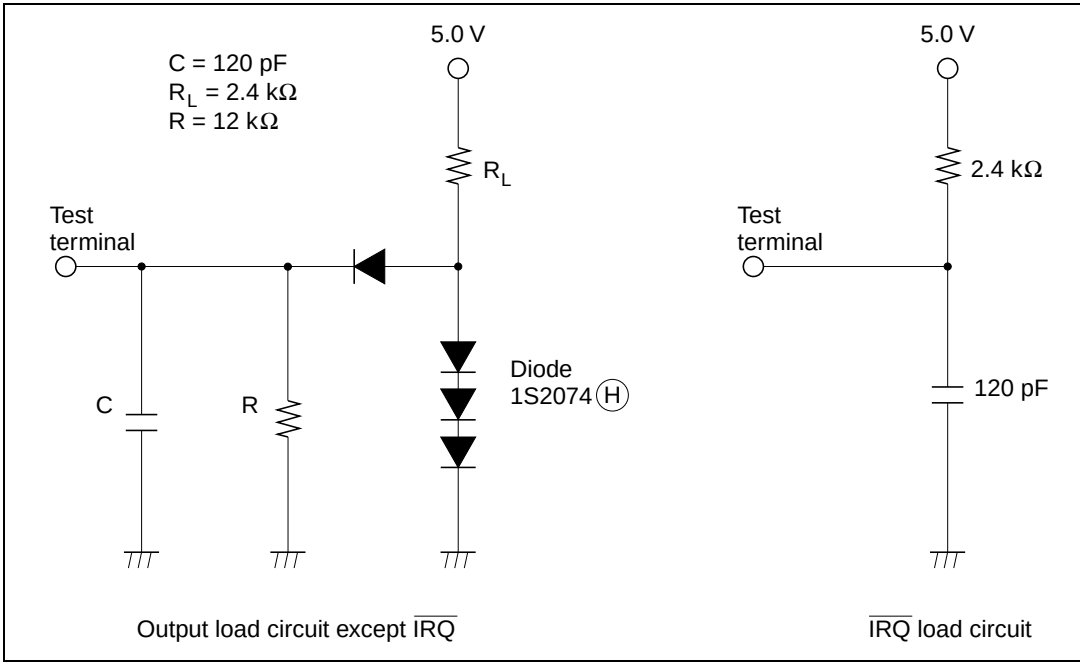


Figure 5-9 Output Load Circuit

Appendix A Command Details

A.1 CPOL (Control Peripheral Output Pin Level)

A.1.1 Format

	7	6	5	4	3	2	1	0	
0	0	1	1	1	1	1	1	0	($10)
1	—								
2	—						EN1	EN0	
3	—						PO1	PO0	

A.1.2 Function

CPOL sets the logic level of the two peripheral output pins.

A.1.3 Command Usage

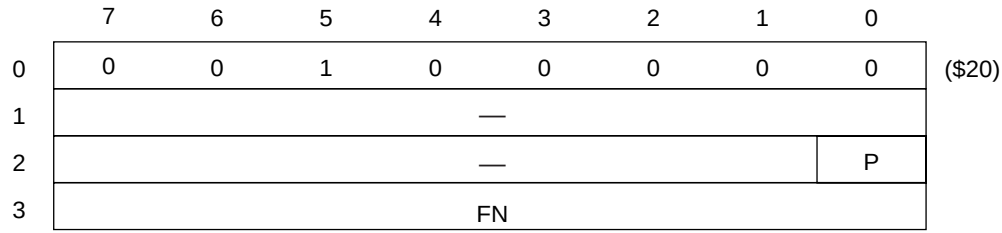
The CPOL command is not valid during RSET command wait state. Using it will generate a command format error (CMSR = 010). This command is valid at all other times.

A.1.4 Description

The HD64541's two peripheral output pins are driven from internal latches. CPOL loads new values into those latches. A new value (0/1), specified by PO, is loaded into the latch bit if the enable bit EN is set to 1. PO0 and EN0 operate on PO0 (pin No. 49), and PO1 and EN1 operate on PO1 (pin No. 50). The two pins are completely independent of each other and of the status of the LSI physical line.

A.2 DDR1 (I-Frame Transmission 1)

A.2.1 Format



FN is the number of frames to be transmitted.

A.2.2 Function

DDR1 (and DDR2) initiates the transmission of a series of I-frames. DDR1 is not valid immediately after the posting of DESI status and before at least one execution of DDR2.

A.2.3 Command Usage

1. This command is not valid if the HD64541 is offline in RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).
3. This command is not valid with an FN which specifies the length of the output I-field buffer descriptor table. FN > NSI or FN = 0 will generate a command format error (CMSR = 010).
4. This command is not valid immediately after the posting of DESI status and before at least one execution of DDR2. This feature forces the driver software to recognize a logical link reset before resuming I-frame transmission. Attempting DDR1 immediately after DESI generate a cannot execute error (CMSR = 100).
5. This command is not valid if the logical link has not yet been established and will generate a cannot execute error (CMSR = 100).

A.2.4 Description

Initiates the transmission of a series of I-frames to the remote station over the logical link. FN specifies the number of I-frames in the series. The SII entry in the SIIT must be prepared prior to DDR execution. The SII contains buffer descriptors for the outbound I-fields.

The P bit of the I-frame to be transmitted immediately following this command is set to the value of the P bit of this command, and the P bits from the second I-frame on are set to 0.

A.3 DDR2 (I-Frame Transmission 2)

A.3.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	0	0	1	($21)
1	—								
2	—							P	
3	FN								

FN indicates the number of frames to be transmitted.

A.3.2 Function

DDR2 (and DDR1) initiates the transmission of a series of I-frames. Unlike DDR1, DDR2 is also valid immediately after the posting of DESI status.

DDR2 also initiates the transmission of frames in transparent mode.

A.3.3 Command Usage

1. This command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid with an FN which specifies the length of the output I-field buffer descriptor table. FN > NSI or FN = 0 will generate a command format error (CMSR = 010).
3. This command is not valid if the logical link has not yet been established. Using it will generate a cannot execute error (CMSR = 100).

In transparent mode, before the current frame has finished being transmitted, the next command can initiate transmission of the following frame.

In transparent mode, if commands are continuously issued before transmission has completed, confirm the completion of transmission by checking the status of TAIF, which corresponds to the final transmission of request frames.

A.3.4 Description

Initiates the transmission of a series of I-frames to the remote station over the logical link. FN specifies the number of I-frames in the series. The SII entry in the SIIT must have been prepared prior to DDR execution. The SII contains buffer descriptors for the outbound I-fields.

A.4 DERC (Dump Statistical Information)

A.4.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	1	1	($13)
1	A23	Dump destination address (H)							
2	Dump destination address (M)								
3	Dump destination address (L)							A0	

A.4.2 Function

DERC causes the HD64541 to write the contents of its internal logout table (LOGT), containing statistical counters, to external memory starting at the address specified in the command, and to clear the counters to zero.

A.4.3 Command Usage

The DERC command is not valid during RSET command wait state. Using it will generate a command format error (CMSR = 010). This command is valid at all other times.

A.4.4 Description

Writes the contents of the HD64541's internal logout table (LOGT) to external memory starting at the address specified in the command and clears the counters to zero.

A.4.5 Note

Counter overflow beyond 255 is indistinguishable from an actual count of 255.

A.5 DESR (Establish Link)

A.5.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	1	0	1	($25)
1					—				
2					—				
3					—				

A.5.2 Function

DESR establishes the logical link.

A.5.3 Command Usage

1. This command is not valid if the HD64541 is offline or in RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the logical link has already been established. Using it will generate a cannot execute error (CMSR = 100).
3. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error.

A.5.4 Description

Establishes the logical link by transmitting SABM/SABME command. DESI status is then reported.

If the logical link cannot be established, DRLI status is reported.

A.6 DESW (Remote Station Link Establish Wait)

A.6.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	0	1	($29)
1					—				
2					—				
3					—				

A.6.2 Function

Places the HD64541 in link establish wait state (link established by remote station).

A.6.3 Command Usage

1. This command is not valid if the HD64541 is not in data link release state. Using it will generate a cannot execute error. (CMSR=100)
2. This command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
3. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).

A.6.4 Description

1. Places the HD64541 in data link establish wait state if data link has already been released.
2. Issue this command to establish the first link (after transition to on-line mode by the OMDS command) by receiving the SABM/SABME command from the remote station. If a SABM/SABME command sent from the remote station is received without this command being issued, the HD64541 will send a DM response.

A.7 DRLR (Release Link)

A.7.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	1	1	0	($26)
1					—				
2					—				
3					—				

A.7.2 Function

DRLR releases the logical link.

A.7.3 Command Usage

1. This command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).
3. This command is not valid if the logical link has not been established. Using it will generate a cannot execute error (CMSR = 100).

A.7.4 Description

Releases the logical link by transmitting DISC command. After the link is released, DRLI status is reported.

A.8 DSPT (Dump System Parameter Table (SYSPT))

A.8.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	1	0	($12)
1	A23	Dump destination address (H)							
2	Dump destination address (M)								
3	Dump destination address (L)							A0	

A.8.2 Function

DSPT causes the HD64541 to write the contents of its internal system parameter table (SYSPT) to external memory starting at the address specified in the command.

A.8.3 Command Usage

The DSPT command is valid only when the HD64541 is offline. Using it otherwise will generate a command format error (CMSR = 010).

A.8.4 Description

Writes the contents of the HD64541's internal system parameter table (SYSPT) to external memory starting at the address specified in the command.

A.9 MPIS (Mask Information from Peripheral Input Pins)

A.9.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	0	1	($11)
1	A23				—				
2			—			PI2	PI1	PI0	
3					—				

When PIi = 1, PIi pin input is masked.

A.9.2 Function

MPIS controls whether level changes on the three peripheral input pins are reported to the external microprocessor via status PITL.

A.9.3 Command Usage

The MPIS command is not valid during RSET command wait state. Using it will generate a command format error (CMSR = 010). This command is valid at all other times.

A.9.4 Description

1. Following a RSET command, all three peripheral input pins are masked off and no level changes are reported.
2. MPIS enables/disables reporting of level changes on the three pins independently.
3. If a level change occurs on a pin that has been masked off, the change is reported as soon as the pin is masked on. If multiple level transitions have occurred while the pin is masked off, only the last one is reported.
4. If the corresponding bit in the MPIS command was set to 1, level changes on that pin are not reported in the PITL status.

A.10 MUDR (U and X Frame Transmission)

A.10.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	0	1	0	($22)
1					—				
2					—				
3					—				

A.10.2 Function

MUDR initiates the transmission of a single UI, XID, or TEST frame.

A.10.3 Command Usage

1. This command is not valid if the HD64541 is offline or in RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).
3. This command is not valid when bit 2 of PMODE in SYSPT is set to 0, (U and X frame inhibit state). Using it will generate a command format error (CMSR = 010).

A.10.4 Description

Initiates the transmission of a single UI, XID, or TEST frame to the remote station over the logical link. The SUXI entry in the SUXIT must be prepared prior to MUDR execution. The SUXI contains buffer descriptors for the outbound I-field.

Even if the transmission of a UI, XID, or TEST frame initiated by the previous MUDR commands is not finished, further MUDRs can be executed.

If before transmission has completed more commands are continuously issued, confirm the completion of transmission by checking the status of TAIF, which corresponds to the final transmission of request frames.

A.11 OMDS (Set Operating Mode)

A.11.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	0	($02)
1	—					M2	M1	M0	
2	—								
3	—								

M0	State
0	Online
1	Online

M2	M1	Mode
0	0	Normal
0	1	Local loopback
1	0	Auto echo
1	1	Auto echo with local loopback

A.11.2 Function

OMDS specifies three operating mode toggles: online/offline (M0), local loopback on/off (M1) and auto echo on/off (M2).

A.11.3 Command Usage

This command is not valid during RSET command wait state. Using it will generate a command format error (CMSR = 010). This command is valid at all other times. RSET command wait state immediately follows a hardware reset and is cleared by the execution of a RSET command from the external microprocessor.

FSYC status is reported if flag sequence is received when this command changes an offline mode to an online mode.

A.11.4 Description

Bit M0: M0 controls whether the HD64541 is online or offline.

- Online (= 0): Enables LAPB frame transmit and receive. If no outbound frames are ready for transmission, the HD64541 transmits flag sequence or frame specified in the procedure.
- Offline (= 1): Disables LAPB frame receive. The HD64541 transmits continuous 1 bits.

Bit M1: M1 controls local loopback (figure A-1).

- Local loopback off (= 0): If auto echo is also off, establishes normal operation using TXD, RXD, TXC, and RXC pins.
- Local loopback on (= 1): Causes transmit data to be internally looped back to receive data as though received over RXD. A clock must be provided on TXC as though normal operation were in effect. Both local loopback and auto echo may be on at the same time.

Bit M2: M2 controls auto echo (figure A-1).

- Auto echo off (= 0): If local loopback is also off, establishes normal operation using TXD, RXD, TXC, and RXC pins. (Auto echo is known as remote loopback.)
- Auto echo on (= 1): Causes received data on RXD to be internally looped back out to TXD transmit data as though sent by the local station. A clock must be provided on TXC as though normal operation were in effect. Both local loopback and auto echo may be on at the same time.

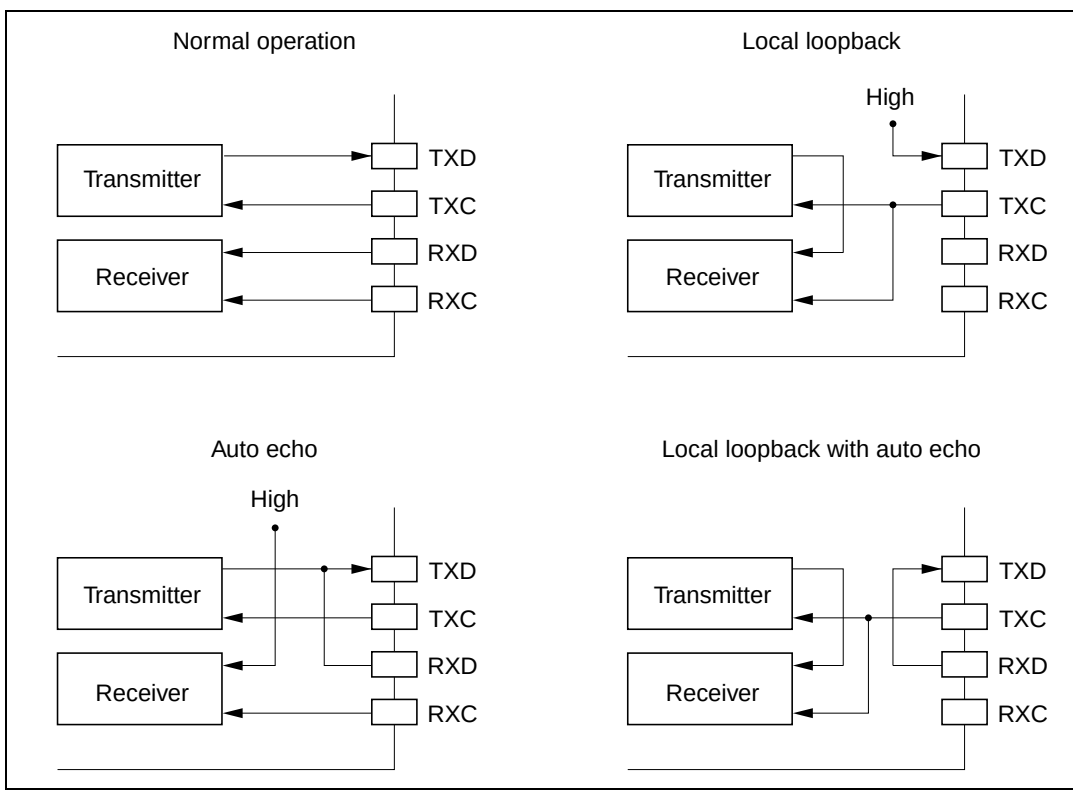


Figure A-1 Operation Modes

A.12 RESR (Reestablish Link)

A.12.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	1	0	($2A)
1					—				
2					—				
3					—				

A.12.2 Function

Reestablishes link while communication is going on or in error recovery wait state.

A.12.3 Command Usage

1. This command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).
3. This command is not valid if the logical link has not been established. Using it will generate a cannot execute error (CMSR = 100).

A.12.4 Description

Reestablishes link by transmitting SABM/SABME command.

A.13 RETD (Resume Frame Transmission)

A.13.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	1	0	0	($24)
1					—				
2					—				
3					—				

A.13.2 Function

Resumes I-, UI, XID, and TEST frame transmission.

A.13.3 Command Usage

The RETD command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).

A.13.4 Description

Reverses the effect of a previously executed SUTD command and allows the resumption of I-, UI, XID, and TEST frame transmission.

A.14 RSBY (Release Local Station from Busy State)

A.14.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	0	0	($28)
1	—								
2	—								
3	—								

A.14.2 Function

RSBY releases the logical link from the busy state set by a previously executed SSBY command.

A.14.3 Command Usage

1. This command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).
3. RSBY is allowed even in HD64541 internal busy state.
4. This command is not valid for a logical link that cannot change from busy to non-busy. Using it will generate a cannot execute error (CMSR = 100).

A.14.4 Description

The logical link exits the busy state previously set by SSBY.

A.15 RSET (Reset)

A.15.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	0	0	($01)
1	A23	System parameter table start address (H)							
2	System parameter table start address (M)								
3	System parameter table start address (L)							A0	

A.15.2 Function

RSET resets the HD64541's internal status and causes the HD64541 to read new system operating parameters from the system parameter table (SYSPT) whose address is specified in the RSET command.

A.15.3 Command Usage

This command is valid only when the HD64541 is offline.

A.15.4 Description

1. Initializes HD64541 internal status.
2. Loads new system parameters from the specified SYSPT.
3. RSET command wait state immediately follows a hardware reset and is cleared by the execution of a RSET command from the external microprocessor.

A.15.5 Notes

1. A bus exception during SYSPT parameter fetch causes the bus cycle to terminate abnormally and generates an interrupt with CMSR = 010. If the interrupt vector cannot be properly fetched, vector 0FH is used.
2. The HD64541 does not check the validity of parameters loaded from the SYSPT.

A.16 SSBY (Set Local Station to Busy State)

A.16.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	1	1	1	($27)
1					—				
2					—				
3					—				

A.16.2 Function

SSBY sets the logical link to busy.

A.16.3 Command Usage

1. This command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. This command is not valid if the HD64541 is in transparent mode. Using it will generate a command format error (CMSR = 010).
3. This command is not valid for a logical link that cannot change from non-busy to busy. Using it will generate a cannot execute error (CMSR = 100).
4. SSBY is allowed even in HD64541 internal busy state.
5. The busy state set by SSBY has no affect on logical link reestablish and release procedures.

A.16.4 Description

Logical link busy set by SSBY may be cancelled by RSBY command or releasing logical link. Busy may be also cancelled by a transition to offline.

A.17 STAC (Set Area Code)

A.17.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	1	($00)
1	0	0	0	0	0	0	AC0		
2	0	0	0	0	0	0	AC1		
3	0	0	0	0	0	0	AC2		

The two bits in each of the three area code fields (AC0–AC2) correspond to the S/$\overline{U}$ and PF pins used in the HD64541 memory management scheme. Bit 0 maps to the supervisor/user pin S/$\overline{U}$ and bit 1 maps to the program fetch (PF) pin. Note that the program fetch (PF) pin is not to be confused with the LAPB protocol poll/final (P/F) bit.

A.17.2 Function

STAC specifies the area code (AC) values to be used by the HD64541 during DMA operations.

A.17.3 Command Usage

This command is always valid.

A.17.4 Description

Every address during a DMA transfer operation is accompanied by an area code specification (S/$\overline{U}$ and PF pins) that allows the targeted memory to either allow or reject the access. The HD64541 separates its memory resident control tables into three access classes, one associated with each of the three AC fields in the STAC command. When accessing a particular table in memory, its associated ACn determines the value of the S/$\overline{U}$ and PF pins sent out on the bus. Table A-1 shows the three access classes and the control tables they encompass.

Table A-1 Access to Control Tables

AC	Read Access	Write Access
AC0	SYSPT, REJIT	SYSDT, LOGT, REJIT
AC1	SIIT, ESII, RBIT, SUXIT	SIIT, SUXIT, RBIT
AC2	SDB	RDB

A.17.5 Notes

1. After a hardware reset, ACn values are unpredictable.
2. A software reset (RSET) has no effect on ACn values.
3. STAC must follow a hardware reset and may precede RSET.

A.18 SUTD (Suspend Frame Transmission)

A.18.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	0	1	1	($23)
1					—				
2					—				
3					—				

A.18.2 Function

Temporarily suspends I-, UI, XID, and TEST frame transmission.

A.18.3 Command Usage

1. The SUTD command is not valid if the HD64541 is offline or during RSET command wait state. Using it will generate a command format error (CMSR = 010).
2. When the operation mode is switched to off-line mode from on-line mode, suspended state will be cleared.
3. If SUTD is issued in this suspended state, command operation will be terminated normally while suspended state remains.

A.18.4 Description

I-, UI, XID, or TEST frame transmission initiated by DDR1, DDR2, and MUDR commands is suspended until the resume transmission command RETD is executed. A frame whose transmission is already in progress when SUTD is executed is allowed to continue to completion.

Appendix B Status Details

B.1 ACIF (Verify I-Frame)

B.1.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	1	($03)
1	—								
2	ASIIN								
3	—								

B.1.2 Reporting Function

1. Indicates that a transmitted I-frame has been acknowledged by the remote station.
2. ASIIN identifies the SII buffer descriptor holding the acknowledged frame.

B.2 DESI (Establish Link)

B.2.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	1	($01)
1	—								
2	—								
3	—								

B.2.2 Reporting Function

1. The logical link has been established or reestablished by the remote station. The HD64541 received SABM/SABME and responded with UA.
2. The logical link has been established or reestablished by the local station. The HD64541 sent SABM/SABME by DESR or RESR command and received UA.
3. The HD64541 was unable to successfully complete the transmission of an I-frame initiated by DDR1 or DDR2 earlier.

B.3 DRLI (Release Link)

B.3.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	0	($02)
1	—								
2	—								
3	—								

B.3.2 Reporting Function

1. The logical link has been released on the remote station's initiative.
2. The logical link establishment from the local station did not complete successfully by receiving DM frame from the remote station.

B.4 FREC (Receive Frames)

B.4.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	1	0	1	0	($0A)
1	—								
2	RBIN								
3	—								

B.4.2 Reporting Function

A frame containing an I-field has been correctly received and the I-field has been stored in the buffer whose descriptor is identified by RBIN. Information regarding the frame type is stored in the corresponding RBI.

FREC is reported once per frame and not once per buffer. If the frame's I-field spilled across two or more buffers, FREC is reported only once.

B.5 FSYC (Flag Synchronization)

B.5.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	1	0	0	($14)
1					—				
2					—				
3					—				

B.5.2 Reporting Function

1. The HD64541 received a flag sequence from the remote station during on-line mode that had been set by OMDS command from the external microprocessor.
2. The HD64541 received a flag sequence from the remote station after timer T3 runout had occurred.

B.6 IDET (Idle Detection)

B.6.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	0	0	($10)
1					—				
2					—				
3					—				

B.6.2 Reporting Function

1. T3 time has elapsed since the detection of an idle pattern.
2. If bit 3 of PMODE in SYSPT is set to 0, IDET will be sent to the external microprocessor immediately following the detection of an idle pattern.

IDET status reporting condition

- Receive continuous 1s for a period of at least 15 bit times when line rate is up to 1.5 Mbps.
- Receive continuous 1s for a period of at least 18 bit times when line rate is more than 1.5 Mbps.

B.7 LRST (Reset Link)

B.7 1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	1	1	0	($16)
1					—				
2					—				
3					—				

B.7.2 Reporting Function

1. The HD64541 issued a SABM/SABME command to initiate a link reset.
2. Issuing this status prevents the HD64541 from execute commands such as data transmission before UA response from the remote station is received.
3. When the HD64541 receives a UA response from the remote station, it sends DESI (establish link) status to the external microprocessor and is placed in link establish state.
4. This status is issued when a SABM/SABME command is transmitted in any of the following cases:
   a. FRMR is received
   b. T1 runout occurs N2 times (in X.25 and X.75 modes)
   c. Unexpected supervisory frame with F = 1 is received (in X.25 mode)
   d. Unexpected UA or DM response is received (in X.25 mode)
5. The HD64541 does not issue this status if it transmits a SABM/SABME command on the Reestablish Link (RESR) command from the external microprocessor.

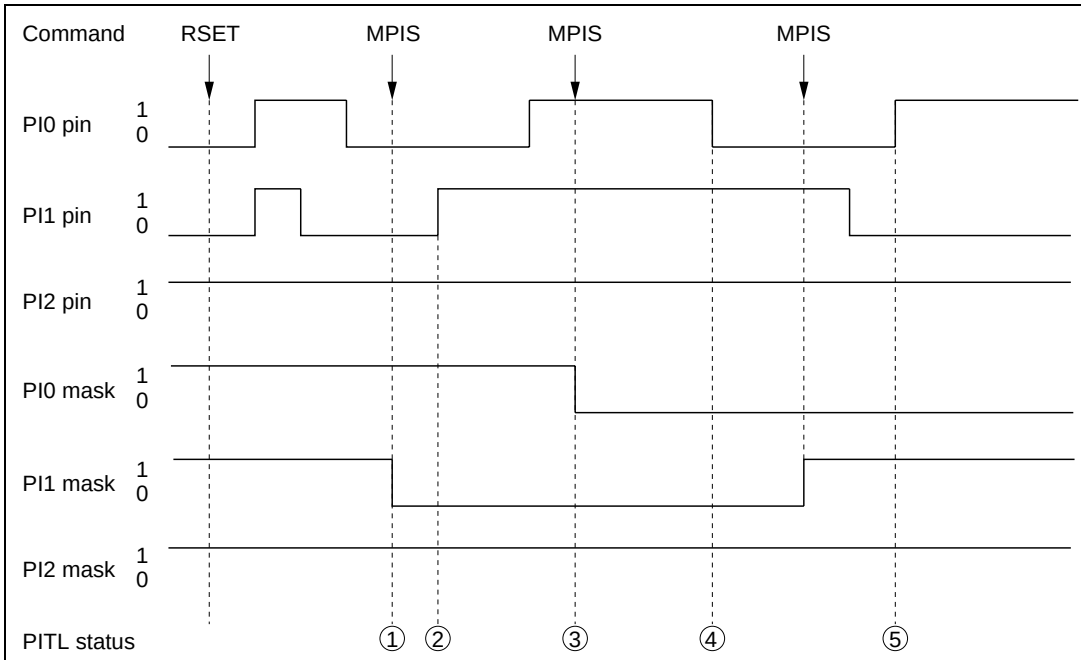
B.8 PITL (Peripheral Input Pin Level)

B.8.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	1	0	($06)
1	—								
2	0	0	0	0	0	PI2	PI1	PI0	
3	0	0	0	0	0	PT2	PT1	PT0	

B.8.2 Reporting Function

1. A level transition has occurred on any one or more of the three peripheral input pins PI0, PI1, or PI2 and the pin(s) are not currently masked by the MPIS command. If they are masked, the transition report is held pending until they are unmasked. If more than one transition occurs on the same pin while masked, only the last transition is reported when it is finally unmasked.
2. Bits PT0, PT1, and PT2 are set to 1 when reporting a transition on the associated pin.
3. Bits PI0, PI1, and PI2 are set to the new level after the transition. See figure B-1.



	PI2	PI1	PI0	PT2	PT1	PT0
①	1	0	0	0	0	0
②	1	1	0	0	1	0
③	1	1	1	0	0	1
④	1	1	0	0	0	1
⑤	1	0	1	0	1	1

Figure B-1 Masking Peripheral Input Pins

B.9 RRBY (Remote Station Busy Release)

B.9.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	0	1	($05)
1					—				
2					—				
3					—				

B.9.2 Reporting Function

The logical link has exited remote station busy by receiving RR from the remote station.

B.10 SRBY (Remote Station Busy)

B.10.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	0	0	($04)
1					—				
2					—				
3					—				

B.10.2 Reporting Function

The logical link has entered remote station busy state by receiving RNR from the remote station.

B.11 SRC1 (System Recovery Request 1)

B.11.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	0	1	($11)
1					—				
2					—				
3					—				

B.11.2 Reporting Function

- Receiving an FRMR-response has caused the HD64541 to be placed in error recovery wait state.
- The I-field of the received FRMR response is sent to the REJIT table.

B.12 SRC2 (System Recovery Request 2)

B.12.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	1	0	($12)
1					—				
2					—				
3					—				

B.12.2 Reporting Function

Though the local station retransmitted frames N2 times, no response was received from the remote station and timer T1 runout occurred in each retransmission.

B.13 TAIF (Terminate Frame Transmission)

B.13.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	1	1	($07)
1	—								
2	SIIN								
3	—								

B.13.2 Reporting Function

TAIF status is valid only in transparent mode. The transmission of a frame initiated by the DDR2 command has completed. SIIN identifies the SII buffer descriptor of the frame transmitted.

B.14 TAUF (Terminate U and X Frame Transmission)

B.14.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	0	1	0	0	1	($09)
1	—								
2	SUXIN								
3	—								

B.14.2 Reporting Function

The transmission of XID, UI or TEST frames initiated by the MUDR command has completed. SUXIN identifies the SUXI buffer descriptor of the frame transmitted.

B.15 YRCV (Remote Station System Recovery Request)

B.15.1 Format

	7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	1	1	($13)
1					—				
2					—				
3					—				

B.15.2 Reporting Function

1. Because an unrecoverable retransmitted frame had been received from the remote station, FRMR response was sent and the HD64541 is placed in the frame reject state.
2. The I-field of the transmitted FRMR response is stored in the REJIT table.

Appendix C Link Layer Protocol Sequence Diagrams

Typical examples of layer 2 protocol sequence diagrams are shown in this appendix. Refer to the state transition table in CCITT recommendation T.90, X.75, and X.25 (’88) in other cases.

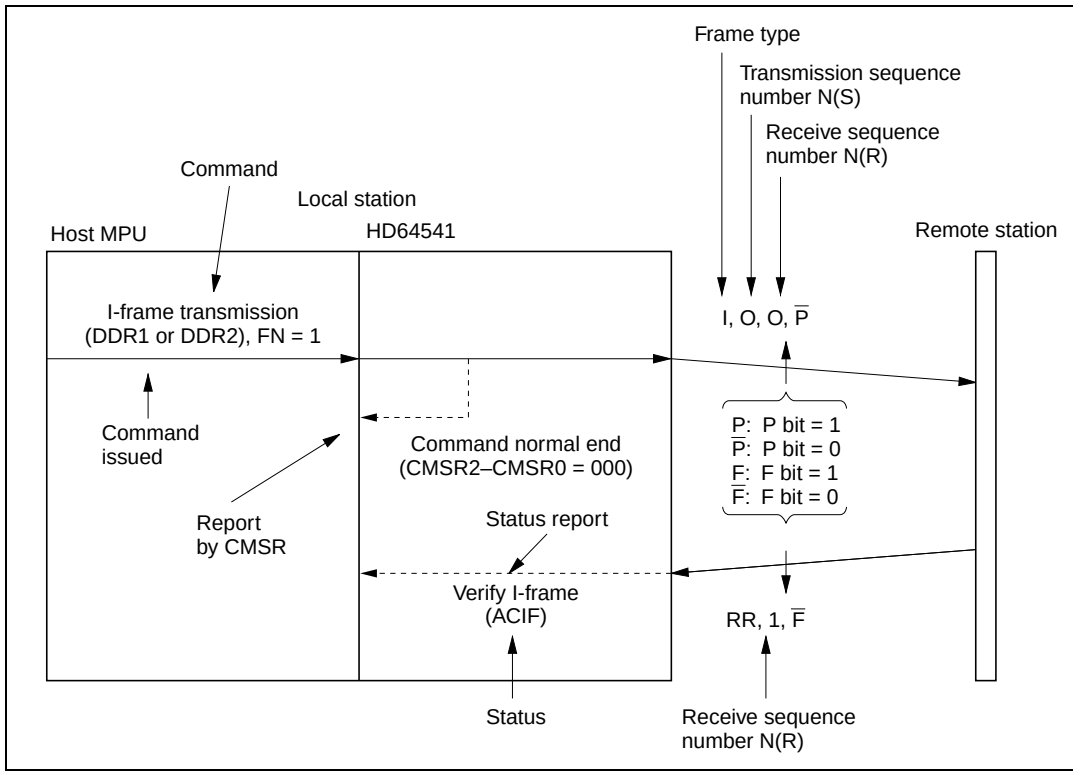


Figure C-1 Explanation of Figures

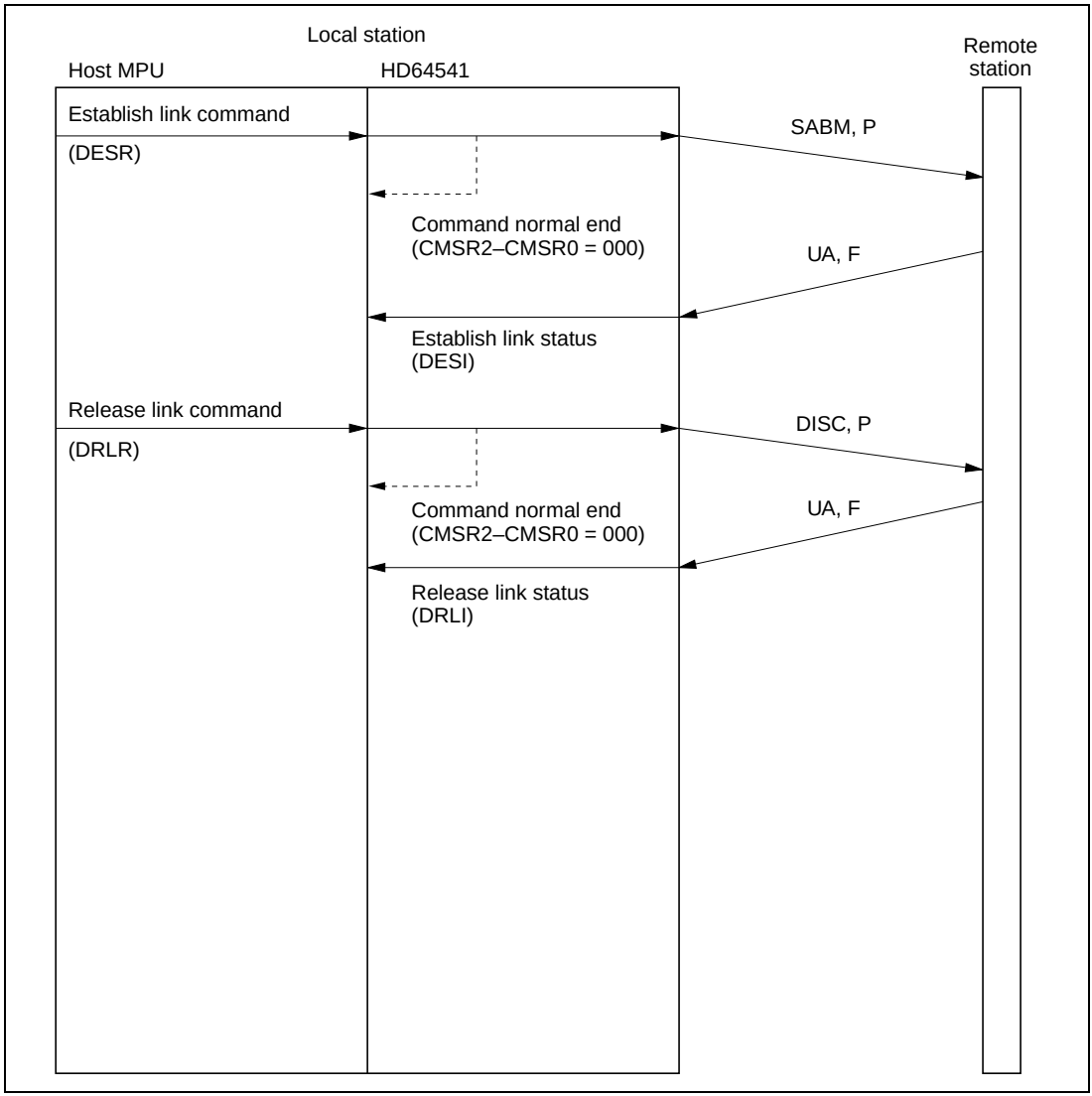


Figure C-2 Link Establishment and Link Release from Local Station

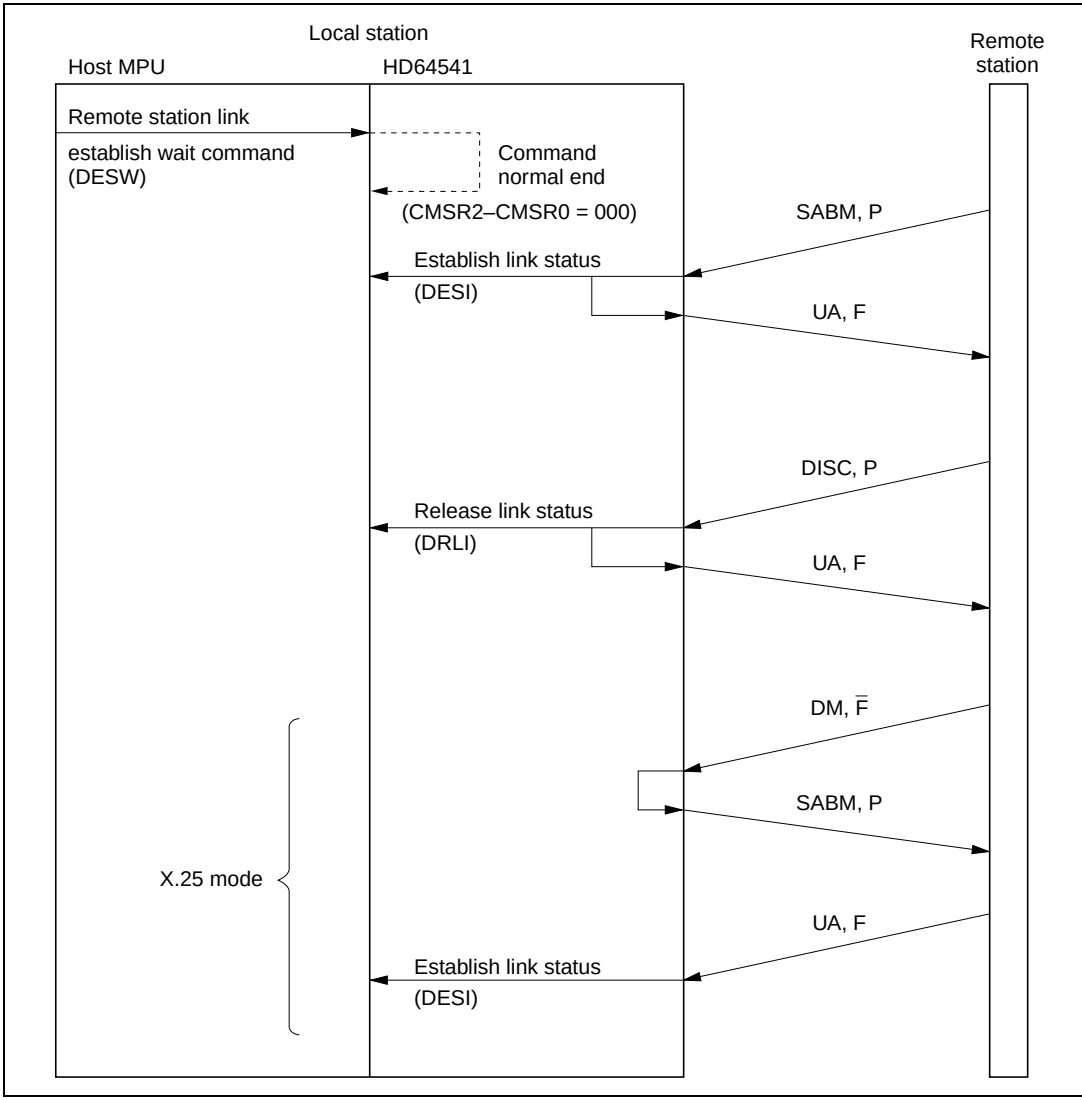


Figure C-3 Link Establishment and Link Release from Remote Station

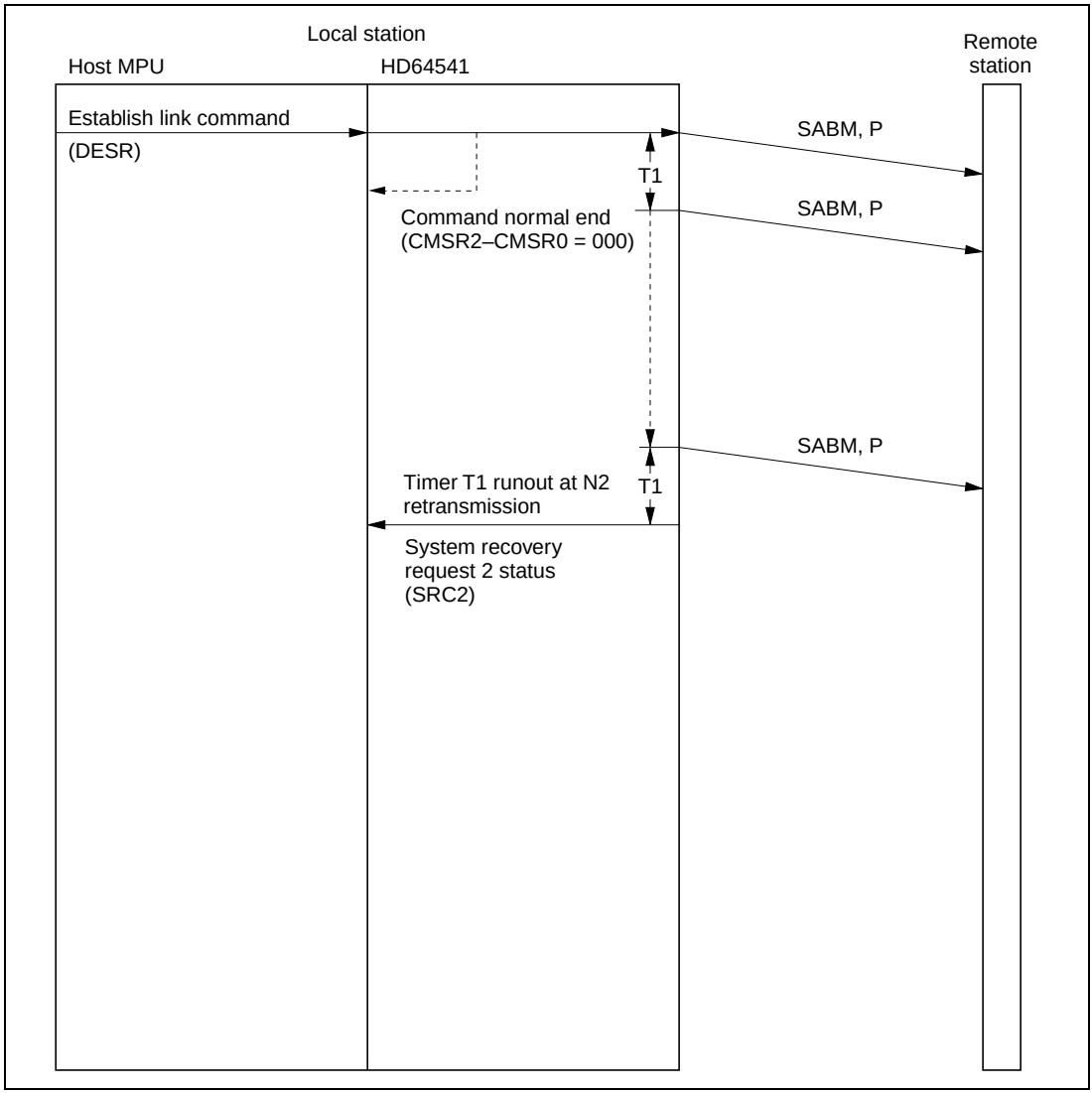


Figure C-4 Timer T1 runout during SABM Command Transmission

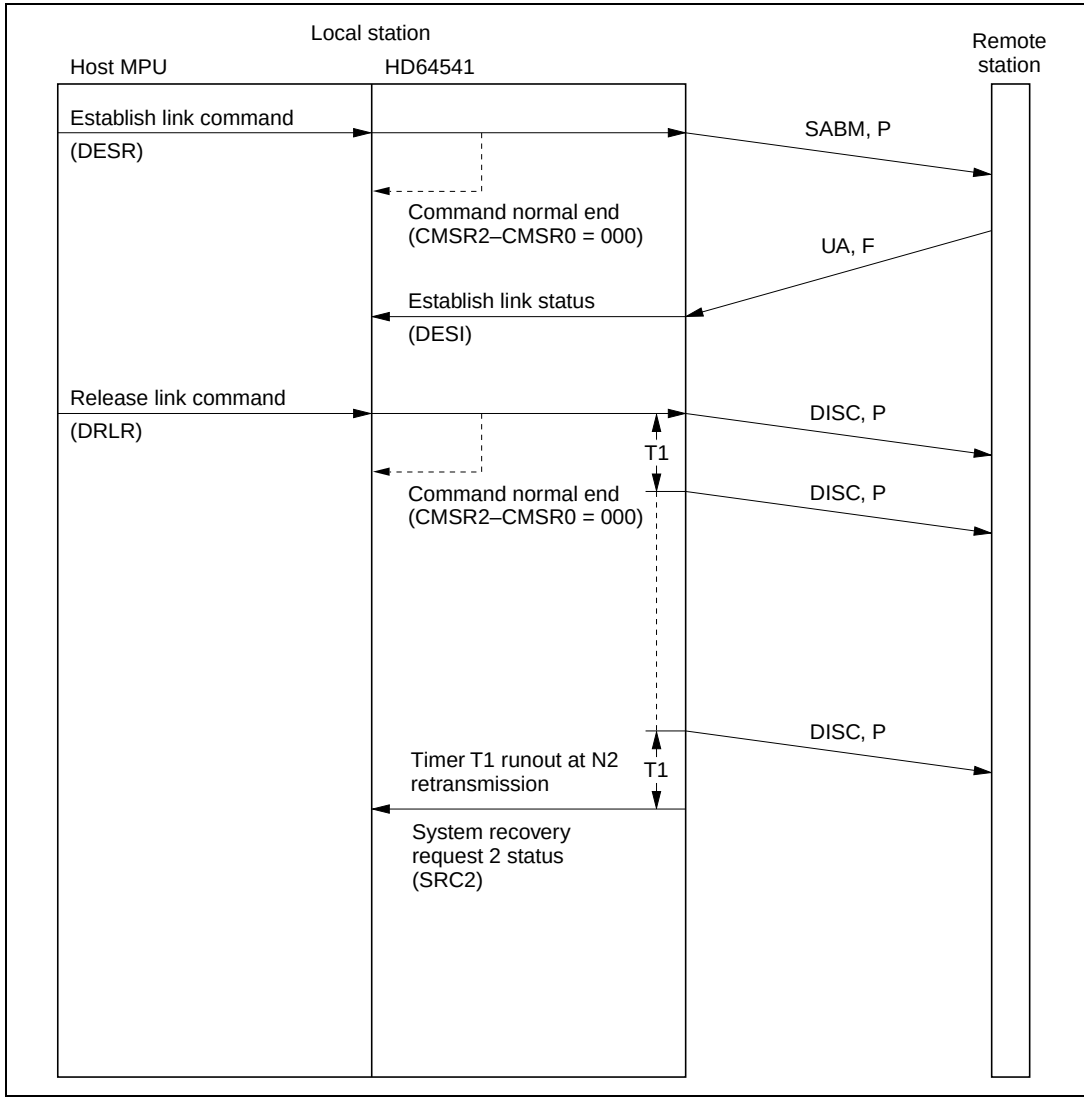


Figure C-5 Timer T1 runout during DISC Command Transmission

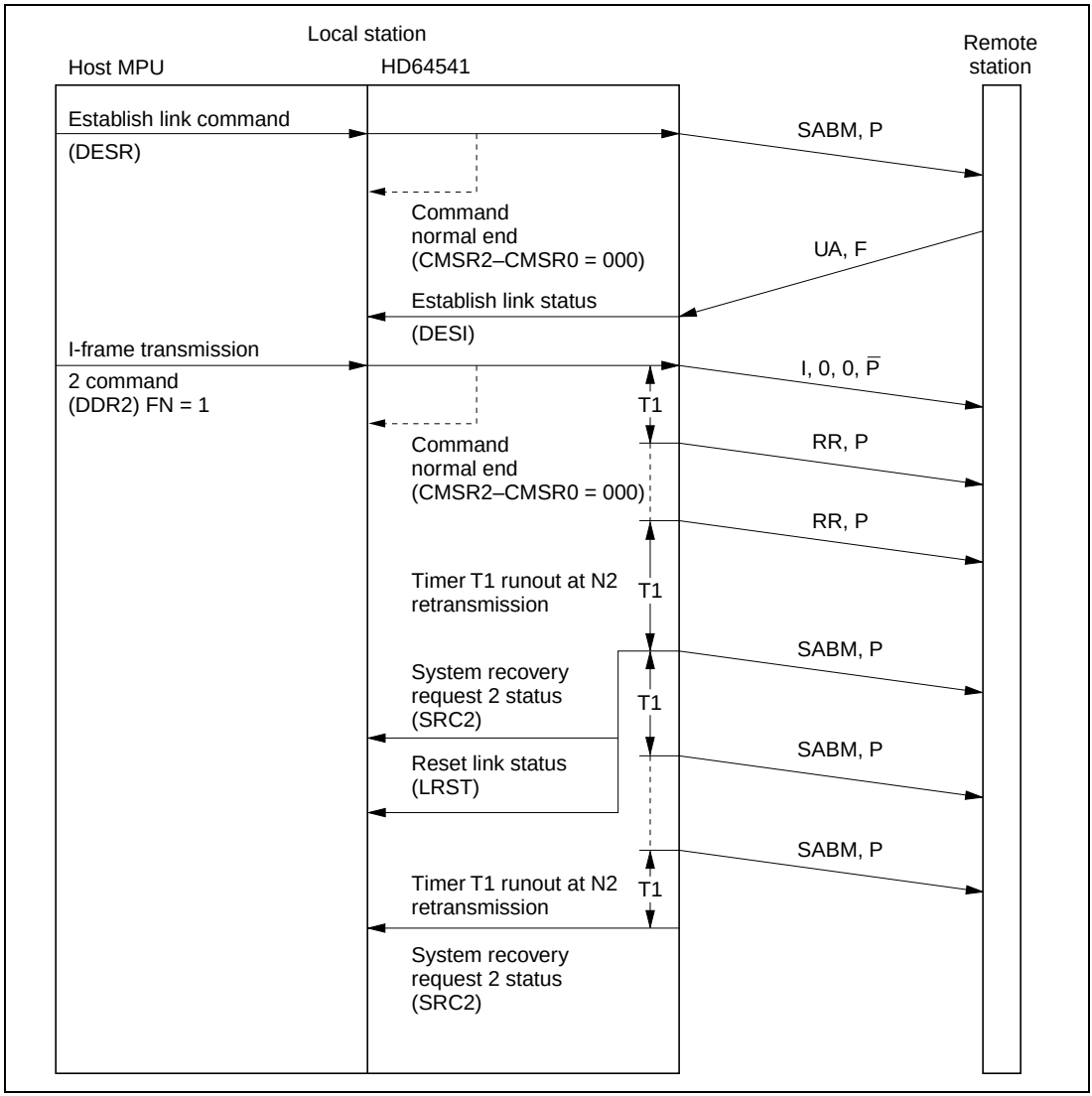


Figure C-6 (a) Link Disconnection by HD64541 (X.25 and X.75 modes)

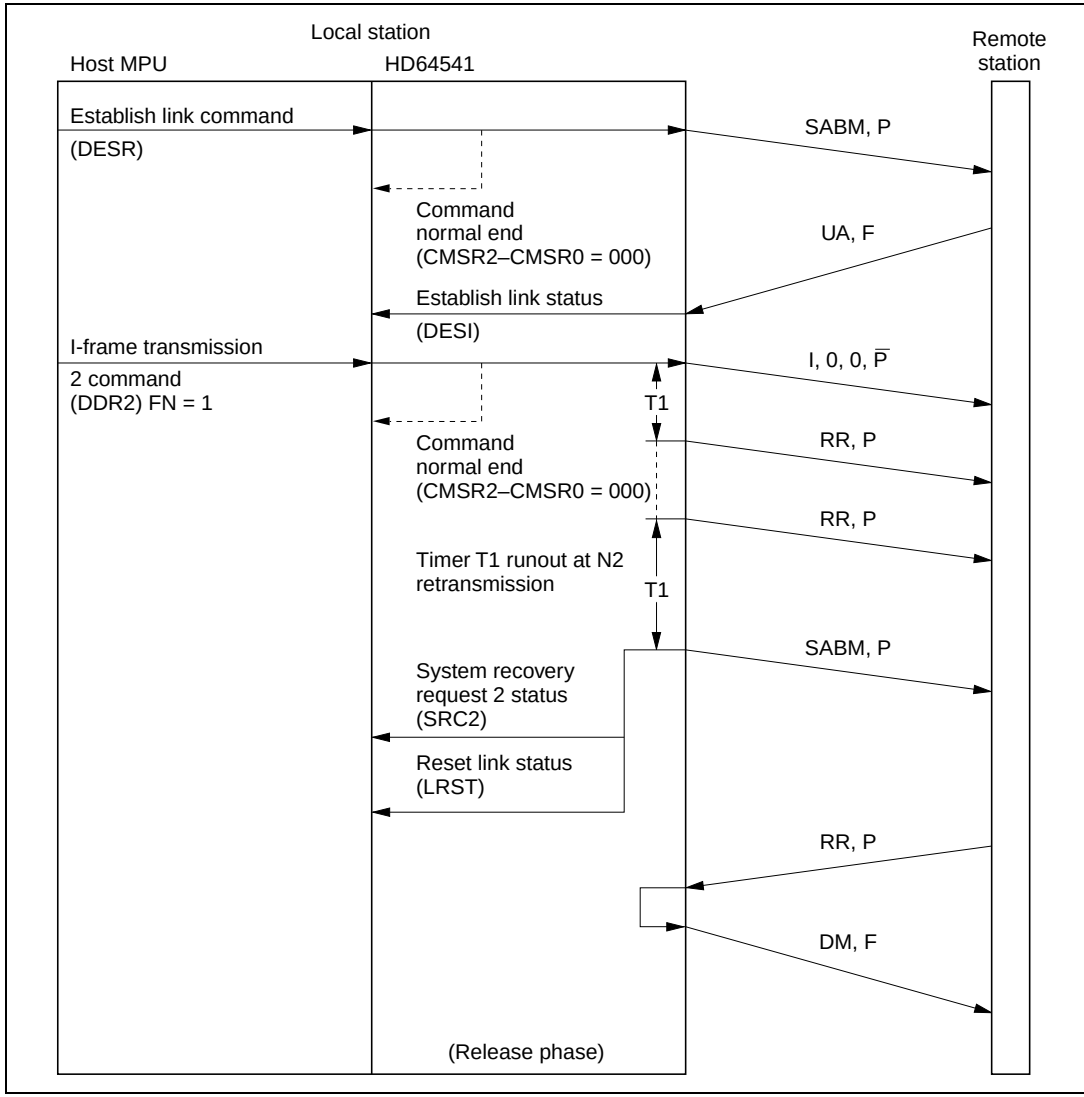


Figure C-6 (b) Link Disconnection by HD64541 (T.90 mode)

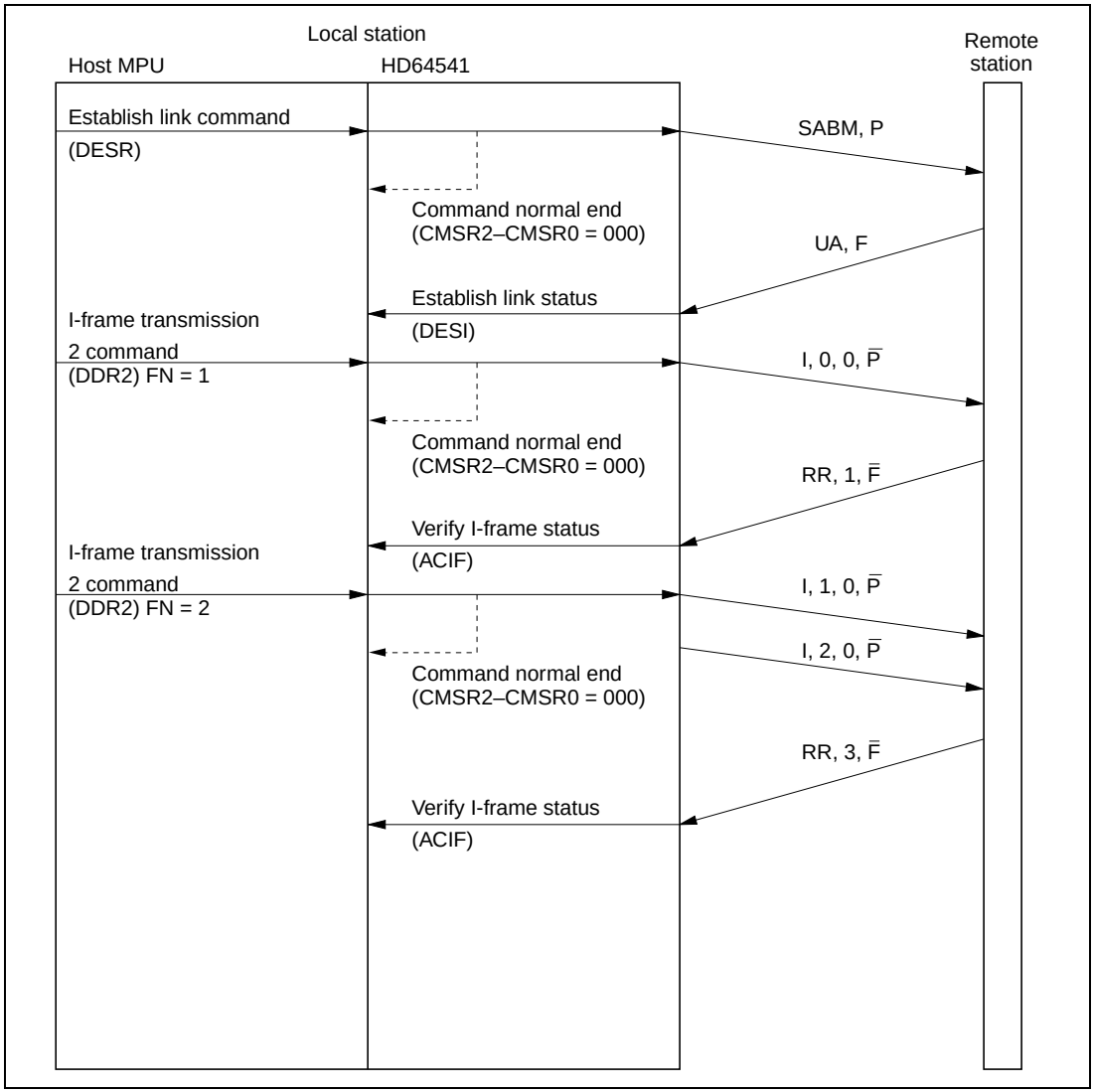


Figure C-7 I-Frame Transmission

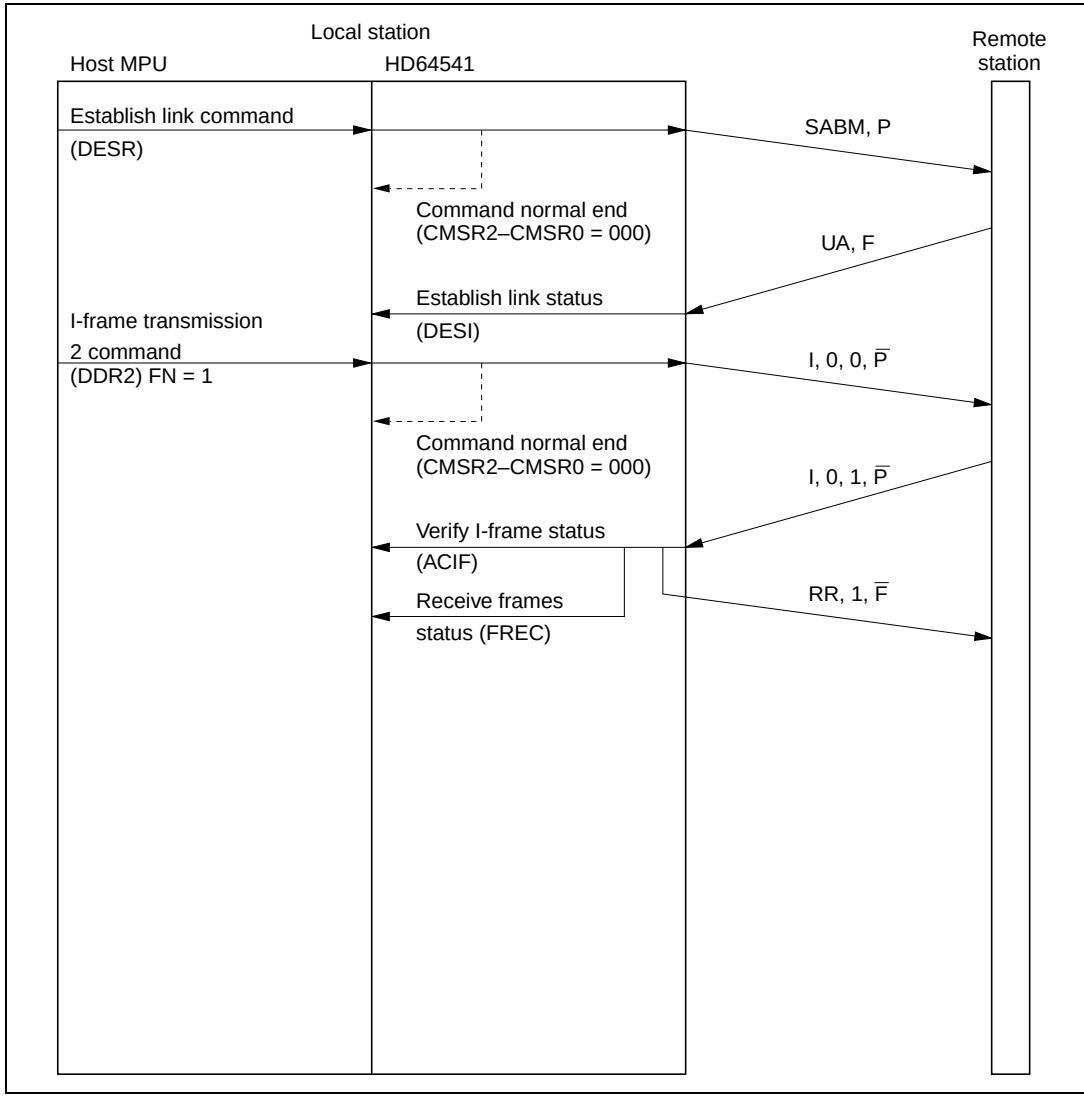


Figure C-8 I-Frame Reception and Transmission

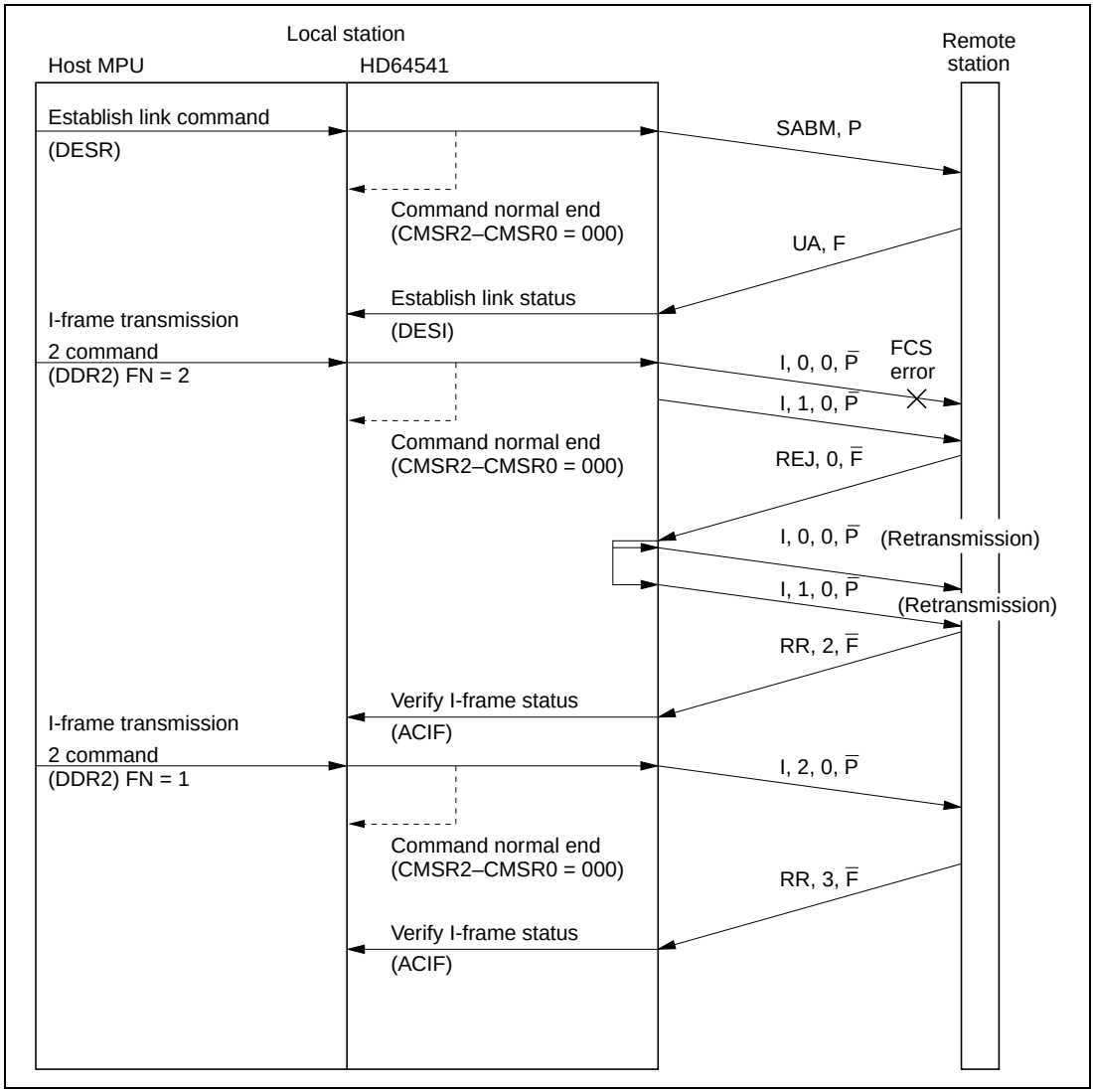


Figure C-9 Recovery of I-Frame Transmit Error by REJ Reception

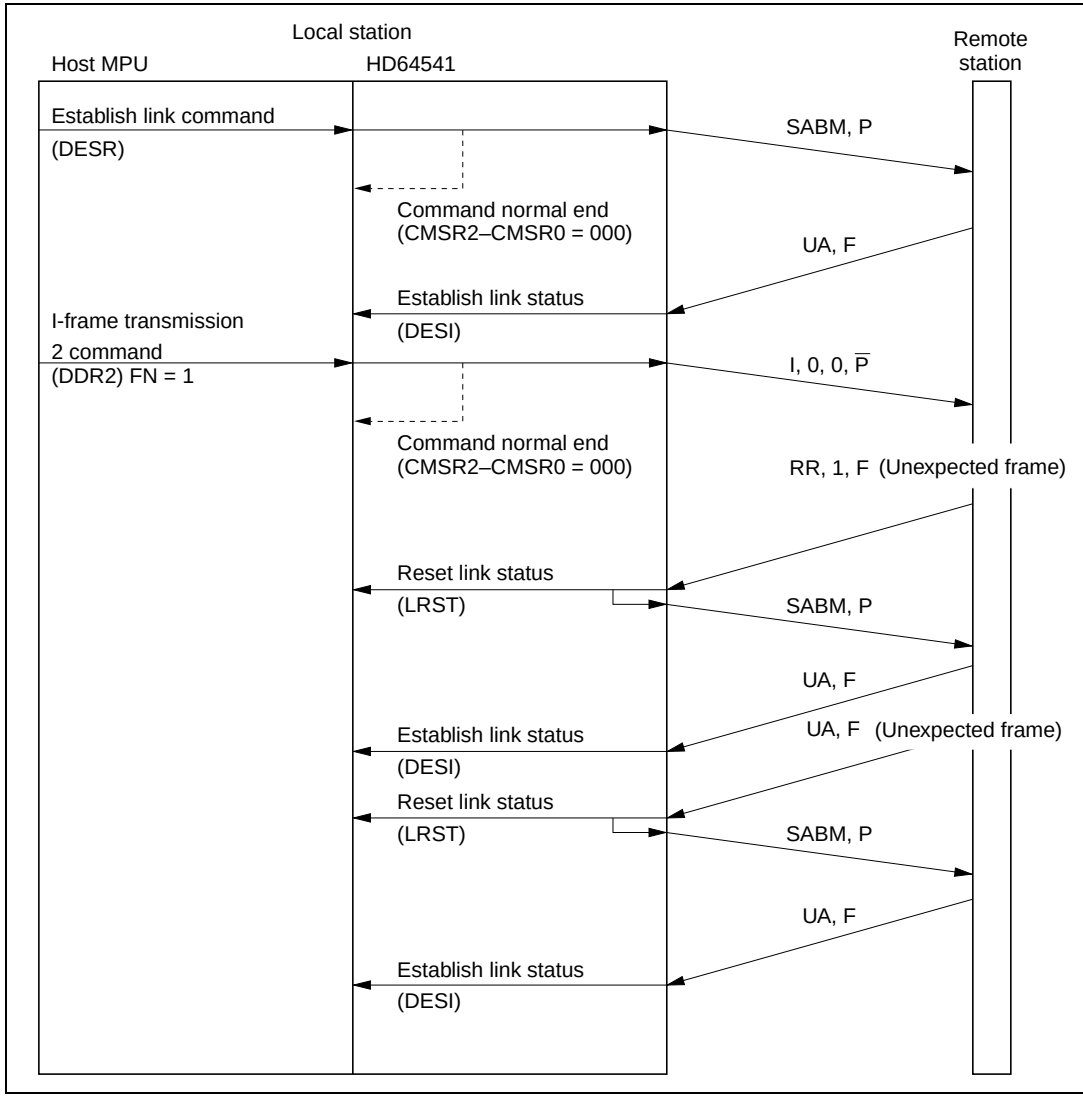


Figure C-10 (a) Reception of Unexpected Frame (X.25 mode)

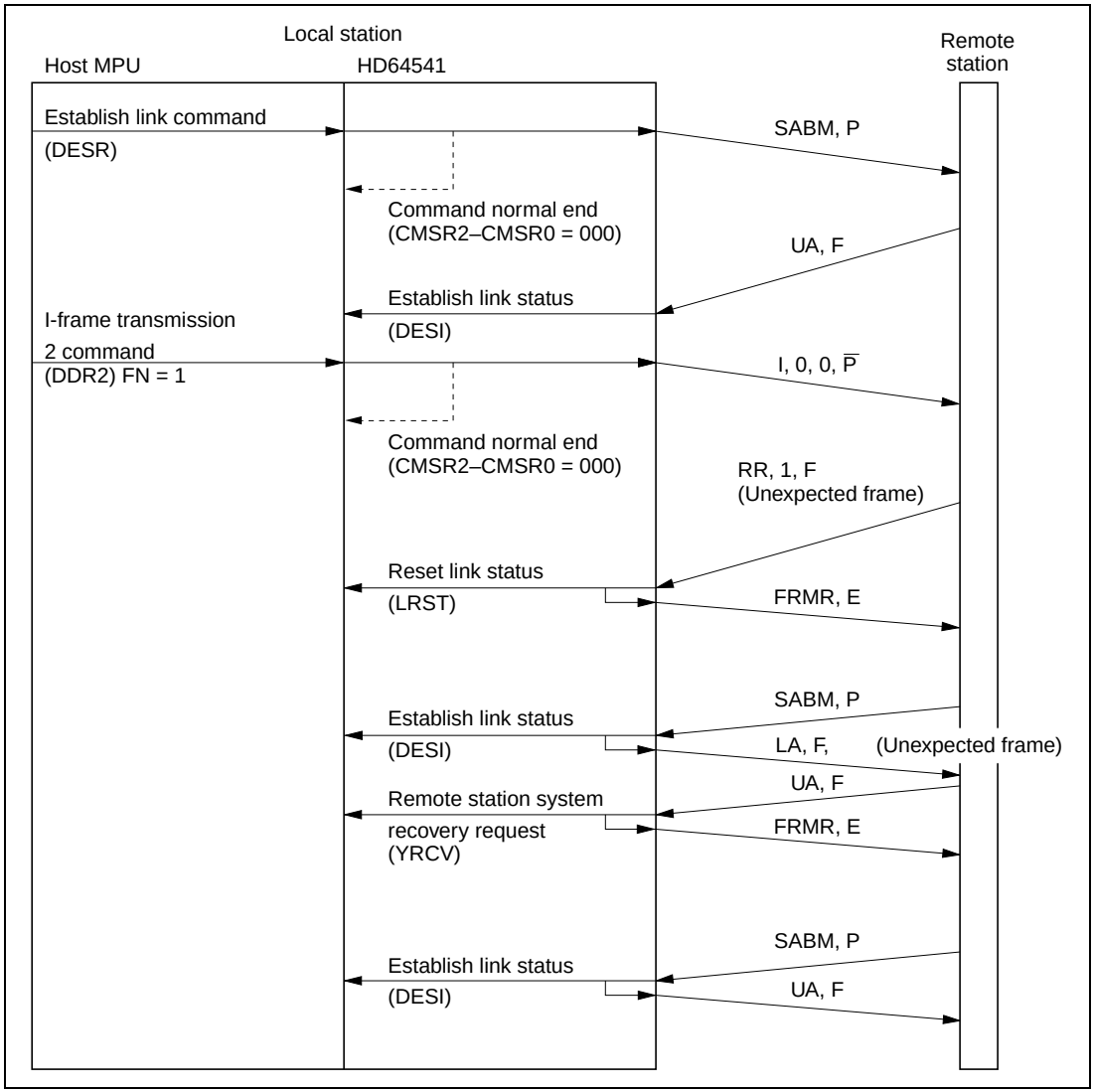


Figure C-10 (b) Reception of Unexpected Frame (X.75 mode)

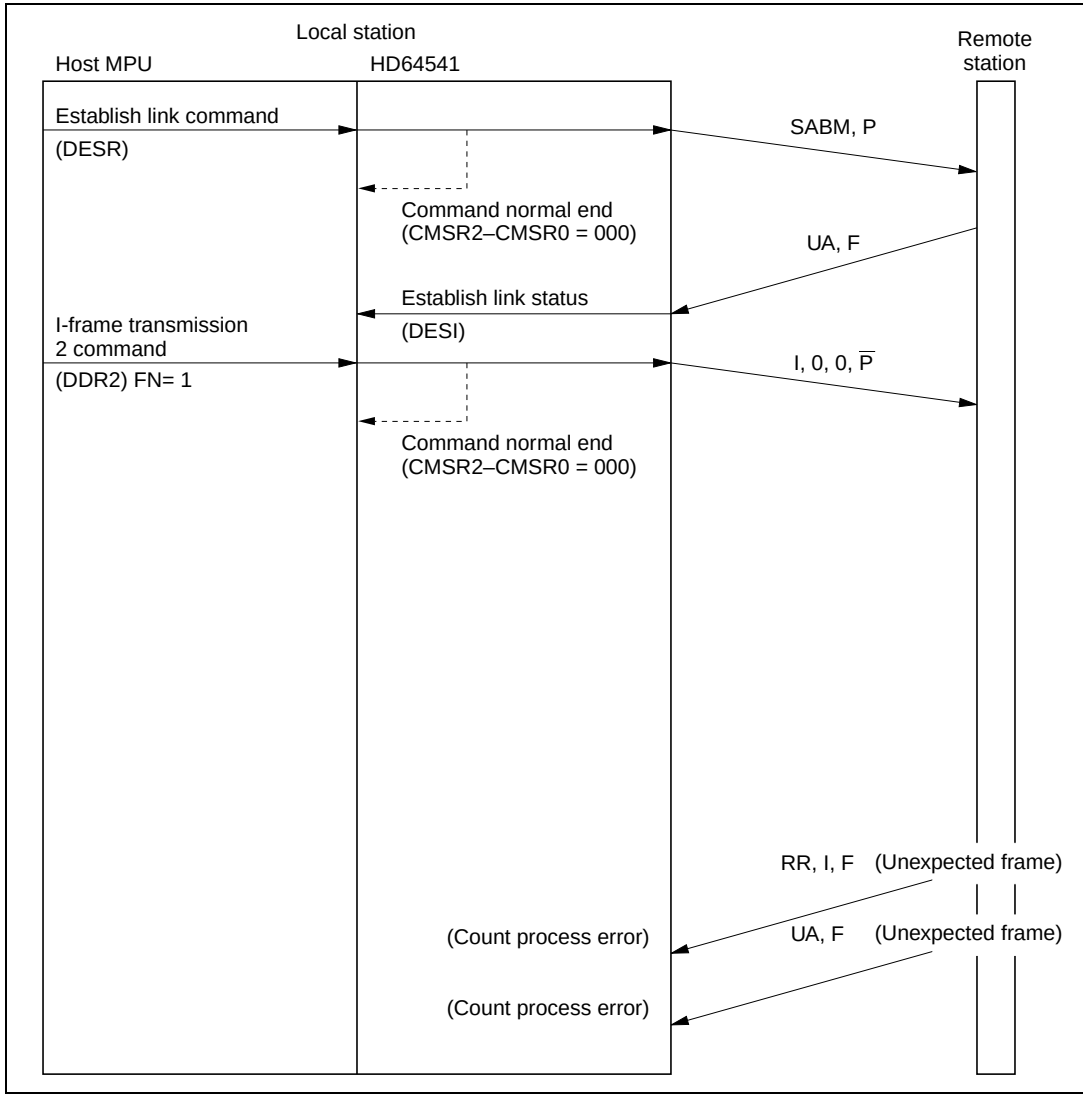


Figure C-10 (c) Reception of Unexpected Frame (T.90 mode)

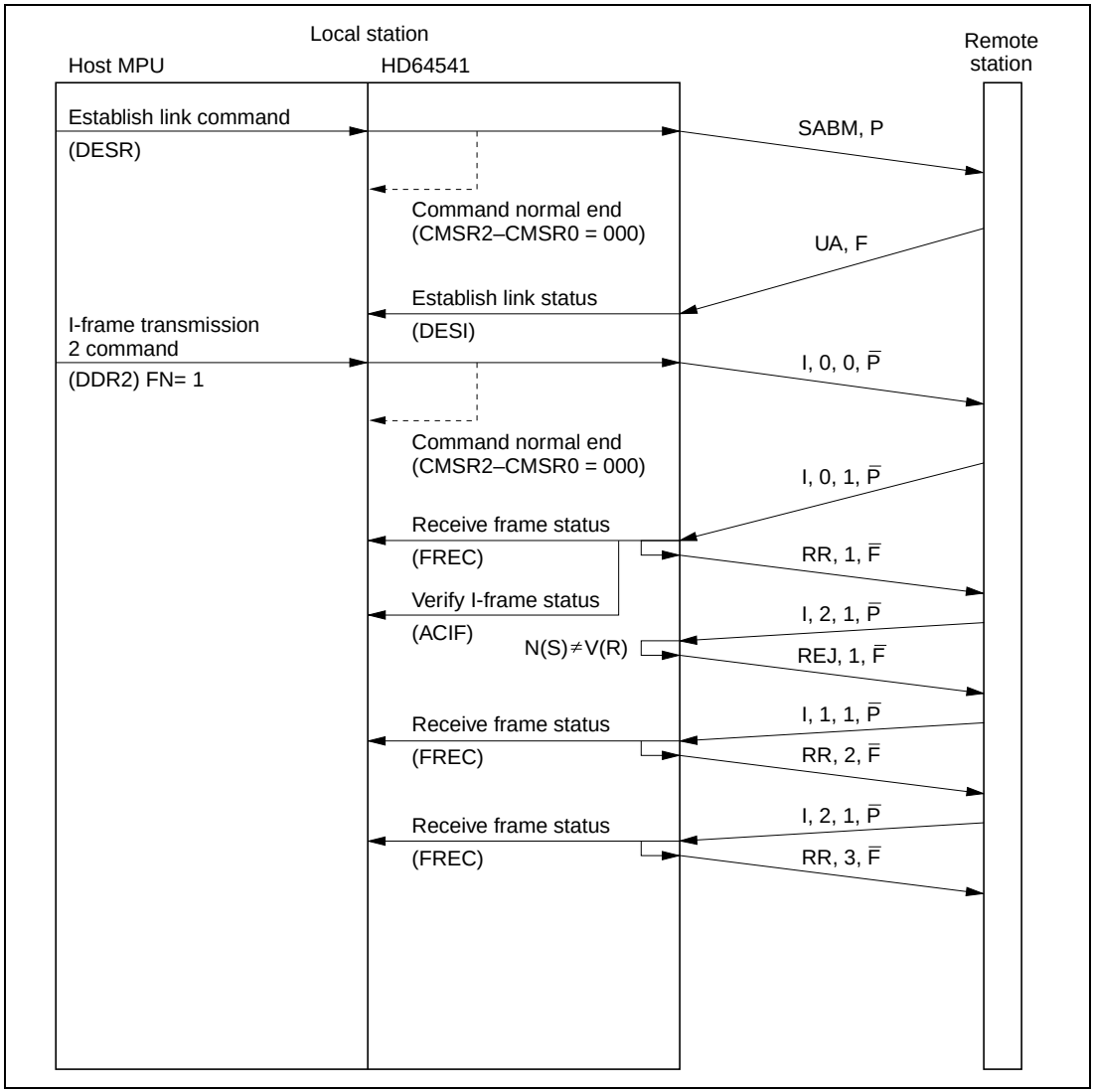


Figure C-11 I-Frame with N(S)≠V(R) Reception

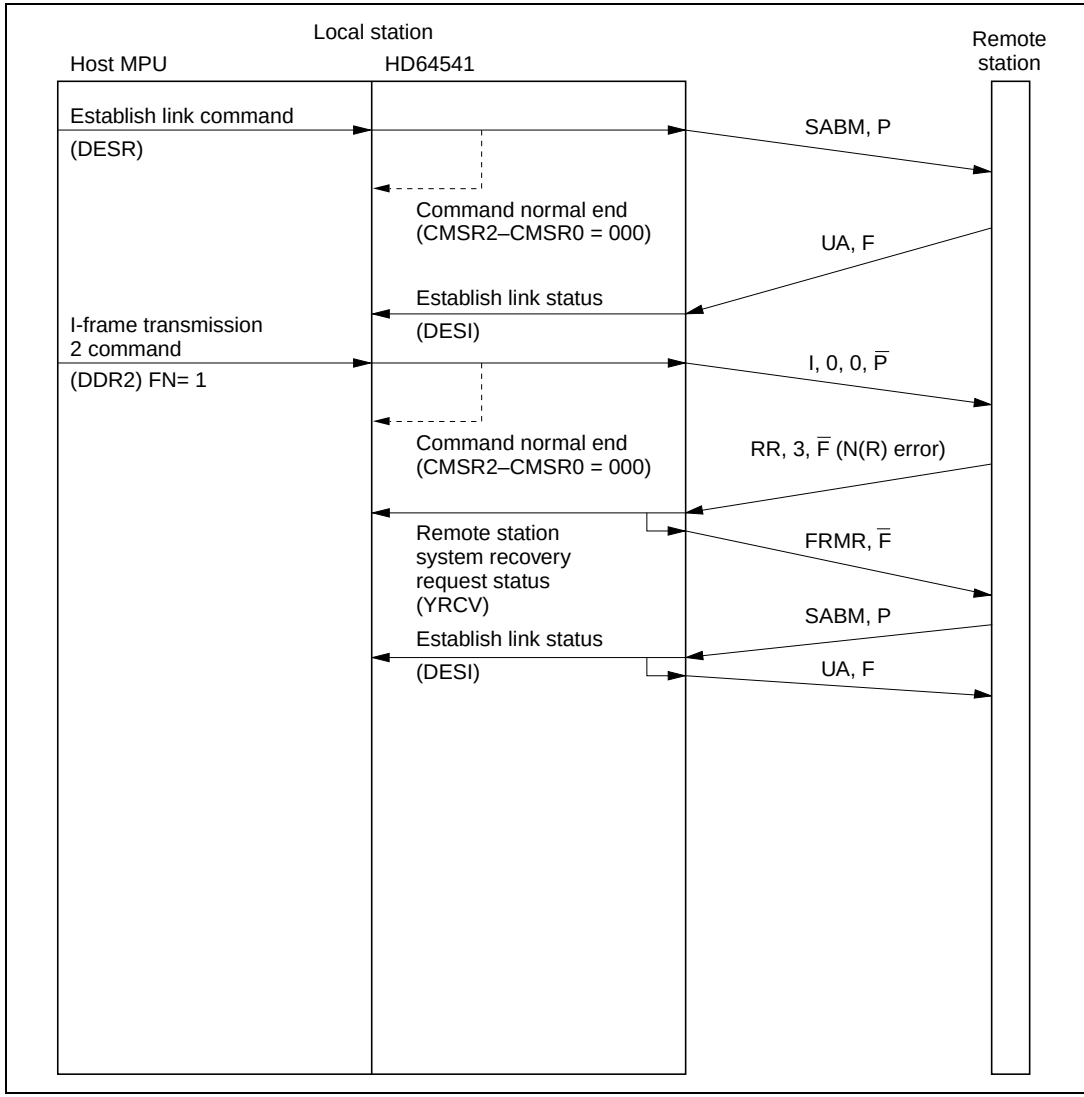


Figure C-12 N(R) Error Frame Reception

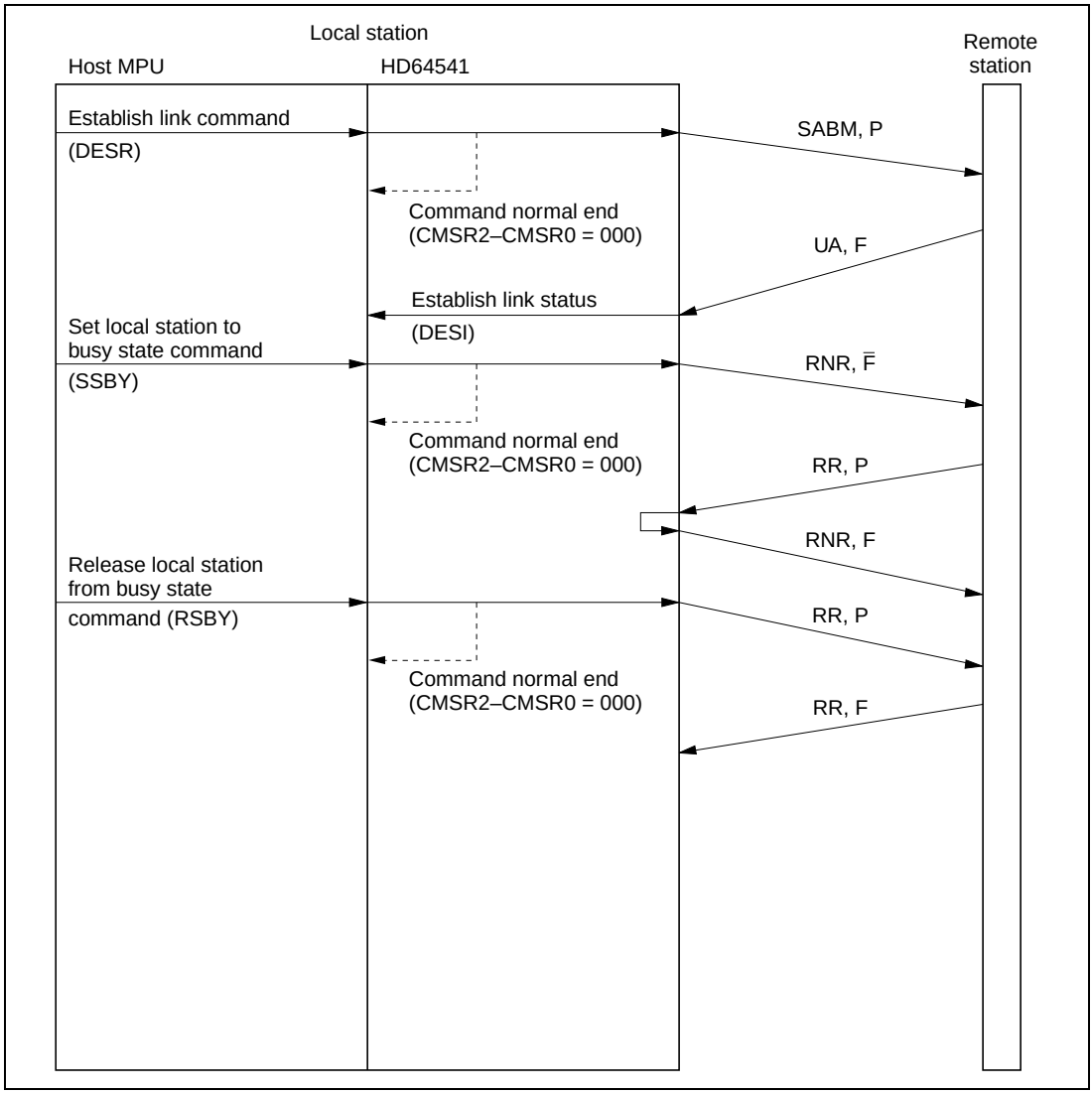


Figure C-13 Local Station Busy Setting/Release

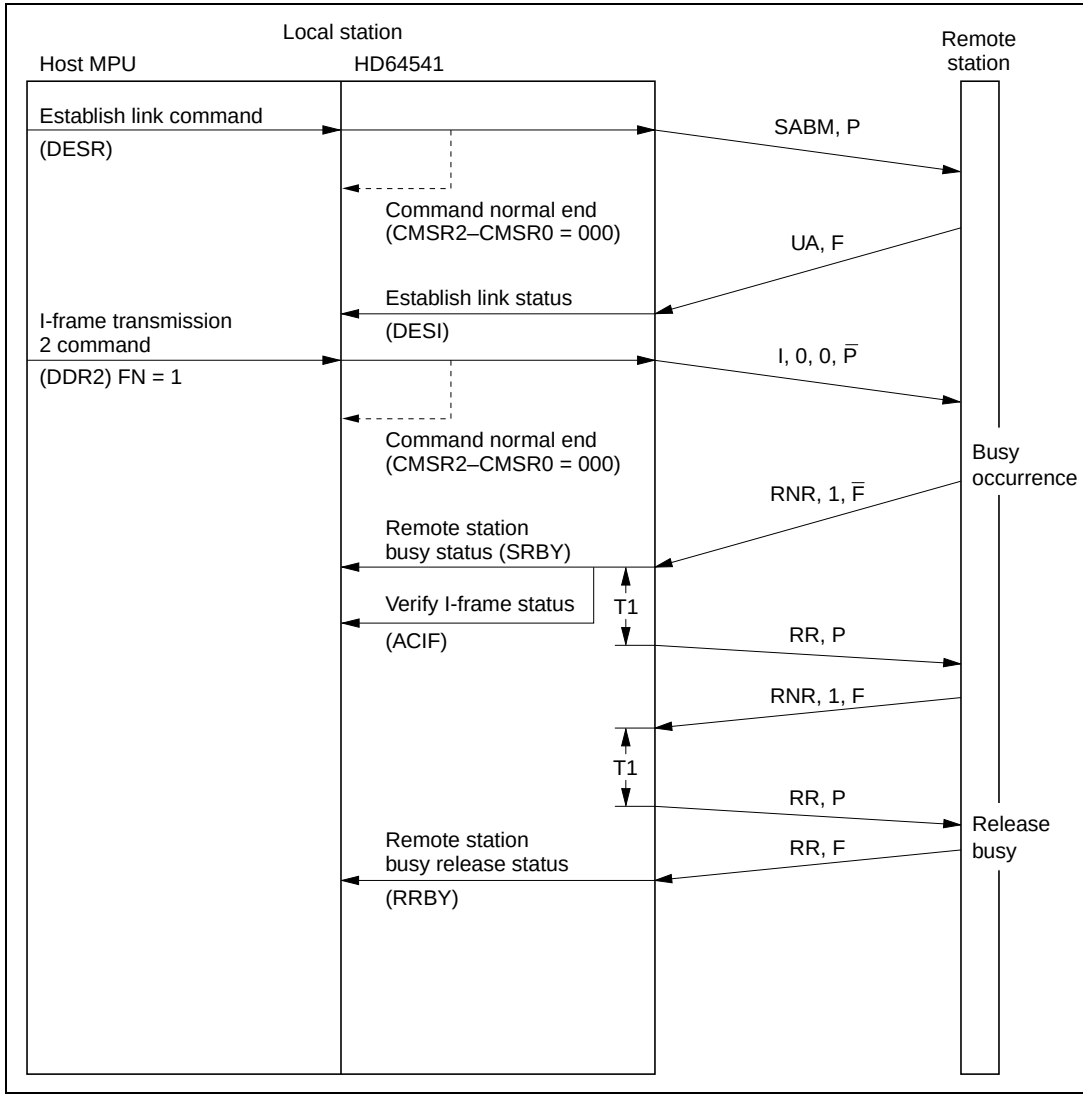


Figure C-14 (a) Remote Station Busy Setting/Release (X.25 and X.75 modes)

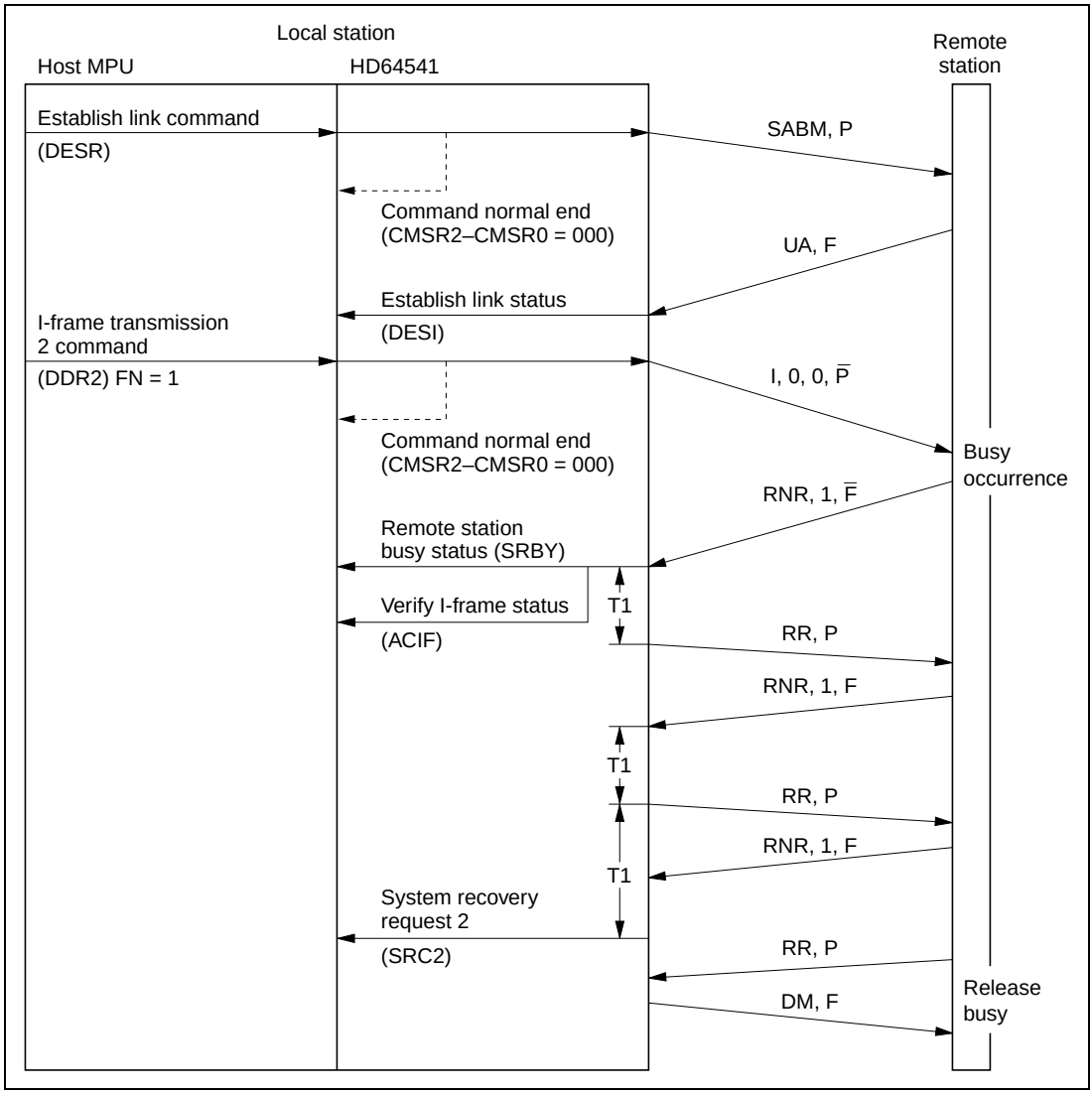


Figure C-14 (b) Remote Station Busy Setting/Release (T.90 mode)

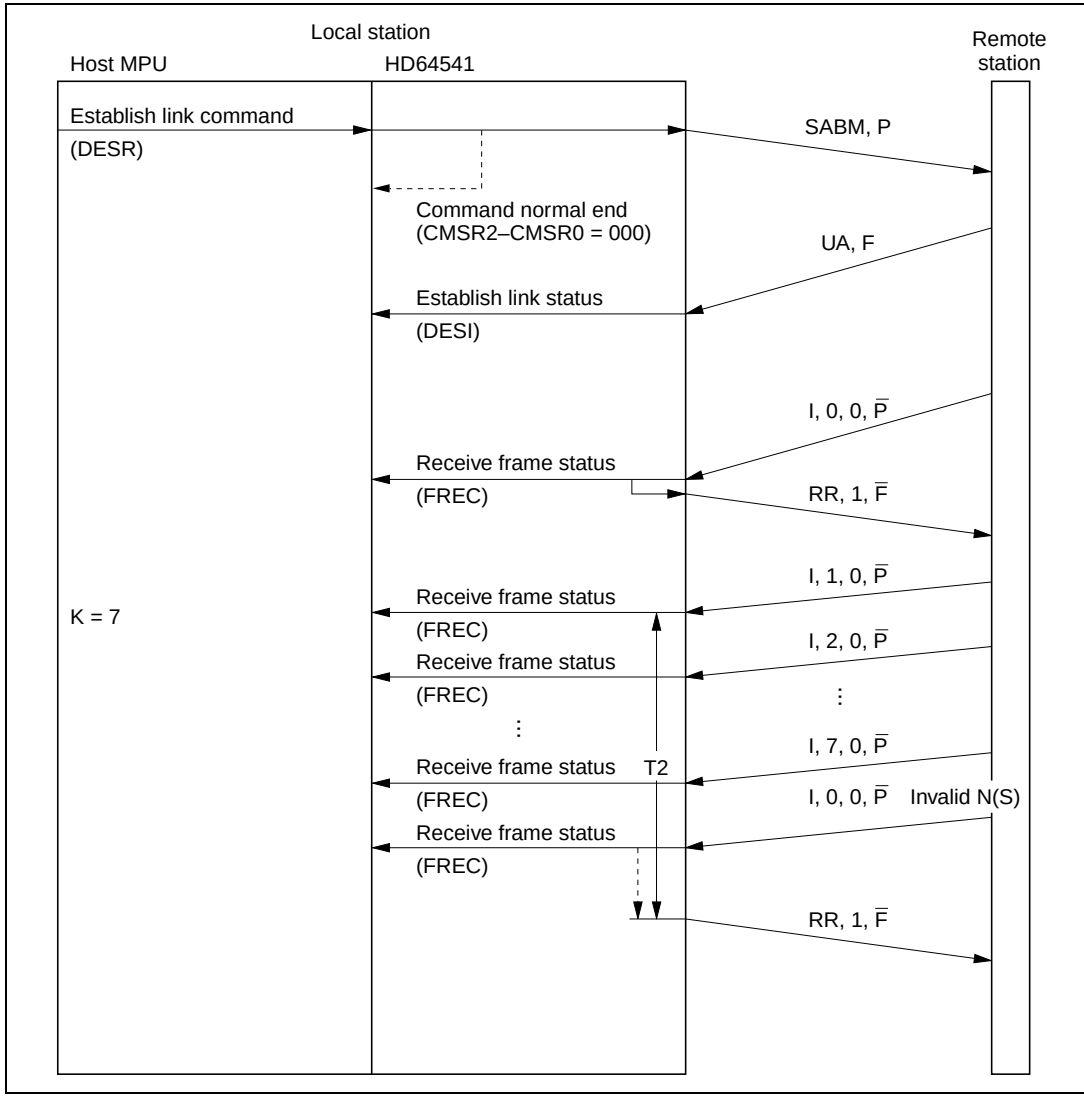


Figure C-15 (a) Reception of I-Frame with Invalid N(S) (X.25 mode)

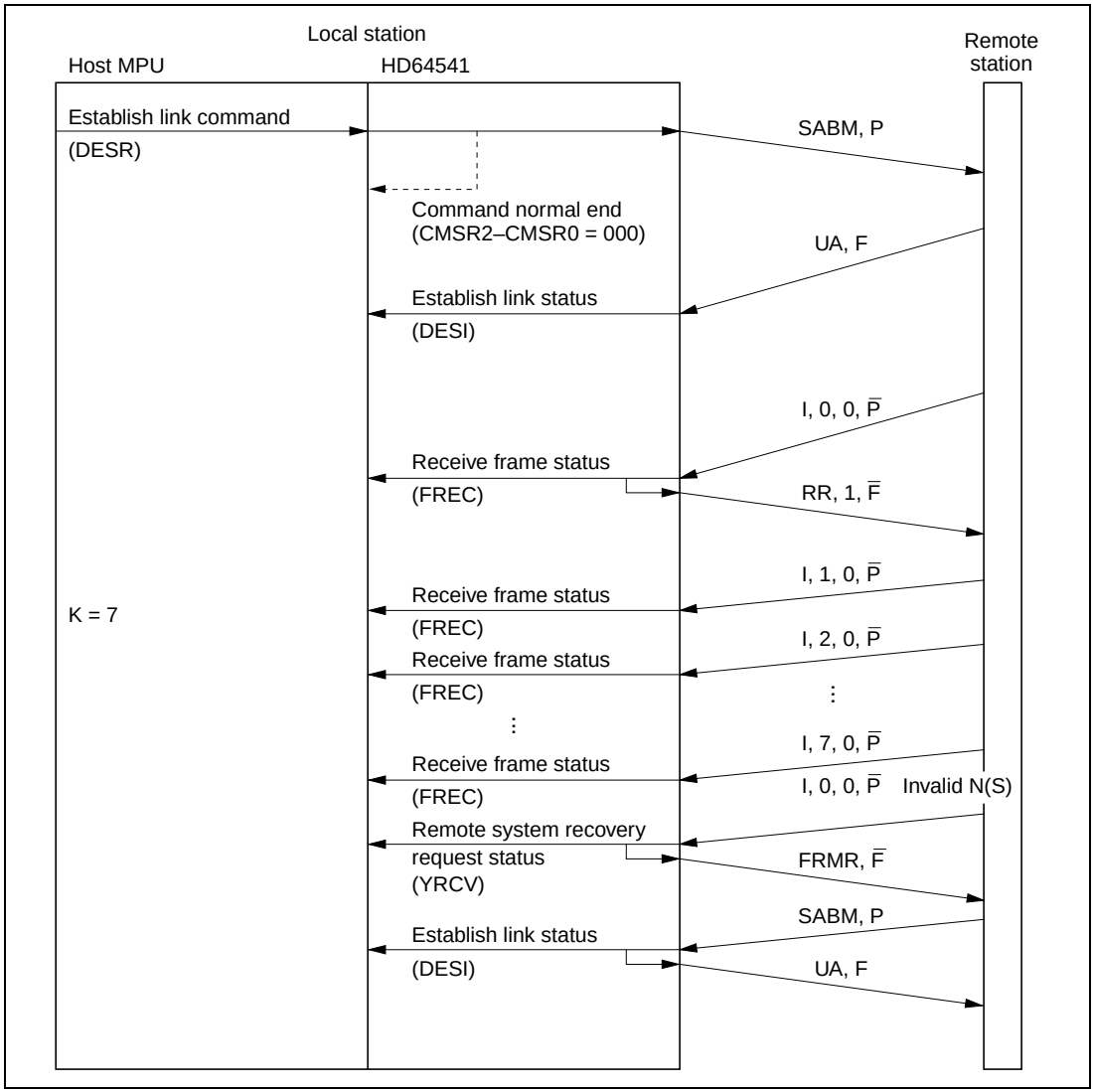


Figure C-15 (b) Reception of I-Frame with Invalid N(S) (X.75 mode)

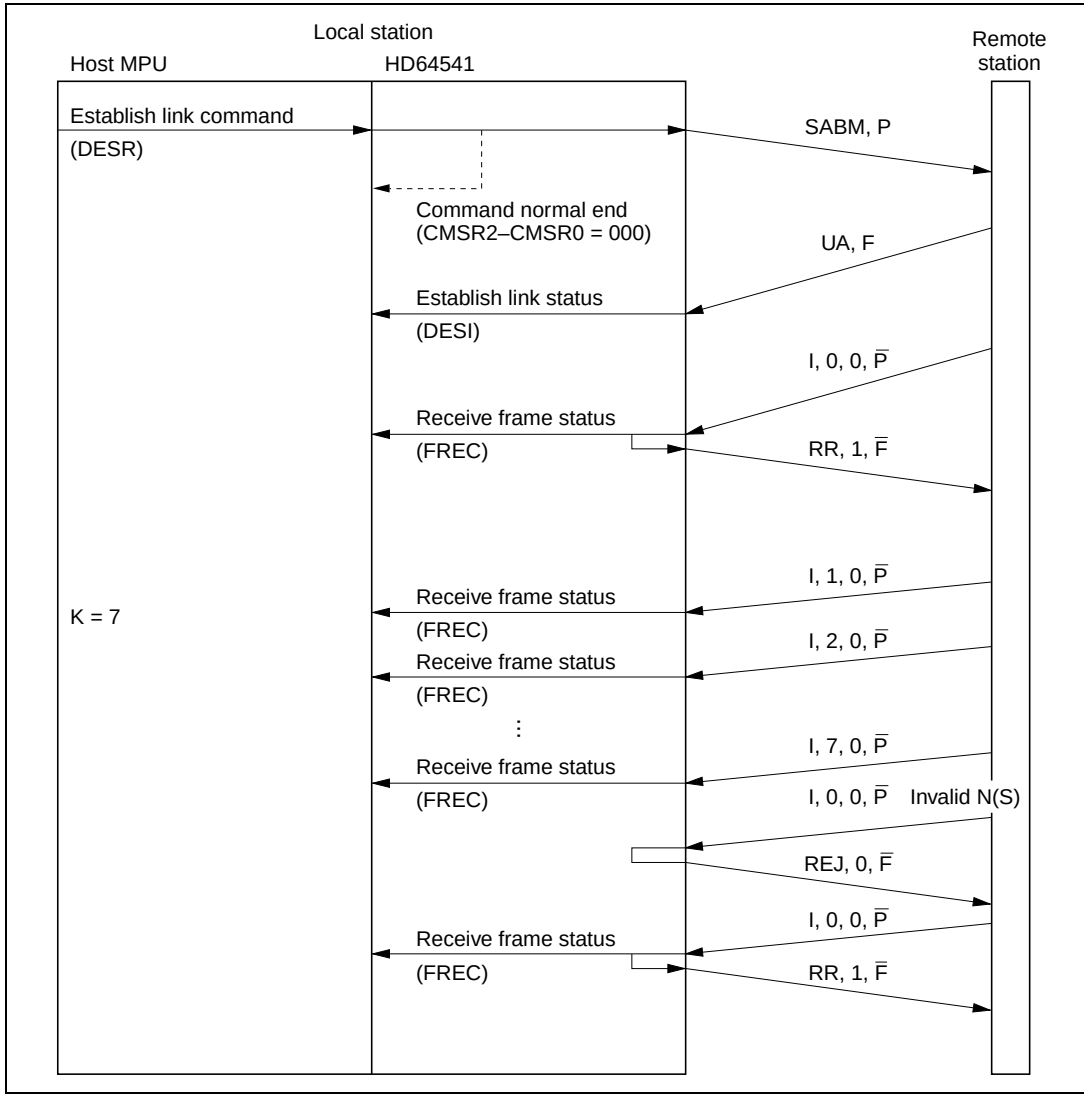


Figure C-15 (c) Reception of I-Frame with Invalid N(S) (T.90 mode)

Table D-1 Link Layer Controller Command Error & Status List

No.	Type	Name	Mnemonic	Protocol	Transparent	Format (HEX)	Format Command parameter #1	Format Command parameter #2	Format Command parameter #3	Reset command waiting	Command LAPB mode Operating mode Off-line	Command LAPB mode Operating mode On-line	Command LAPB mode U, X frame inhibited	Command LAPB mode FN=0, FN≠NSI	Command LAPB mode After SSBY	Command LAPB mode Before SSBY	Command LAPB mode Before DDR2	Command *1	Command Transparent mode Operating mode Off-line	Command Transparent mode Operating mode On-line	Command Transparent mode FN=0, FN≠NSI
1	Structure control	Set area code	STAC	○	○	(00)	A,C :0		A,C :2												
2		Reset	RSET	○	○	(01)															
3		Set operating mode	OMDS	○	○	(02)	M,M,M 2',1',0	Starting address of system parameter table		Format											
4	Maintenance & peripheral control	Control peripheral output pin level	CPOL	○	○	(10)		E, E 1',0	P, P 1',0	Format											
5		Mask information from peripheral input pins	MPIS	○	○	(11)		P', P', P 2, 1, 0		←											
6		Dump system parameter table	DSPT	○	○	(12)		Dump address		←		Format								Format	
7		Dump statistical information	DERC	○	○	(13)		Dump address		←											
8	Transmission control	I-frame transmission 1	DDR1	○		(20)		P	FN	Format		Format			Format			Unexecutable	Unexecutable	Format	Format
9		I-frame transmission 2	DDR2	○	○	(21)		P	FN	←	←				Format			←	←		Format
10		U and X frame transmission	MUDR	○		(22)				←	←		Format							←	Format
11		Suspend frame transmission	SUTD	○	○	(23)				←	←									←	
12		Resume frame transmission	RETD	○	○	(24)				←	←									←	
13		Establish link	DESR	○		(25)				←	←							Unexecutable		←	Format
14		Release link	DRLR	○		(26)				←	←							←		←	←
15		Set local station to busy state	SSBY	○		(27)				←	←				Unexecutable			←		←	←
16		Release local station from busy state	RSBY	○		(28)				←	←					Unexecutable		←		←	←
17		Remote station link establish wait	DESW	○		(29)				←	←							←		←	←
18		Reestablish link	RESR	○		(2A)				←	←							←		←	←

Note: 1. A cannot execute error may sometimes occur depending on the state of the link at the time command is issued.

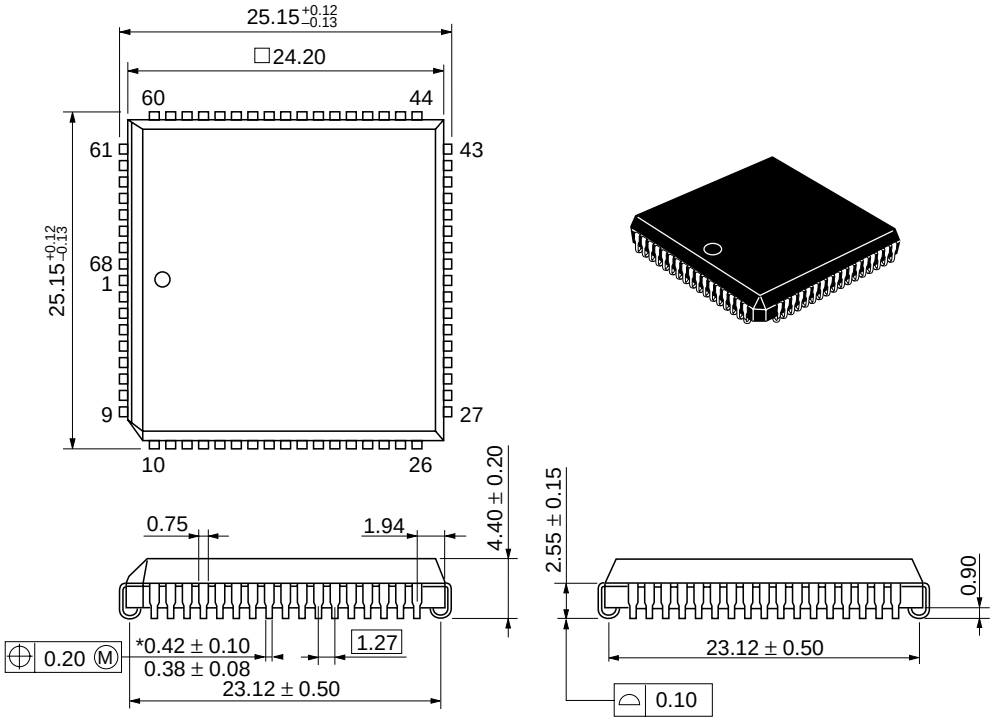
Table D-1 Link Layer Controller Command Error & Status List (cont)

Status								
No.	Name	Mnemonic	Protocol	Transparent	Format (HEX) #0	Status parameter #1	Status parameter #2	Status parameter #3
1	Establish link	DESI	○		(01)			
2	Release link	DRLI	○		(02)			
3	Verify I-frame	ACIF	○		(03)		ASIIN	
4	Remote station busy	SRBY	○		(04)			
5	Remote station busy release	RRBY	○		(05)			
6	Peripheral input pin level	PITL	○	○	(06)		I2, I1, I0	T2, T1, T0
7	Terminate frame transmission	TAIF	○	○	(07)		SIIN	
8	Terminate U and X frame transmission	TAUF	○		(09)		SUXIN	
9	Receive frames	FREC	○	○	(0A)		RBIN	
10	Idle detection	IDET	○	○	(10)			
11	System recovery request 1	SRC1	○		(11)			
12	System recovery request 2	SRC2	○		(12)			
13	Remote station system recovery request	YRCV	○		(13)			
14	Flag synchronization	FSYC	○	○	(14)			
15	Reset link	LRST	○		(16)			

Appendix E Package Dimensions

Package Dimensions

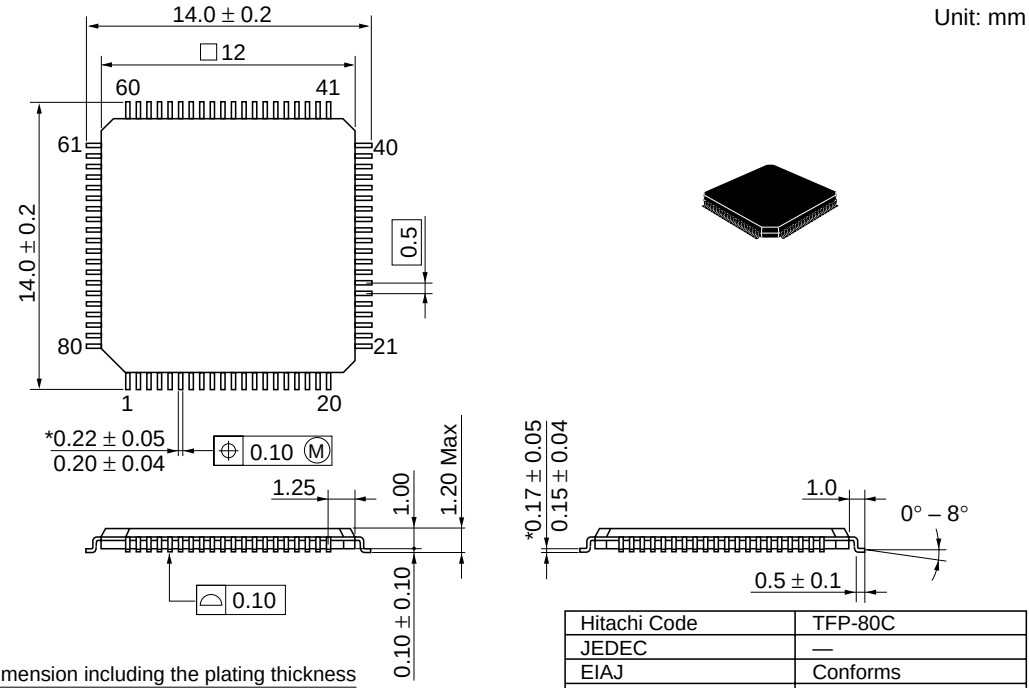
Unit: mm



Hitachi Code	CP-68
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	4.2 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-80C
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.4 g

HD64541 User's Manual

Publication Date: 1st Edition, March 1991
2nd Edition, May 2000
Published by: Electronic Devices Sales & Marketing Group
Semiconductor & Integrated Circuits
Hitachi, Ltd.
Edited by: Technical Documentation Group
Hitachi Kodaira Semiconductor Co., Ltd.