

# MOS INTEGRATED CIRCUIT

## $\mu$ PD42S4210, 424210

### 4 M-BIT DYNAMIC RAM

#### 256K-WORD BY 16-BIT, HYPER PAGE MODE (EDO), BYTE READ/WRITE MODE

#### Description

The  $\mu$ PD42S4210, 424210 are 262,144 words by 16 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the  $\mu$ PD42S4210 can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh.

The  $\mu$ PD42S4210, 424210 are packaged in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.

#### Features

- Hyper page mode (EDO)
- 262,144 words by 16 bits organization
- Single power supply
  - +5.0 V  $\pm$  10 % :  $\mu$ PD42S4210-60-A, 424210-60-A, 42S4210-70, 424210-70
  - +5.0 V  $\pm$  5 % :  $\mu$ PD42S4210-60-G, 424210-60-G

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
$\mu$ PD42S4210-60-A, 424210-60-A	880 mW	60 ns	104 ns	25 ns
$\mu$ PD42S4210-60-G, 424210-60-G	840 mW	60 ns	104 ns	25 ns
$\mu$ PD42S4210-70, 424210-70	825 mW	70 ns	124 ns	30 ns

- The  $\mu$ PD42S4210 can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
$\mu$ PD42S4210-60-A $\mu$ PD42S4210-70	512 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,	0.825 mW (CMOS level input)
$\mu$ PD42S4210-60-G	512 cycles/128 ms	$\overline{\text{RAS}}$ only refresh, Hidden refresh	0.7875 mW (CMOS level input)
$\mu$ PD424210-60-A $\mu$ PD424210-70	512 cycles/8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh,	5.5 mW (CMOS level input)
$\mu$ PD424210-60-G	512 cycles/8 ms	Hidden refresh	5.25 mW (CMOS level input)

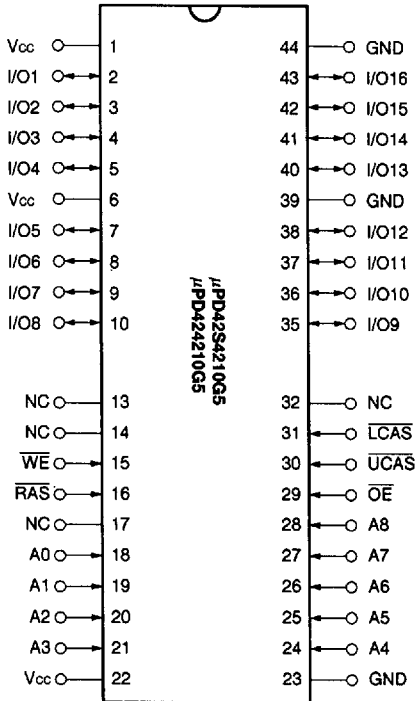
The information in this document is subject to change without notice.

Ordering Information

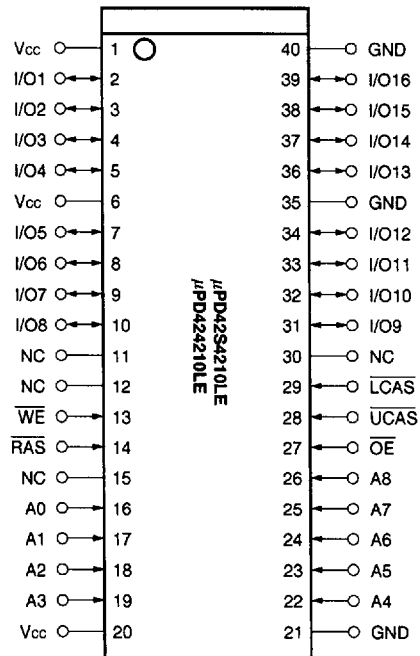
Part number	Access time (MAX.)	Package	Refresh
μPD42S4210G5-60-A	60	44-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
μPD42S4210G5-60-G	60		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μPD42S4210G5-70	70		$\overline{\text{RAS}}$ only refresh
μPD42S4210LE-60-A	60	40-pin plastic SOJ (400 mil)	Hidden refresh
μPD42S4210LE-60-G	60		
μPD42S4210LE-70	70		
μPD424210G5-60-A	60	44-pin plastic TSOP(II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μPD424210G5-60-G	60		$\overline{\text{RAS}}$ only refresh
μPD424210G5-70	70		Hidden refresh
μPD424210LE-60-A	60	40-pin plastic SOJ (400 mil)	
μPD424210LE-60-G	60		
μPD424210LE-70	70		

Pin Configurations (Marking Side)

44-pin Plastic TSOP (II) (400 mil)

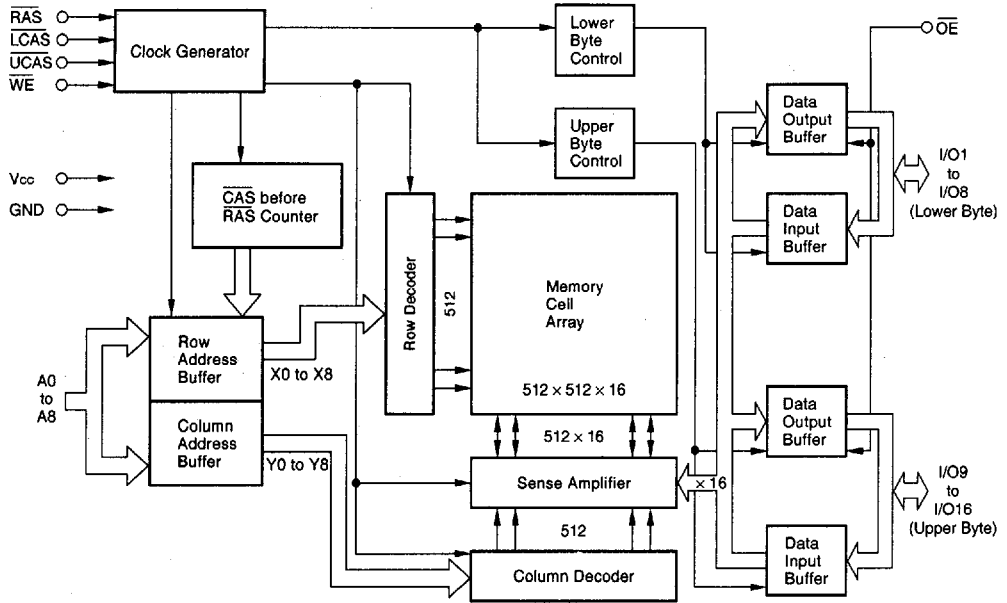


40-pin Plastic SOJ (400 mil)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$  : Row Address Strobe
- $\overline{\text{UCAS}}$  : Column Address Strobe (upper)
- $\overline{\text{LCAS}}$  : Column Address Strobe (lower)
- $\overline{\text{WE}}$  : Write Enable
- $\overline{\text{OE}}$  : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



**Input/Output Pin Functions**

The μPD42S4210, 424210 have input pins  $\overline{RAS}$ ,  $\overline{CAS}$ <sup>Note</sup>,  $\overline{WE}$ ,  $\overline{OE}$ , A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	Address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262,144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$ . Then, switch the address bus to column address and activate $\overline{CAS}$ . Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time ( $t_{ASR}$ , $t_{ASC}$ ) and hold time ( $t_{RAH}$ , $t_{CAH}$ ) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$ .
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ .
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{OE}$ . If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

**Note**  $\overline{CAS}$  means  $\overline{UCAS}$  and  $\overline{LCAS}$ .

**Hyper Page Mode (EDO)**

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

**1. Data output time is extended.**

In the hyper page mode (EDO), the output data is held to the next  $\overline{\text{CAS}}$  cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the  $\overline{\text{CAS}}$  cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the  $\overline{\text{CAS}}$  cycle time becomes shorter.

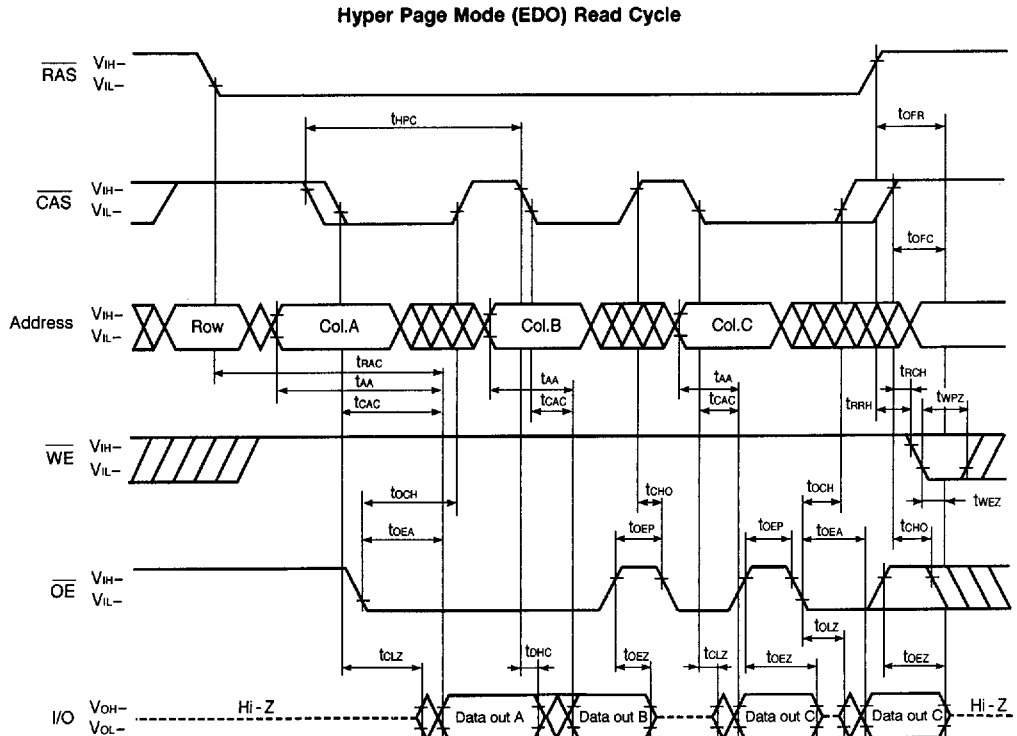
**2. The  $\overline{\text{CAS}}$  cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**

In the hyper page mode (EDO), due to the data extend function, the  $\overline{\text{CAS}}$  cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose  $t_{\text{rAC}}$  is 60 ns as an example, the  $\overline{\text{CAS}}$  cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one  $\overline{\text{RAS}}$  cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.



**Cautions when using the hyper page mode (EDO)**

1.  $\overline{\text{CAS}}$  access should be used to operate  $t_{\text{HPC}}$  at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  as follows. The effective specification depends on the state of each signal.
  - (1) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive (at the end of read cycle)  
 $\overline{\text{WE}}$ : inactive,  $\overline{\text{OE}}$ : active  
 $t_{\text{OFC}}$  is effective when  $\overline{\text{RAS}}$  is inactivated before  $\overline{\text{CAS}}$  is inactivated.  
 $t_{\text{OFF}}$  is effective when  $\overline{\text{CAS}}$  is inactivated before  $\overline{\text{RAS}}$  is inactivated.
  - (2) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are active or either  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  is active (in read cycle)  
 $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : inactive .....  $t_{\text{OEZ}}$  is effective.
  - (3) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive or  $\overline{\text{RAS}}$  is active and  $\overline{\text{CAS}}$  is inactive (at the end of read cycle)  
 $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : active and either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be met .....  $t_{\text{WEZ}}$  and  $t_{\text{WPZ}}$  are effective.
3. In read cycle, the effective specification depends on the state of  $\overline{\text{CAS}}$  signal when controlling data output with the  $\overline{\text{OE}}$  signal.
  - (1)  $\overline{\text{CAS}}$ : inactive,  $\overline{\text{OE}}$ : active .....  $t_{\text{CHO}}$  is effective.
  - (2)  $\overline{\text{CAS}}$ ,  $\overline{\text{OE}}$ : active .....  $t_{\text{OCH}}$  is effective.

**Electrical Specifications**

- $\overline{\text{CAS}}$  means  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
- All voltages are referenced to GND.
- After power up ( $V_{\text{CC}} \geq V_{\text{CC(MIN.)}}$ ), wait more than 100 μs ( $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  inactive) and then, execute eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$  only refresh cycles as dummy cycles to initialize internal circuit.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	$V_T$		-1.0 to +7.0	V
Supply voltage	$V_{\text{CC}}$		-1.0 to +7.0	V
Output current	$I_O$		50	mA
Power dissipation	$P_D$		1	W
Operating ambient temperature	$T_A$		0 to +70	°C
Storage temperature	$T_{\text{stg}}$		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{\text{CC}}$	μPD42S4210-60-A, 424210-60-A	4.5	5.0	5.5	V
		μPD42S4210-70, 424210-70				
		μPD42S4210-60-G, 424210-60-G	4.75	5.0	5.25	
High level input voltage	$V_{\text{IH}}$		2.4		$V_{\text{CC}} + 1.0$	V
Low level input voltage	$V_{\text{IL}}$		-1.0		+0.8	V
Operating ambient temperature	$T_A$		0		70	°C

**Capacitance ( $T_A = 25\text{ °C}$ ,  $f = 1\text{ MHz}$ )**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{I1}$	Address			5	pF
	$C_{I2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

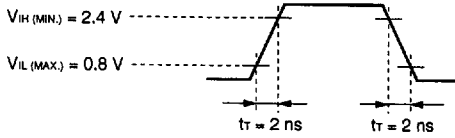
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I <sub>CC1</sub>	$\overline{RAS}, \overline{CAS}$ cycling	tr <sub>AC</sub> = 60 ns	160	mA	1, 2, 3
			tr <sub>C</sub> = tr <sub>C(MIN.)</sub> , I <sub>O</sub> = 0 mA	tr <sub>AC</sub> = 70 ns	150		
Standby current	μPD42S4210	I <sub>CC2</sub>	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}$ , I <sub>O</sub> = 0 mA		2.0	mA	
			$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 V$ , I <sub>O</sub> = 0 mA		0.15		
	μPD424210	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}$ , I <sub>O</sub> = 0 mA		2.0			
		$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 V$ , I <sub>O</sub> = 0 mA		1.0			
RAS only refresh current		I <sub>CC3</sub>	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH(MIN.)}$	tr <sub>AC</sub> = 60 ns	160	mA	1, 2, 3, 4
			tr <sub>C</sub> = tr <sub>C(MIN.)</sub> , I <sub>O</sub> = 0 mA	tr <sub>AC</sub> = 70 ns	150		
Operating current (Hyper page mode (EDO))		I <sub>CC4</sub>	$\overline{RAS} \leq V_{IL(MAX.)}$ , $\overline{CAS}$ cycling	tr <sub>AC</sub> = 60 ns	160	mA	1, 2, 5
			th <sub>PC</sub> = th <sub>PC(MIN.)</sub> , I <sub>O</sub> = 0 mA	tr <sub>AC</sub> = 70 ns	150		
CAS before RAS refresh current		I <sub>CC5</sub>	$\overline{RAS}$ cycling	tr <sub>AC</sub> = 60 ns	160	mA	1, 2
			tr <sub>C</sub> = tr <sub>C(MIN.)</sub> , I <sub>O</sub> = 0 mA	tr <sub>AC</sub> = 70 ns	150		
CAS before RAS long refresh current (512 cycles / 128 ms, only for the μPD42S4210)		I <sub>CC6</sub>	CAS before RAS refresh: tr <sub>C</sub> = 250.0 μs RAS, CAS: $V_{CC} - 0.2 V \leq V_{IH} \leq V_{IH(MAX.)}$ $0 V \leq V_{IL} \leq 0.2 V$	tr <sub>AS</sub> ≤ 200 ns	200	μA	1, 2
			Standby: $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 V$ Address: V <sub>IH</sub> or V <sub>IL</sub> $\overline{WE}, \overline{OE}$ : V <sub>IH</sub> I <sub>O</sub> = 0 mA	tr <sub>AS</sub> ≤ 1 μs	300	μA	1, 2
CAS before RAS self refresh current (only for the μPD42S4210)		I <sub>CC7</sub>	$\overline{RAS}, \overline{CAS}$ : tr <sub>AS</sub> = 5 ms $V_{CC} - 0.2 V \leq V_{IH} \leq V_{IH(MAX.)}$ $0 V \leq V_{IL} \leq 0.2 V$ I <sub>O</sub> = 0 mA		150	μA	2
Input leakage current		I <sub>I(L)</sub>	V <sub>I</sub> = 0 to 5.5 V	μPD42S4210-60-A, 424210-60-A μPD42S4210-70, 424210-70	-10	+10	μA
			V <sub>I</sub> = 0 to 5.25 V	μPD42S4210-60-G, 424210-60-G			
			All other pins not under test = 0 V				
Output leakage current		I <sub>O(L)</sub>	V <sub>O</sub> = 0 to 5.5 V	μPD42S4210-60-A, 424210-60-A μPD42S4210-70, 424210-70	-10	+10	μA
			V <sub>O</sub> = 0 to 5.25 V	μPD42S4210-60-G, 424210-60-G			
			Output in disabled (Hi-Z)				
High level output voltage		V <sub>OH</sub>	I <sub>O</sub> = -5.0 mA	μPD42S4210-60-A, 424210-60-A μPD42S4210-70, 424210-70	2.4		V
			I <sub>O</sub> = -0.1 mA	μPD42S4210-60-G, 424210-60-G			
Low level output voltage		V <sub>OL</sub>	I <sub>O</sub> = +4.2 mA	μPD42S4210-60-A, 424210-60-A μPD42S4210-70, 424210-70		0.4	V
			I <sub>O</sub> = +0.1 mA	μPD42S4210-60-G, 424210-60-G			

- Notes**
1.  $t_{CC1}$ ,  $t_{CC3}$ ,  $t_{CC4}$ ,  $t_{CC5}$  and  $t_{CC6}$  depend on cycle rates ( $t_{RC}$  and  $t_{HPC}$ ).
  2. Specified values are obtained with outputs unloaded.
  3.  $t_{CC1}$  and  $t_{CC3}$  are measured assuming that address can be changed once or less during  $\overline{RAS} \leq V_{IL (MAX.)}$  and  $\overline{CAS} \geq V_{IH (MIN.)}$ .
  4.  $t_{CC3}$  is measured assuming that all column address inputs are held at either high or low.
  5.  $t_{CC4}$  is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

**AC Characteristics (Recommended Operating Conditions unless otherwise noted)**

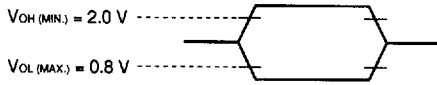
**AC Characteristics Test Conditions**

(1) Input timing specification

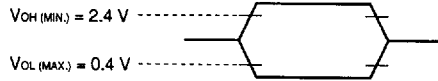


(2) Output timing specification

- $\mu$ PD42S4210-60-A, 424210-60-A

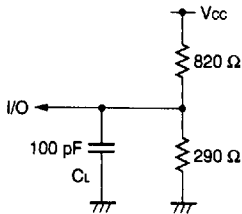


- $\mu$ PD42S4210-60-G, 424210-60-G
- $\mu$ PD424210-70, 424210-70

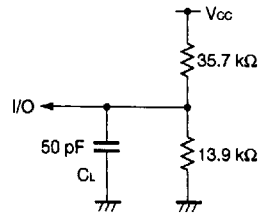


(3) Output loading conditions

- $\mu$ PD42S4210-60-A, 424210-60-A
- $\mu$ PD42S4210-70, 424210-70



- $\mu$ PD42S4210-60-G, 424210-60-G



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t <sub>TRAC</sub> = 60 ns		t <sub>TRAC</sub> = 70 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.			
Read / Write cycle time	t <sub>RC</sub>	104	—	124	—	ns		
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	40	—	50	—	ns		
$\overline{\text{CAS}}$ precharge time	t <sub>CPN</sub>	10	—	10	—	ns		
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	60	10,000	70	10,000	ns	1	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	10	10,000	12	10,000	ns		
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	10	—	12	—	ns		
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	40	—	50	—	ns		
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RC</sub>	14	45	14	50	ns	2	
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	12	30	12	35	ns	2	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	5	—	5	—	ns	3	
Row address setup time	t <sub>ASR</sub>	0	—	0	—	ns		
Row address hold time	t <sub>RAH</sub>	10	—	10	—	ns		
Column address setup time	t <sub>ASC</sub>	0	—	0	—	ns		
Column address hold time	t <sub>CAH</sub>	10	—	12	—	ns		
$\overline{\text{OE}}$ lead time referenced to $\overline{\text{RAS}}$	t <sub>OES</sub>	0	—	0	—	ns		
$\overline{\text{CAS}}$ to data setup time	t <sub>CLZ</sub>	0	—	0	—	ns		
$\overline{\text{OE}}$ to data setup time	t <sub>OLZ</sub>	0	—	0	—	ns		
$\overline{\text{OE}}$ to data delay time	t <sub>OED</sub>	13	—	15	—	ns		
Masked byte write hold time referenced to $\overline{\text{RAS}}$	t <sub>MRH</sub>	0	—	0	—	ns		
Transition time (rise and fall)	t <sub>r</sub>	1	50	1	50	ns		
Refresh time	μPD42S4210	t <sub>REF</sub>	—	128	—	128	ms	4
	μPD424210		—	8	—	8	ms	

- Notes**
- In  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles, t<sub>TRAS(MAX.)</sub> is 100 μs.  
If 10 μs ≤ t<sub>TRAS</sub> < 100 μs,  $\overline{\text{RAS}}$  precharge time for  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh (t<sub>RP</sub>) is applied.
  - For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
t <sub>TRAD</sub> ≤ t <sub>TRAD (MAX.)</sub> and t <sub>TRCD</sub> ≤ t <sub>TRCD (MAX.)</sub>	t <sub>TRAC (MAX.)</sub>	t <sub>TRAC (MAX.)</sub>
t <sub>TRAD</sub> > t <sub>TRAD (MAX.)</sub> and t <sub>TRCD</sub> ≤ t <sub>TRCD (MAX.)</sub>	t <sub>TA</sub> (MAX.)	t <sub>TRAD</sub> + t <sub>TA</sub> (MAX.)
t <sub>TRCD</sub> > t <sub>TRCD (MAX.)</sub>	t <sub>TCAC (MAX.)</sub>	t <sub>TRCD</sub> + t <sub>TCAC (MAX.)</sub>

t<sub>TRAD (MAX.)</sub> and t<sub>TRCD (MAX.)</sub> are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t<sub>TRAC</sub>, t<sub>TA</sub> or t<sub>TCAC</sub>) is to be used for finding out when output data will be available. Therefore, the input conditions t<sub>TRAD</sub> ≥ t<sub>TRAD (MAX.)</sub> and t<sub>TRCD</sub> ≥ t<sub>TRCD (MAX.)</sub> will not cause any operation problems.

- t<sub>CRP (MIN.)</sub> requirement is applied to  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycles.
- This specification is applied only to the μPD42S4210.

Read Cycle

Parameter	Symbol	t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t <sub>RAC</sub>	-	60	-	70	ns	1
Access time from $\overline{CAS}$	t <sub>CAC</sub>	-	15	-	20	ns	1
Access time from column address	t <sub>AA</sub>	-	30	-	35	ns	1
Access time from $\overline{OE}$	t <sub>OEA</sub>	-	15	-	20	ns	
Column address lead time referenced to $\overline{RAS}$	t <sub>RAL</sub>	30	-	35	-	ns	
Read command setup time	t <sub>RCS</sub>	0	-	0	-	ns	
Read command hold time referenced to $\overline{RAS}$	t <sub>RRH</sub>	0	-	0	-	ns	2
Read command hold time referenced to $\overline{CAS}$	t <sub>RCH</sub>	0	-	0	-	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t <sub>OEZ</sub>	0	15	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t <sub>CHO</sub>	5	-	5	-	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
t <sub>RAD</sub> ≤ t <sub>RAD</sub> (MAX.) and t <sub>RCD</sub> ≤ t <sub>RCD</sub> (MAX.)	t <sub>RAC</sub> (MAX.)	t <sub>RAC</sub> (MAX.)
t <sub>RAD</sub> > t <sub>RAD</sub> (MAX.) and t <sub>RCD</sub> ≤ t <sub>RCD</sub> (MAX.)	t <sub>AA</sub> (MAX.)	t <sub>RAD</sub> + t <sub>AA</sub> (MAX.)
t <sub>RCD</sub> > t <sub>RCD</sub> (MAX.)	t <sub>CAC</sub> (MAX.)	t <sub>RCD</sub> + t <sub>CAC</sub> (MAX.)

t<sub>RAD</sub>(MAX.) and t<sub>RCD</sub>(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t<sub>RAC</sub>, t<sub>AA</sub> or t<sub>CAC</sub>) is to be used for finding out when output data will be available. Therefore, the input conditions t<sub>RAD</sub> ≥ t<sub>RAD</sub>(MAX.) and t<sub>RCD</sub> ≥ t<sub>RCD</sub>(MAX.) will not cause any operation problems.

2. Either t<sub>RCH</sub>(MIN.) or t<sub>RRH</sub>(MIN.) should be met in read cycles.
3. t<sub>OEZ</sub>(MAX.) defines the time when the output achieves the condition of Hi-Z and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.

**Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	twch	10	-	10	-	ns	1
$\overline{WE}$ pulse width	twp	10	-	10	-	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	trwl	10	-	12	-	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	tcwl	10	-	12	-	ns	
$\overline{WE}$ setup time	twcs	0	-	0	-	ns	2
$\overline{OE}$ hold time	toeh	0	-	0	-	ns	
Data-in setup time	t <sub>DS</sub>	0	-	0	-	ns	3
Data-in hold time	t <sub>DH</sub>	10	-	10	-	ns	3

- Notes**
1. t<sub>WP(MIN.)</sub> is applied to late write cycles or read modify write cycles. In early write cycles, t<sub>WCH(MIN.)</sub> should be met.
  2. If t<sub>WCS</sub> ≥ t<sub>WCS(MIN.)</sub>, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
  3. t<sub>DS(MIN.)</sub> and t<sub>DH(MIN.)</sub> are referenced to the  $\overline{CAS}$  falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the  $\overline{WE}$  falling edge.

**Read Modify Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	trwc	133	-	157	-	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	trwd	77	-	89	-	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	tcwd	32	-	37	-	ns	1
Column address to $\overline{WE}$ delay time	tawd	47	-	54	-	ns	1

- Note**
1. If t<sub>WCS</sub> ≥ t<sub>WCS(MIN.)</sub>, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>TRWD</sub> ≥ t<sub>TRWD(MIN.)</sub>, t<sub>TCWD</sub> ≥ t<sub>TCWD(MIN.)</sub>, t<sub>TAWD</sub> ≥ t<sub>TAWD(MIN.)</sub> and t<sub>TCPWD</sub> ≥ t<sub>TCPWD(MIN.)</sub>, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t <sub>TRAC</sub> = 60 ns		t <sub>TRAC</sub> = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t <sub>HPC</sub>	25	—	30	—	ns	1
$\overline{\text{RAS}}$ pulse width	t <sub>RASP</sub>	60	125,000	70	125,000	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>HGAS</sub>	10	10,000	12	10,000	ns	
$\overline{\text{CAS}}$ precharge time	t <sub>CP</sub>	10	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>ACP</sub>	—	35	—	40	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t <sub>CPWD</sub>	52	—	59	—	ns	2
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t <sub>RHCP</sub>	35	—	40	—	ns	
Read modify write cycle time	t <sub>HPRWC</sub>	66	—	75	—	ns	
Data output hold time	t <sub>DHC</sub>	5	—	5	—	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t <sub>OCH</sub>	5	—	5	—	ns	4
$\overline{\text{OE}}$ precharge time	t <sub>OEP</sub>	5	—	5	—	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	t <sub>WEZ</sub>	0	13	0	15	ns	3,4
$\overline{\text{WE}}$ pulse width	t <sub>WPZ</sub>	10	—	10	—	ns	4
Output buffer turn-off delay from $\overline{\text{RAS}}$	t <sub>FR</sub>	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{\text{CAS}}$	t <sub>FC</sub>	0	13	0	15	ns	3,4

- Notes**
- t<sub>HPC</sub> (MIN.) is applied to  $\overline{\text{CAS}}$  access.
  - If t<sub>WCs</sub> ≥ t<sub>WCs</sub> (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>RWD</sub> ≥ t<sub>RWD</sub> (MIN.), t<sub>CPWD</sub> ≥ t<sub>CPWD</sub> (MIN.), t<sub>AWD</sub> ≥ t<sub>AWD</sub> (MIN.) and t<sub>CPWD</sub> ≥ t<sub>CPWD</sub> (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
  - t<sub>OFC</sub> (MAX.), t<sub>OFR</sub> (MAX.) and t<sub>WEZ</sub> (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
  - To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  as follows. The effective specification depends on state of each signal.
    - Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive (at the end of the read cycle)  
 $\overline{\text{WE}}$ : inactive,  $\overline{\text{OE}}$ : active  
 t<sub>OFC</sub> is effective when  $\overline{\text{RAS}}$  is inactivated before  $\overline{\text{CAS}}$  is inactivated.  
 t<sub>OFR</sub> is effective when  $\overline{\text{CAS}}$  is inactivated before  $\overline{\text{RAS}}$  is inactivated.
    - Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are active or either  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  is active (in read cycle)  
 $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : inactive ..... t<sub>WEZ</sub> is effective.
    - Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are inactive or  $\overline{\text{RAS}}$  is active and  $\overline{\text{CAS}}$  is inactive (at the end of read cycle)  
 $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : active and either t<sub>TRH</sub> or t<sub>TRCH</sub> must be met ..... t<sub>WEZ</sub> and t<sub>WPZ</sub> are effective.
    - $\overline{\text{WE}}$ : inactive (in read cycle)  
 $\overline{\text{CAS}}$ : inactive,  $\overline{\text{OE}}$ : active ..... t<sub>CHO</sub> is effective.  
 $\overline{\text{CAS}}$ ,  $\overline{\text{OE}}$ : active ..... t<sub>OCH</sub> is effective.

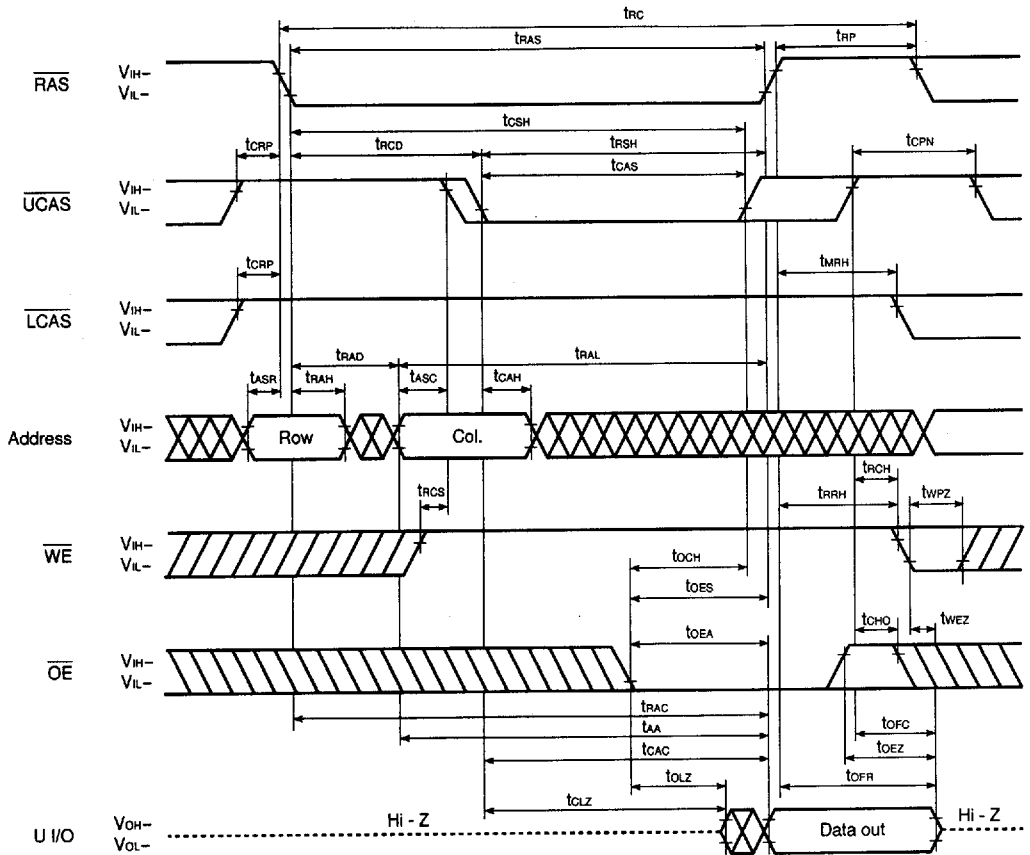
Refresh Cycle

Parameter	Symbol	t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
CAS setup time	t <sub>CSR</sub>	5	-	5	-	ns	
CAS hold time (CAS before RAS refresh)	t <sub>CHR</sub>	10	-	10	-	ns	
RAS precharge CAS hold time	t <sub>RPC</sub>	5	-	5	-	ns	
RAS pulse width (CAS before RAS self refresh)	t <sub>RASS</sub>	100	-	100	-	μs	1
RAS precharge time (CAS before RAS self refresh)	t <sub>RPS</sub>	110	-	130	-	ns	1
CAS hold time (CAS before RAS self refresh)	t <sub>CHS</sub>	-50	-	-50	-	ns	1
WE hold time	t <sub>WHR</sub>	15	-	15	-	ns	

**Note 1.** This specification is applied only to the μPD42S4210.

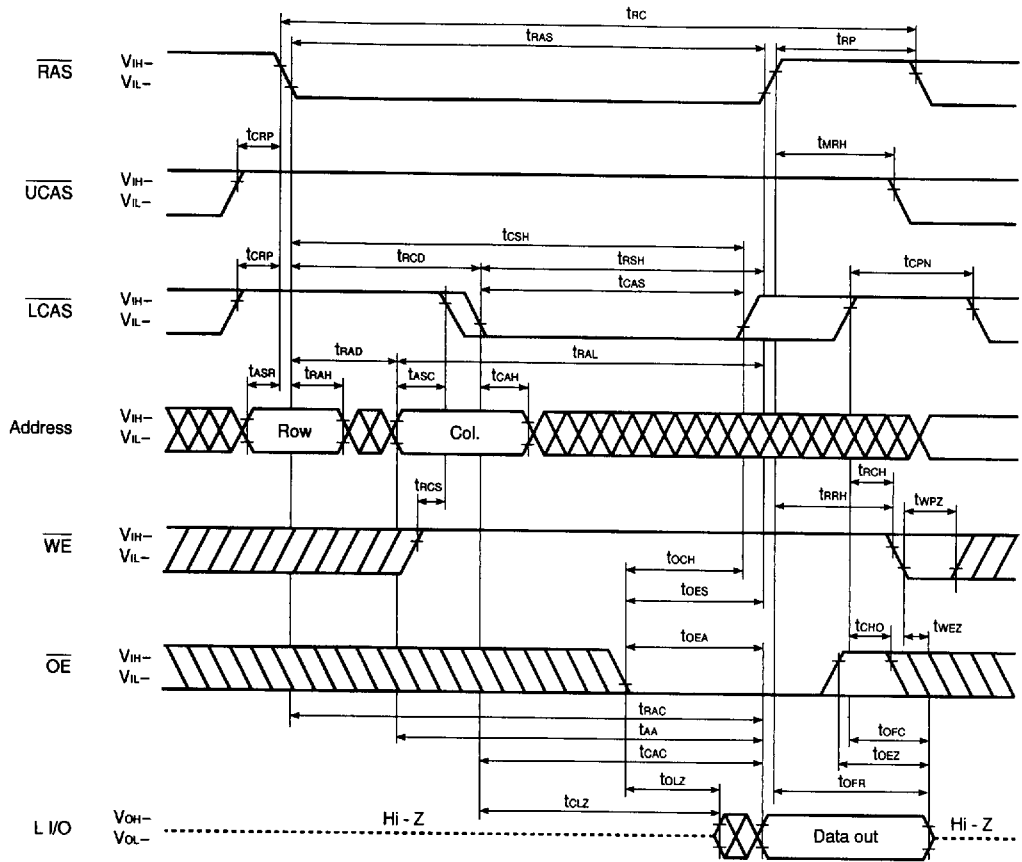


Upper Byte Read Cycle



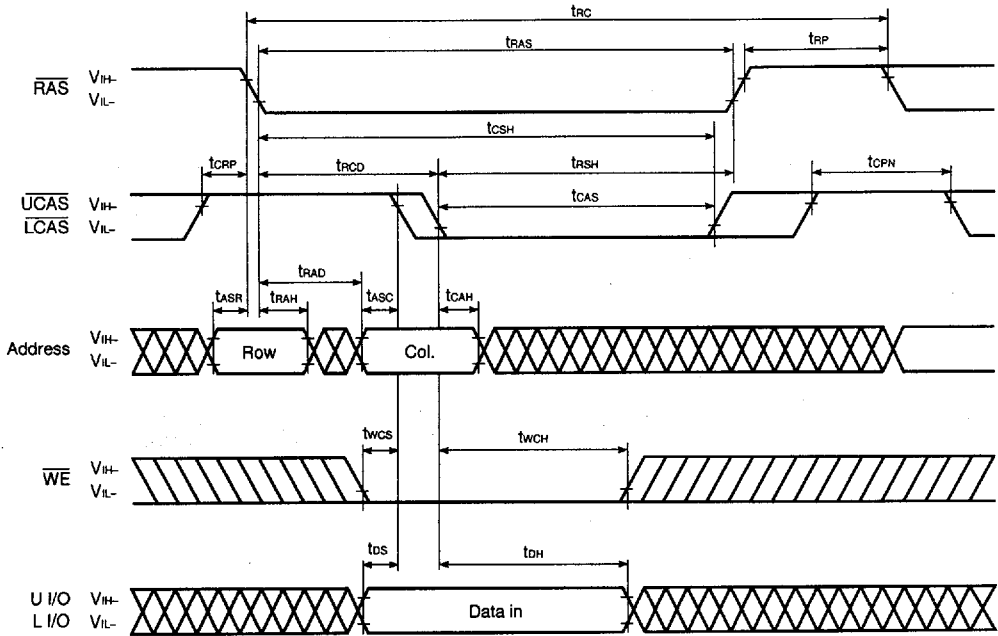
Remark L I/O: Hi-Z

Lower Byte Read Cycle



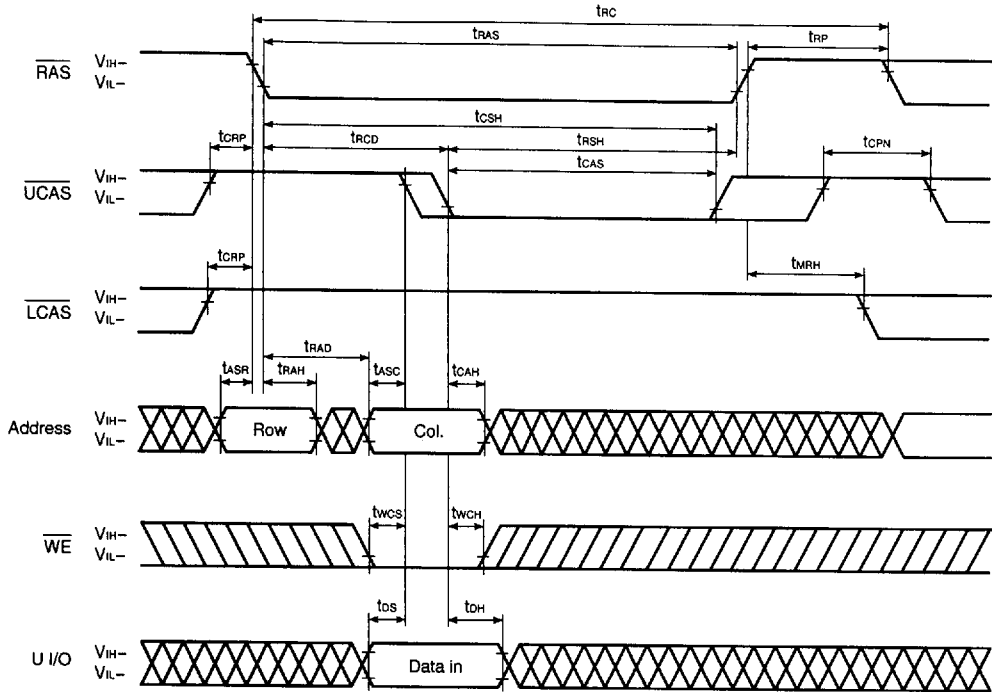
Remark U I/O: Hi-Z

Early Write Cycle



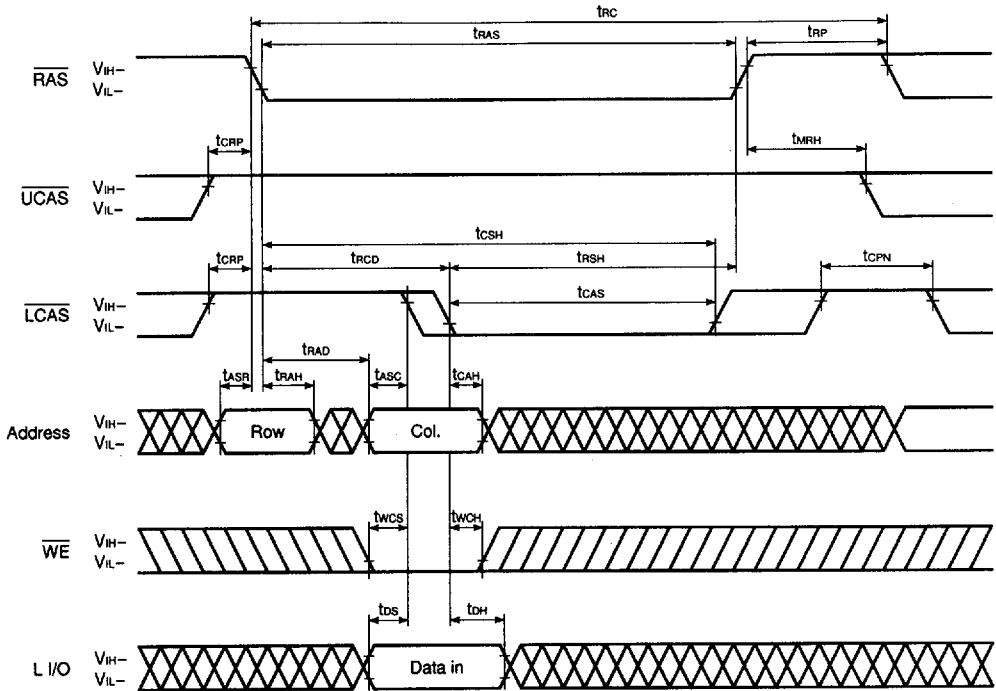
Remark  $\overline{\text{OE}}$ : Don't care

Upper Byte Early Write Cycle



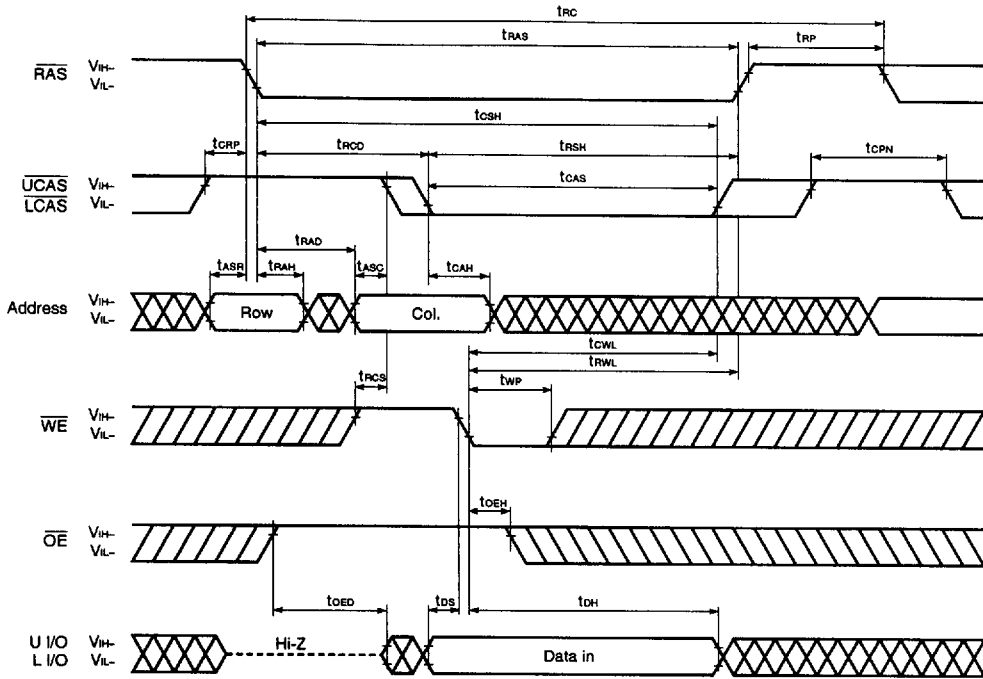
Remark  $\overline{OE}$ , L I/O: Don't care

Lower Byte Early Write Cycle

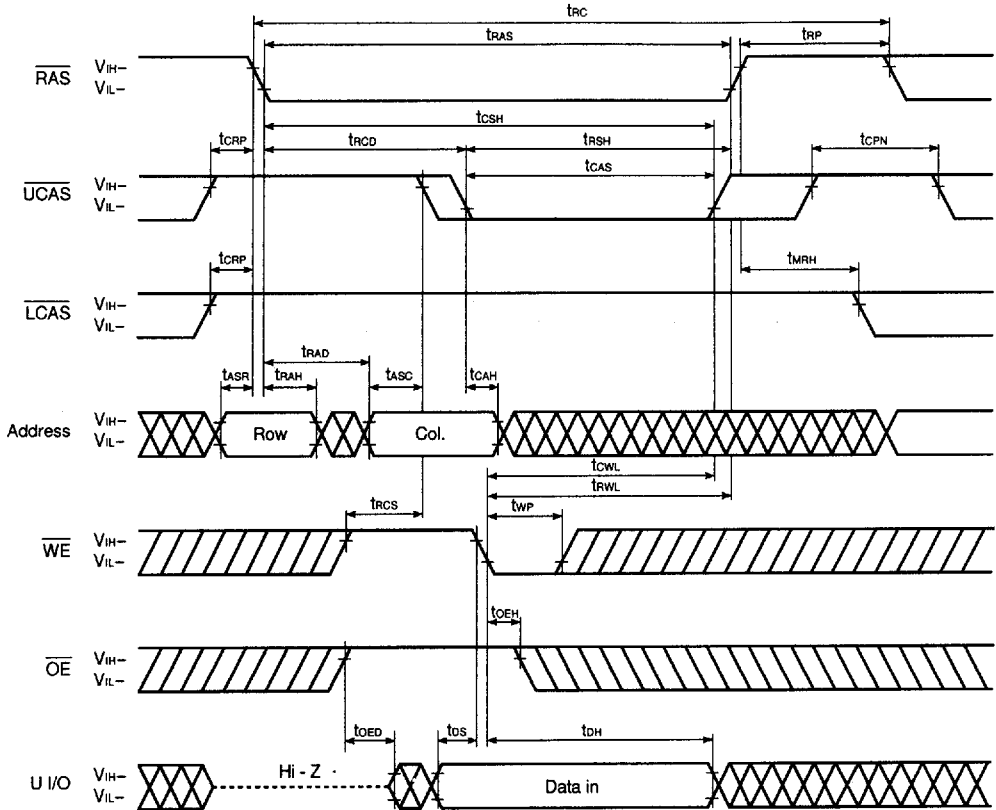


Remark  $\overline{OE}$ , U I/O: Don't care

Late Write Cycle

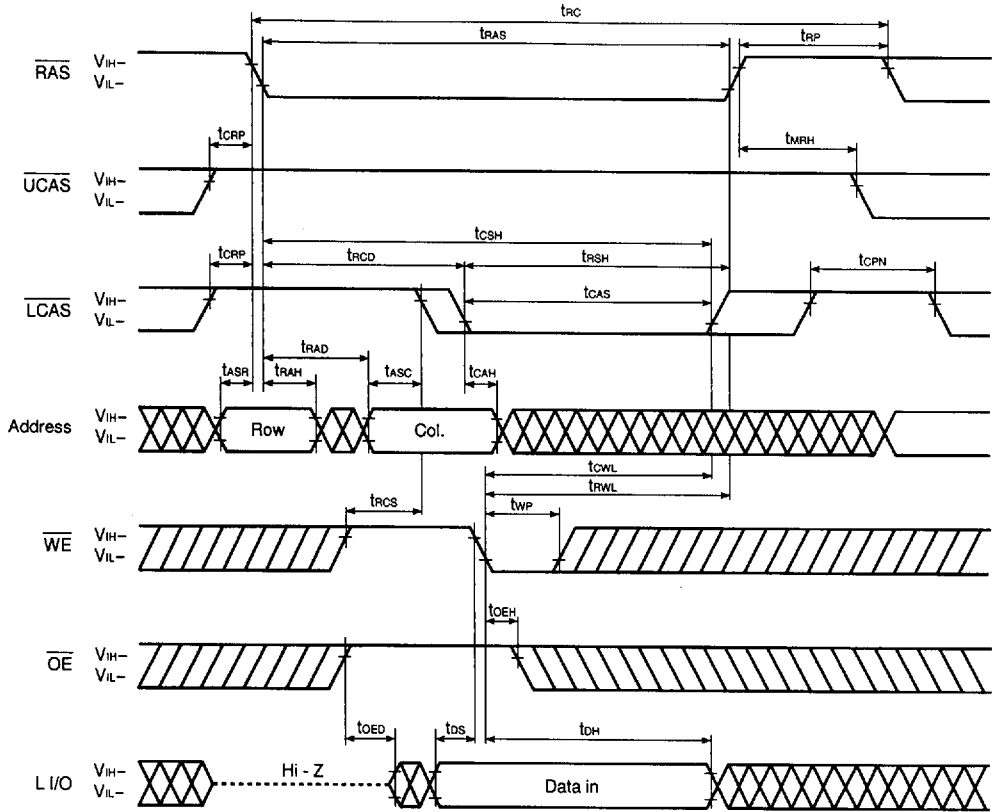


Upper Byte Late Write Cycle



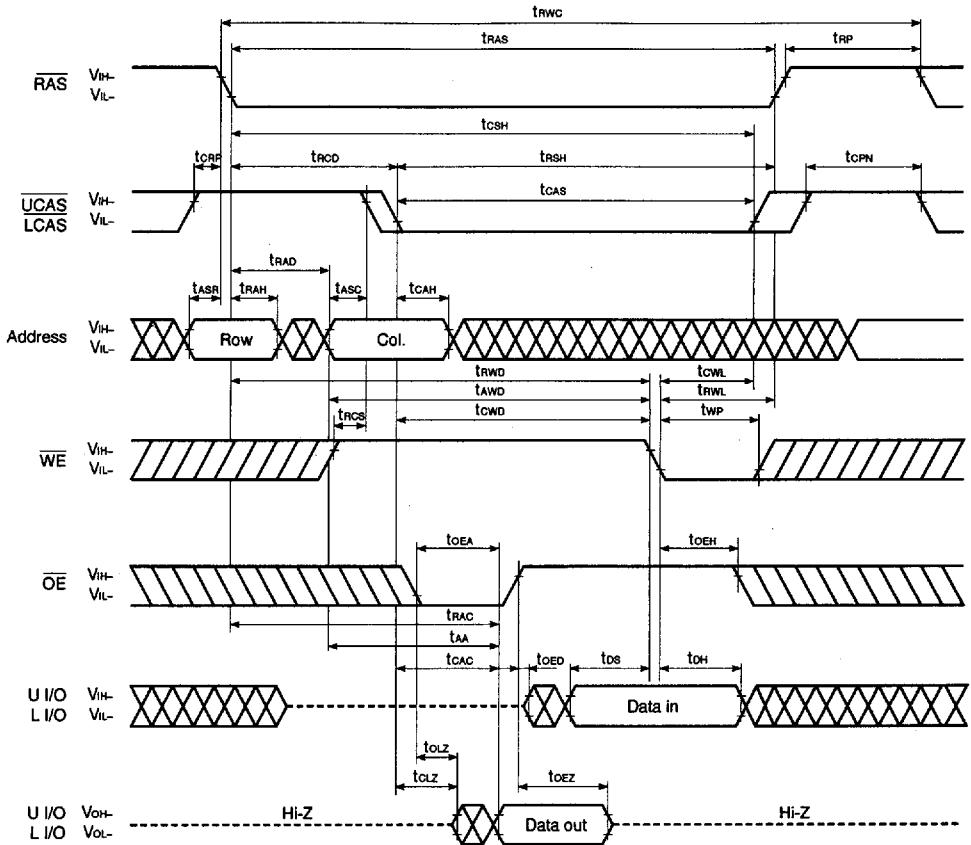
Remark L I/O: Don't care

Lower Byte Late Write Cycle

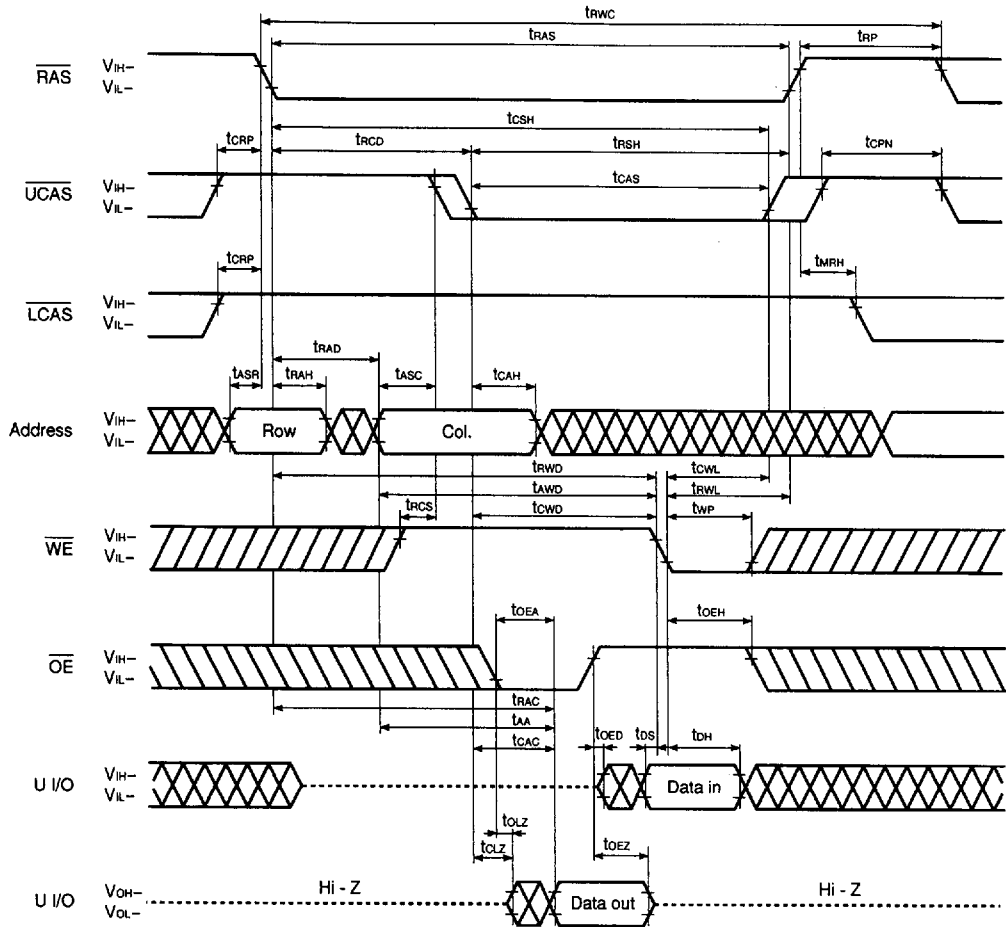


Remark U I/O: Don't care

Read Modify Write Cycle

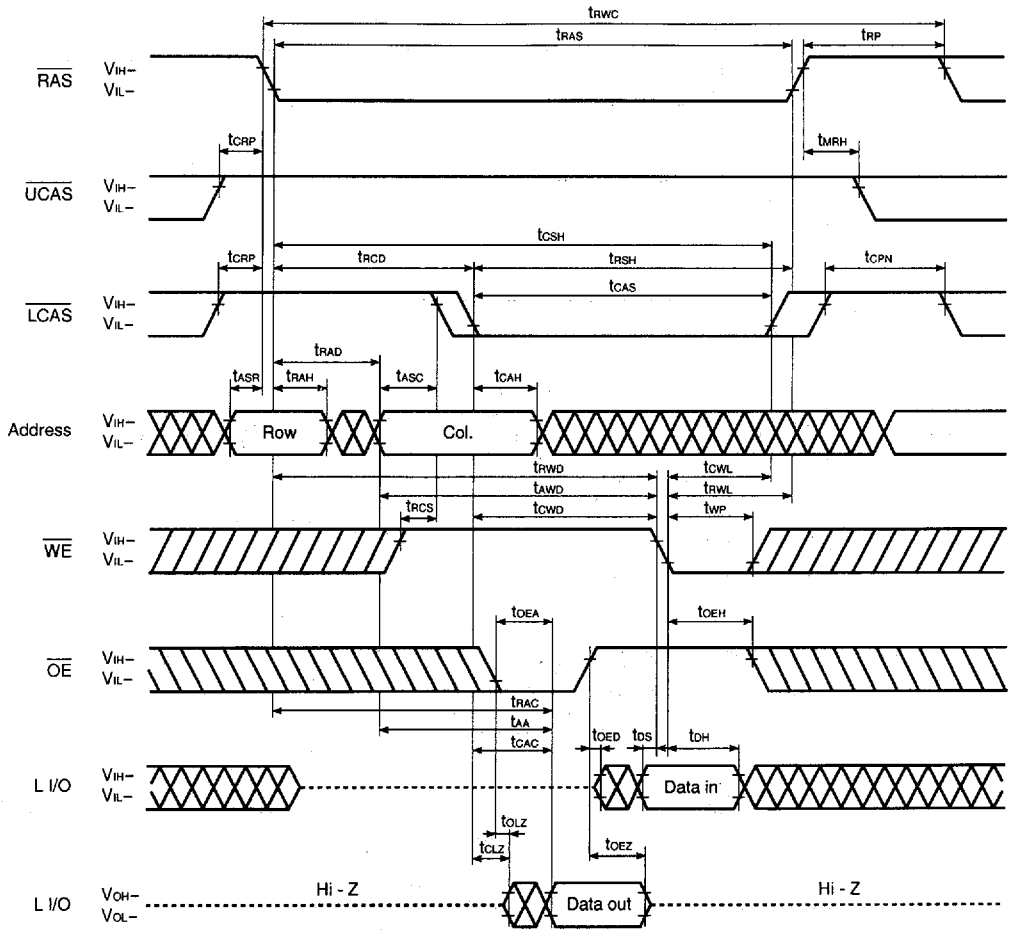


Upper Byte Read Modify Write Cycle



**Remark** In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



**Remark** In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

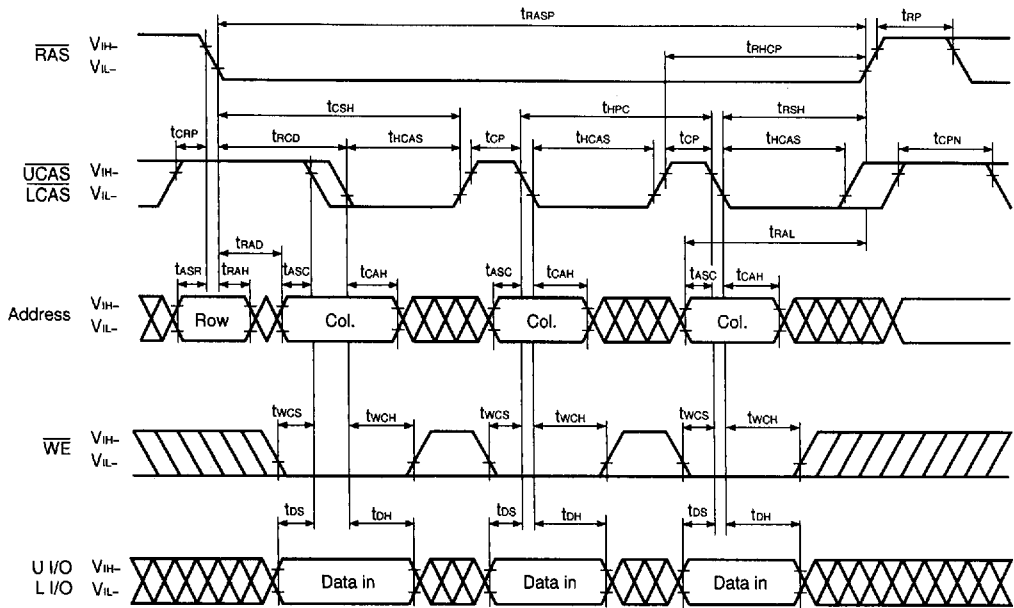








Hyper Page Mode (EDO) Early Write Cycle

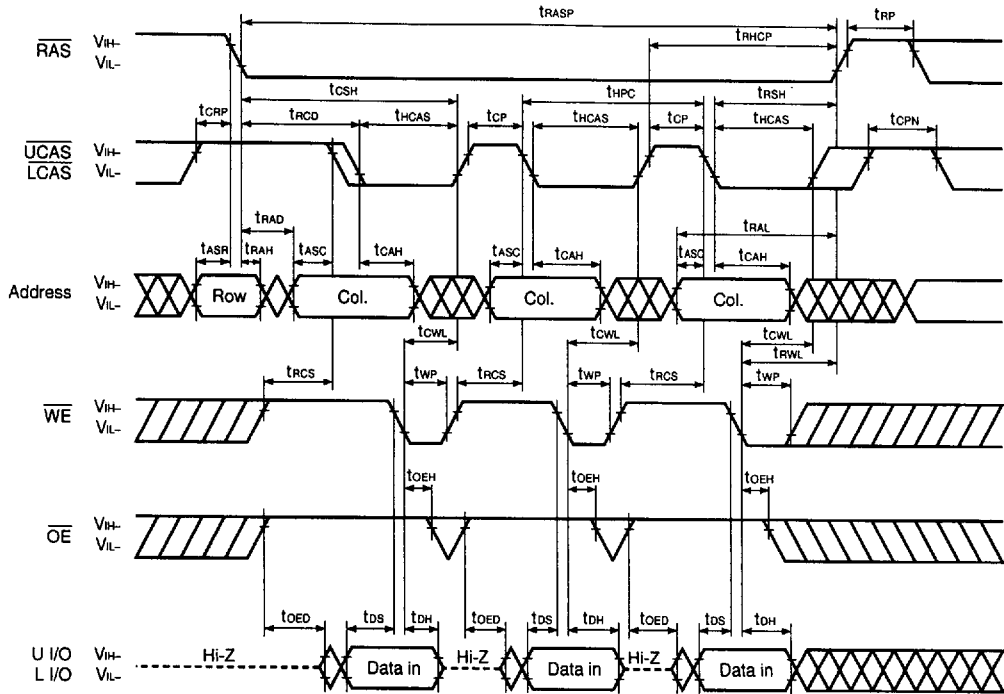


Remarks 1.  $\overline{OE}$ : Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.



Hyper Page Mode (EDO) Late Write Cycle



**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

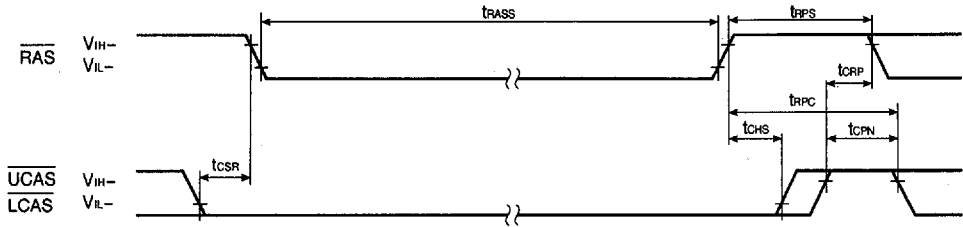








**CAS Before RAS Self Refresh Cycle (Only for the μPD42S4210)**



**Remark** Address,  $\overline{WE}$ ,  $\overline{OE}$ : Don't care L I/O, U I/O: Hi-Z

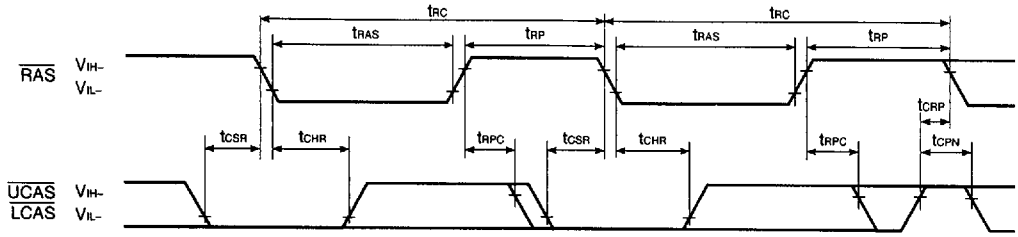
**Cautions on Use of CAS Before RAS Self Refresh**

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

- (1) **Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh**  
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 512 times within an 8 ms interval just before and after setting CAS before RAS self refresh.
- (2) **Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh**  
When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 512 times within an 8 ms interval just before and after setting CAS before RAS self refresh.
- (3) If  $t_{RASS(MIN)}$  is not satisfied at the beginning of CAS before RAS self refresh cycles ( $t_{RAS} < 100 \mu s$ ), CAS before RAS refresh cycles will be executed one time.  
If  $10 \mu s < t_{RAS} < 100 \mu s$ , RAS precharge time for CAS before RAS self refresh ( $t_{RPS}$ ) is applied.  
And refresh cycles (512/128 ms) should be met.

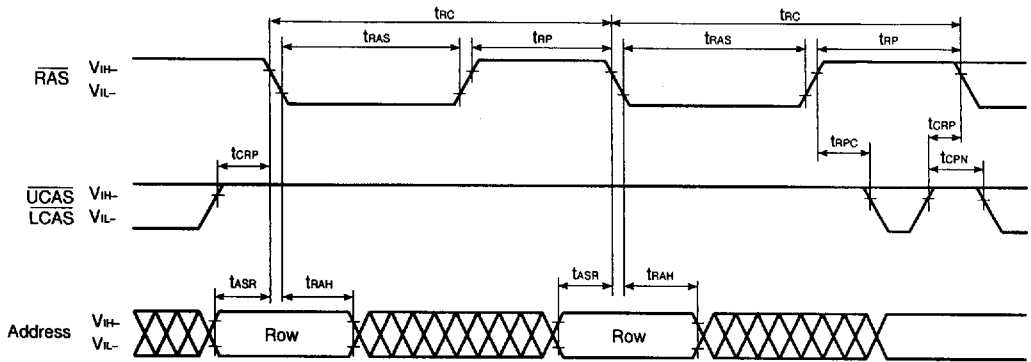
For details, please refer to **How to use DRAM** User's Manual.

**CAS Before RAS Refresh Cycle**



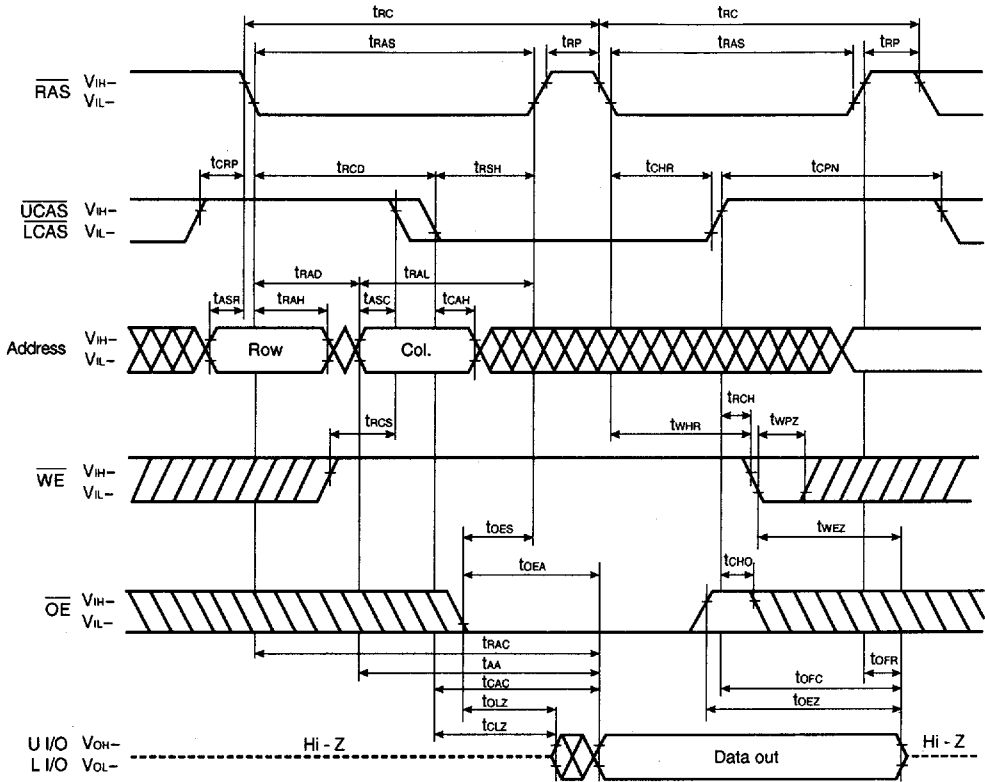
**Remark** Address,  $\overline{WE}$ ,  $\overline{OE}$ : Don't care L I/O, U I/O: Hi-Z

**RAS Only Refresh Cycle**

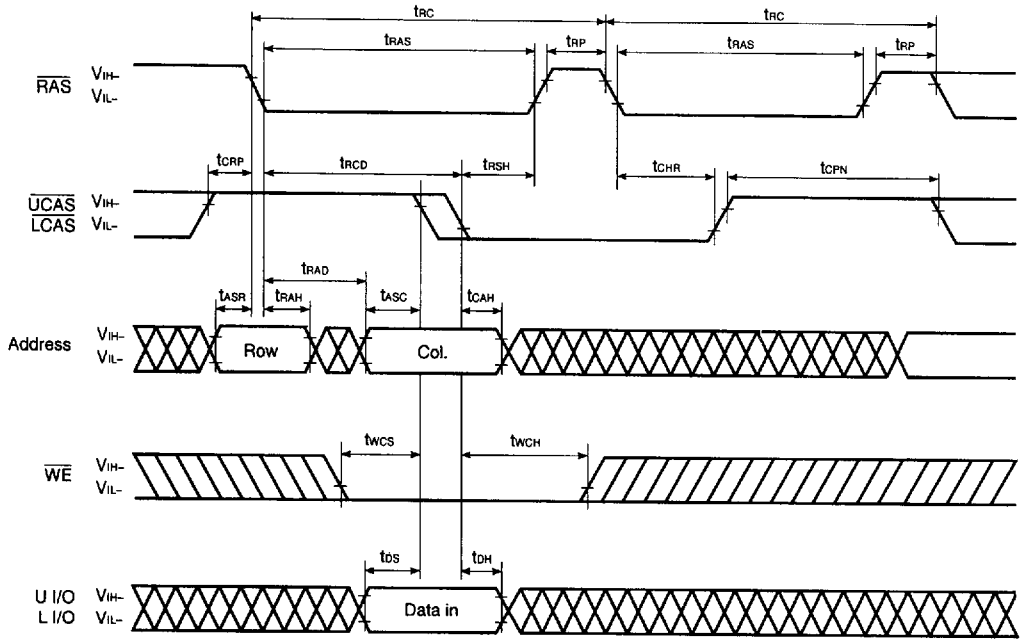


**Remark**  $\overline{WE}$ ,  $\overline{OE}$ : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



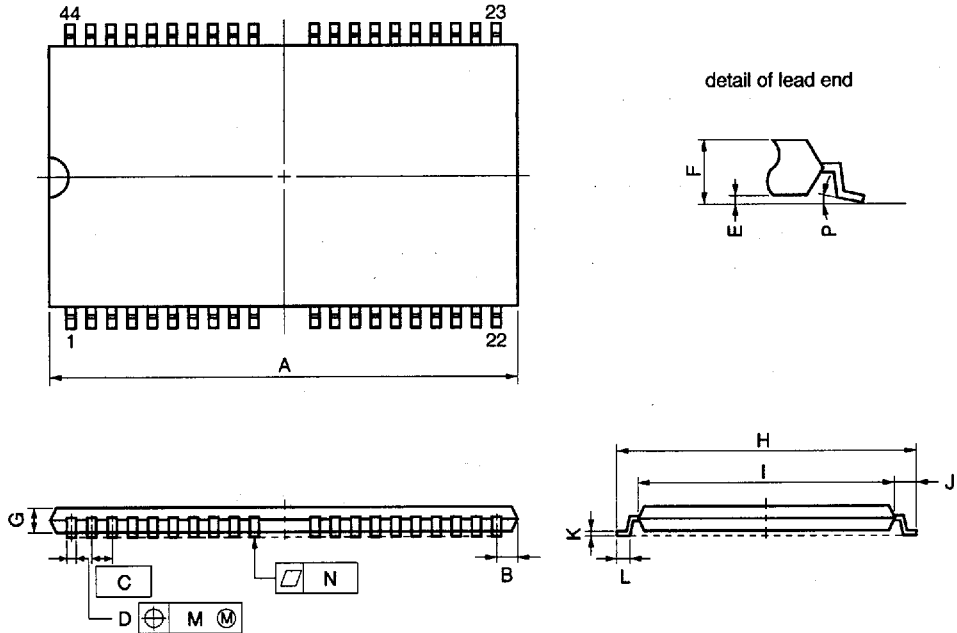
Hidden Refresh Cycle (Write)



Remark  $\overline{OE}$ : Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



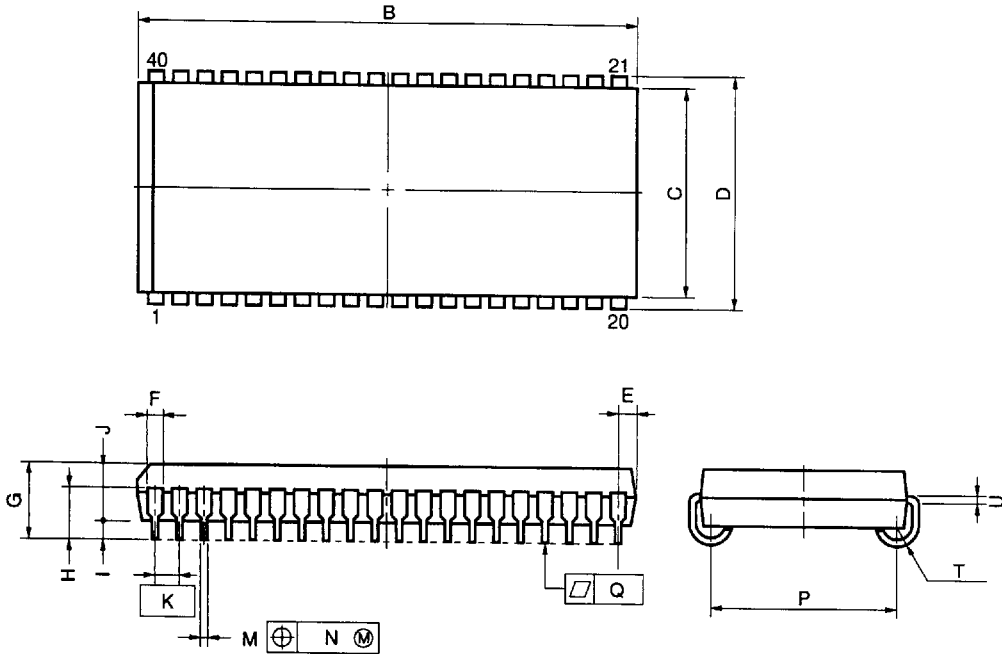
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 <sup>+0.08</sup> <sub>-0.07</sub>	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
M	0.13	0.005
N	0.10	0.004
P	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>

S44G5-80-7JF4

40 PIN PLASTIC SOJ (400 mil)



**NOTE**  
 Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	26.29 <sup>+0.2</sup> <sub>-0.35</sub>	1.035 <sup>+0.008</sup> <sub>-0.014</sub>
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 <sup>+0.006</sup> <sub>-0.007</sub>
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 <sup>+0.009</sup> <sub>-0.008</sub>
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>

P40LE-400A-2

**Recommended Soldering Conditions****Types of Surface Mount Device**

μPD42S4210G5, 424210G5: 44-pin plastic TSOP (II) (400 mil)  
μPD42S4210LE, 424210LE: 40-pin plastic SOJ (400 mil)