OKI Semiconductor

MSM5300/5303

80-DOT SEGMENT DRIVER

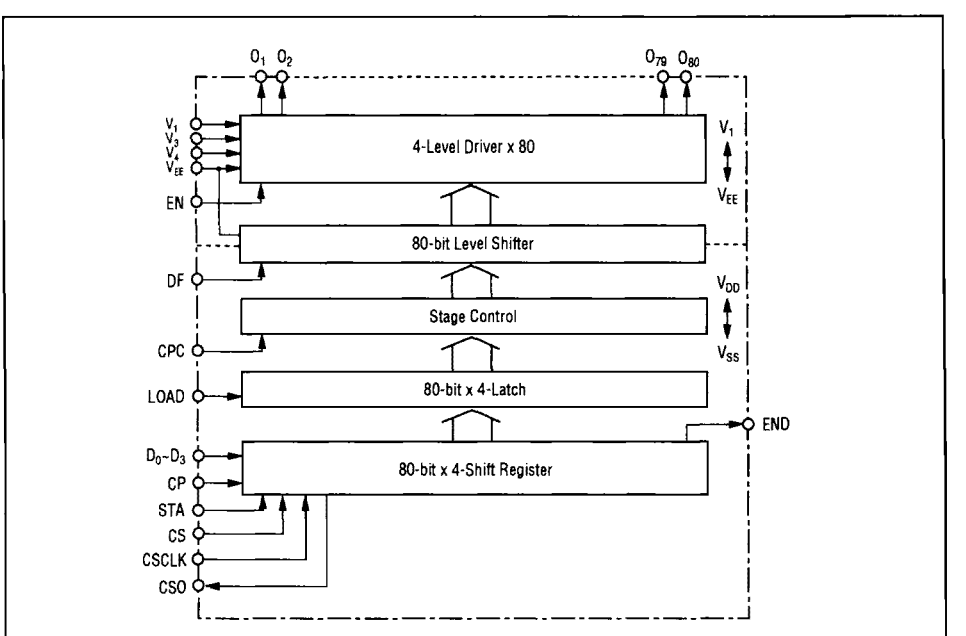
GENERAL DESCRIPTION

The OKI MSM5300GS is an LCD driver LSI installed with 16-stage shift resister for driving segments.

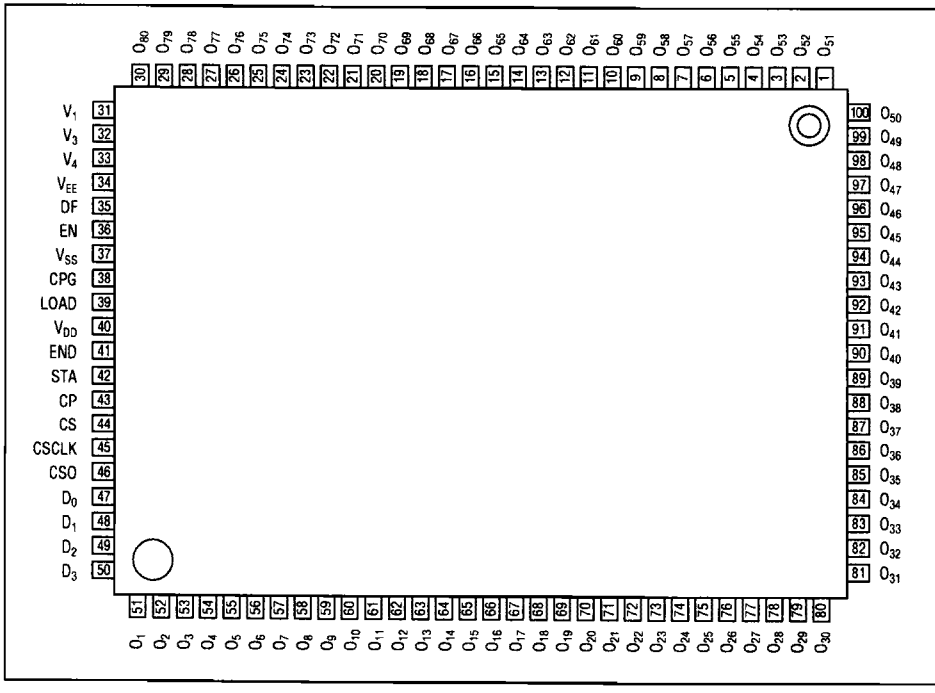
FEATURES

- Integrated 80 bit x 4 latch and shift register
- Capable of a 16-stage dot display
- Maximum input voltage (V_{DD} - V_{EE}) 25V
- MSM5303: Mirror type of MSM5300 (Chip form).
- 100-pin Plastic QFP (QFP100-P-1420-K)
- 100-pin Plastic QFP (QFP100-P-1420-L)

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage for the logic section	V_{DD} - V_{SS}	Ta = 25°C	-0.3 ~ 6.0	V
Applied voltage for driver section	V_{DD} - V_{EE} *1	Ta = 25°C	0 ~ 28	V
Input voltage	V_I	Ta = 25°C	-0.3 ~ V_{DD}+0.3	V
Storage temperature	Tstg	-	-55 ~ +150	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V \leqq V_{DD}$, $V_{SS} = 0V$

OPERATING RANGE

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage for the logic section	V_{DD} - V_{SS}	-	4.5 ~ 5.5	V
Applied voltage for driver section	V_{DD} - V_{EE} *1	-	14 ~ 25	V
Operating temperature	T_{OP}	-	-20 ~ 75	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V \leqq V_{DD}$, $V_{SS} = 0V$

DC CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = -20°C ~ 70°C, V_{SS} = 0V)

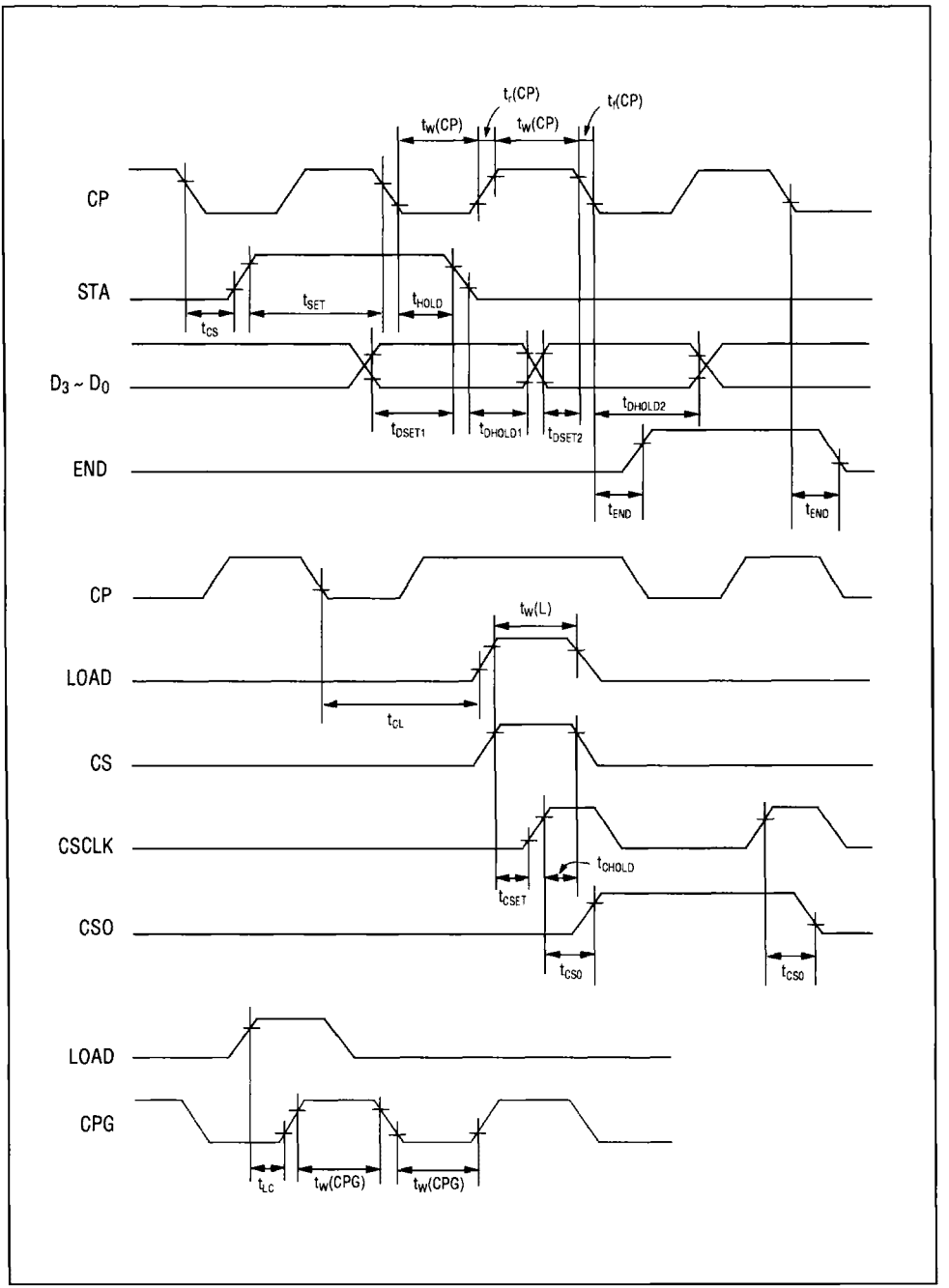
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Corresponding pin
"H" input voltage	V_{IH}		0.8 V_{DD}	-	-	V	DF, STA, CPG, LOAD, D_0~D_3, CP, CS, CSCLK, EN
"L" input voltage	V_{IL}		-	-	0.2 V_{DD}	V	
"H" input current	I_{IH}	$V_I = V_{DD}$	-	-	1	µA	
"L" input current	I_{IL}	V_I = 0V	-	-	-1	µA	
"H" output voltage	V_{OH}	I_O = -0.2mA	V_{DD} -0.4	-	-	V	END, CSO
"L" output voltage	V_{OL}	I_O = 0.2mA	-	-	0.4	V	
ON Resistance	R_{ON}	$V_{DD} = V_{EE}$ = 25V $[V_N - V_O]$ = 0.25V *1	-	2	4	kΩ	O_1~O_{80}
Standby current consumption	$I_{DD}SBY$	f_{CP} = 1MHz, CS = "L" *2 $V_{DD} - V_{EE}$ = 25V No load	-	-	3	mA	
Current consumption (1)	I_{DD}	f_{CP} = 1MHz, CS = "H" *3 $V_{DD} - V_{EE}$ = 25V No load	-	-	5	mA	
Current consumption (2)	IV_1	f_{CP} = 1MHz, *4 $V_{DD} - V_{EE}$ = 25V No load	-	-	200	µA	
Current consumption (3)	IV_2	f_{CP} = 1MHz, *5 $V_{DD} - V_{EE}$ = 25V No load	-	-	500	µA	
Input capacity	C_I	f_{CP} = 1MHz	-	5	-	pF	

*1 $V_N = V_{DD} \sim V_{EE}$, V3 = V_{DD} - 4.5, $V_4 = V_{DD}$ - 20.5, $V_1 = V_{DD}$
*2 Indicating data F0F0 .... DF = 40 Hz, Current flow from V_{DD} to V_{SS}
*3 Indicating data F0F0 .... DF = 40 Hz, Current flow from V_{DD} to V_{SS}
*4 Indicating data F0F0 .... DF = 40 Hz, Current flow through V_1, V_3, V_4
*5 Indicating data F0F0 .... DF = 40 Hz, Current flow through V_{EE}

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = -20°C ~ +75°C, C_L = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum clock frequency	f_{CPMAX}	Duty 50%	4.0	-	-	MHz
CP Pulse width	$t_{W(CP)}$		80	-	-	ns
CP → STA	t_{CS}		100	-	-	ns
STA set-up time	t_{SET}		120	-	-	ns
STA holding time	t_{HOLD}		50	-	-	ns
D_3 ~ D_0 set-up time	t_{DSET1}	When starting	100	-	-	ns
D_3 ~ D_0 holding time	t_{DHOLD1}	When starting	50	-	-	ns
D_3 ~ D_0 set-up time	t_{DSET2}		100	-	-	ns
D_3 ~ D_0 holding time	t_{DEST2}		50	-	-	ns
END signal delay time	t_{END}		-	-	150	ns
CP → LOAD	t_{CL}		150	-	-	ns
Load pulse width	$t_{W(L)}$		250	-	-	ns
CS set-up time	t_{CSET}		80	-	-	ns
CS holding time	t_{CHOLD}		50	-	-	ns
CSO delay time	t_{CSO}		-	-	100	ns
LOAD → CPG	t_{LC}		0	-	$t_{W(L)}$	ns
CP rising/falling time	t_r(CP) t_f(CP)		30	-	-	ns
CPG pulse width	$t_{W(CPG)}$		300	-	-	ns
CSCLK maximum frequency	$f_{CSCLKMAX}$	Duty 50%	4.0	-	-	MHz
CSCLK pulse width	$t_{W(CSCLK)}$		80			ns


CP
STA
D3 ~ D0
END
tr(CP)
tf(CP)
tW(CP)
tW(CP)
tSET
tHOLD
tCS
tDSET1
tDHOLD1
tDSET2
tDHOLD2
tEND
tEND
CP
LOAD
CS
CSCLK
CSO
tW(L)
tCL
tCHOLD
tCSET
tCSO
tCSO
LOAD
CPG
tLC
tW(CPG)
tW(CPG)

PIN DESCRIPTION

Name	I/O	Function
V_1	I	$V_1 \leqq V_{DD}$ V_{LCD}: LCD maximum voltage
V_3	I	$V_1 - \frac{2}{a} V_{LCD}$
V_4	I	$V_1 - (1 - \frac{2}{a})V_{LCD}$ $a = \sqrt{N} + 1$
V_{EE}	I	$V_1 - V_{LCD}$ (1/N: Common duty)
V_{DD}	I	4.5 ~ 5.5V
V_{SS}	I	0V
EN	I	On "H": Normal, on "L" $O_1 \sim O_{80}$ become V_1 level
DF	I	Converted A.C. signal input
CPG	I	Clock pulse input for stage control
LOAD	I	Latch display data used as input. Display data held during high to low transition.
$D_3 \sim D_0$	I	Stage data input
CP	I	Shift clock pulse input for shift register
STA	I	Start pulse input for shift register
CS	I	IC internal enable F/F data input
CSCLK	I	Enable F/F clock input for the above mentioned. When rising, enable F/F is shifted.
CSO	O	Connects to CS pin in the next stage when cascade is connected at the above mentioned enable F/F output.
END	O	Connects to STA when cascade is connected at the shift register final stage output.
$O_1 \sim O_{80}$	O	4 level data output

FUNCTIONAL DESCRIPTION

• POWER DOWN FUNCTION

When cascade is connected, the enable F/F is installed within IC internal section as shown in the power consumption diagram (refer to Fig. 1). Only the display data of the IC set by this enable F/F is transferred. The IC not set by this enable F/F does not transfer and remains at low current consumption condition.

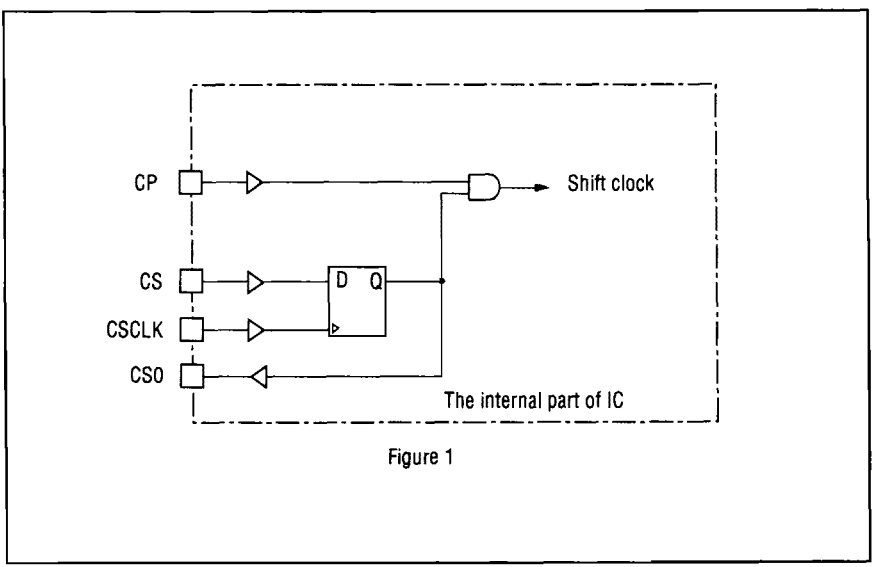


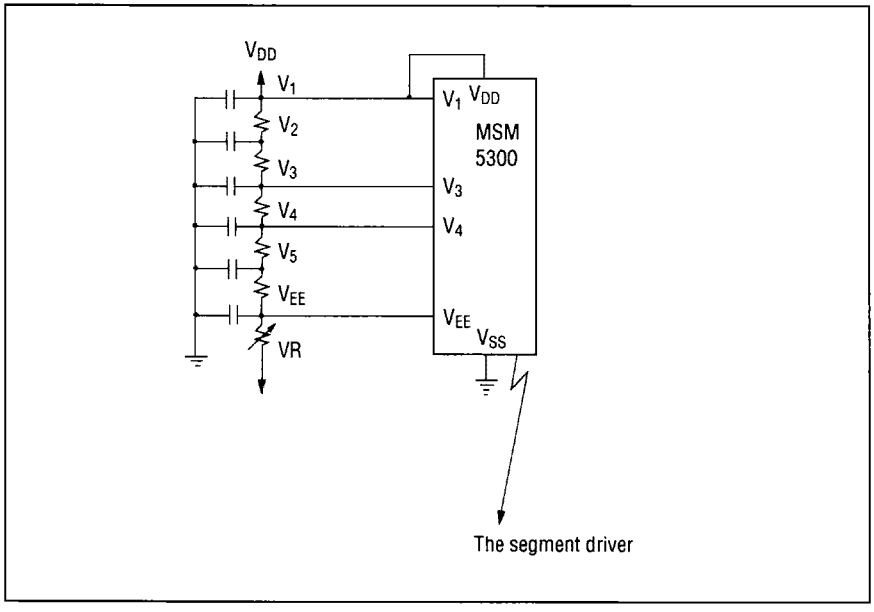
Figure 1

• TRUTH TABLE

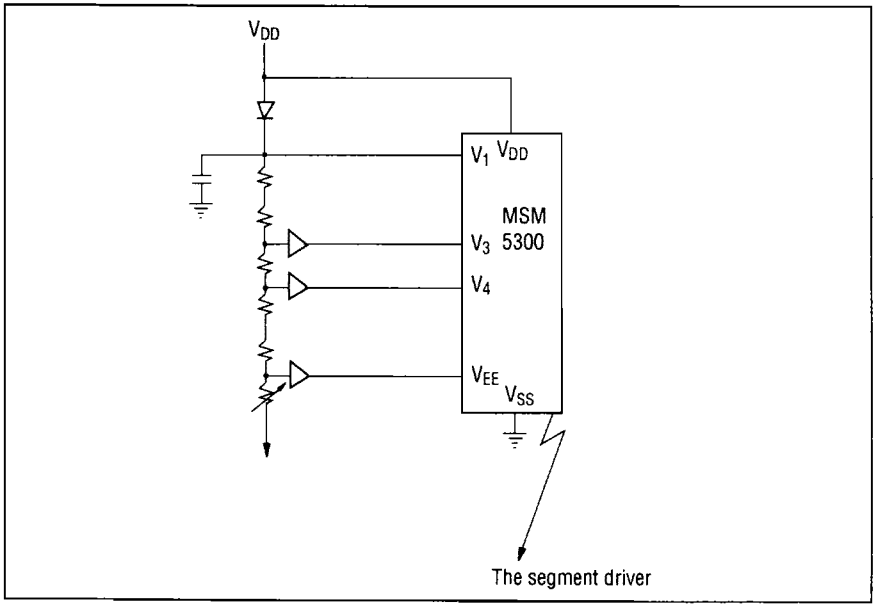
(O_1 ~ O_{80})

EN	DF	Latch data	Driver output
H	L	L	V_3
H	L	H	V_1
H	H	L	V_4
H	H	H	V_{EE}
L	X	X	V_1

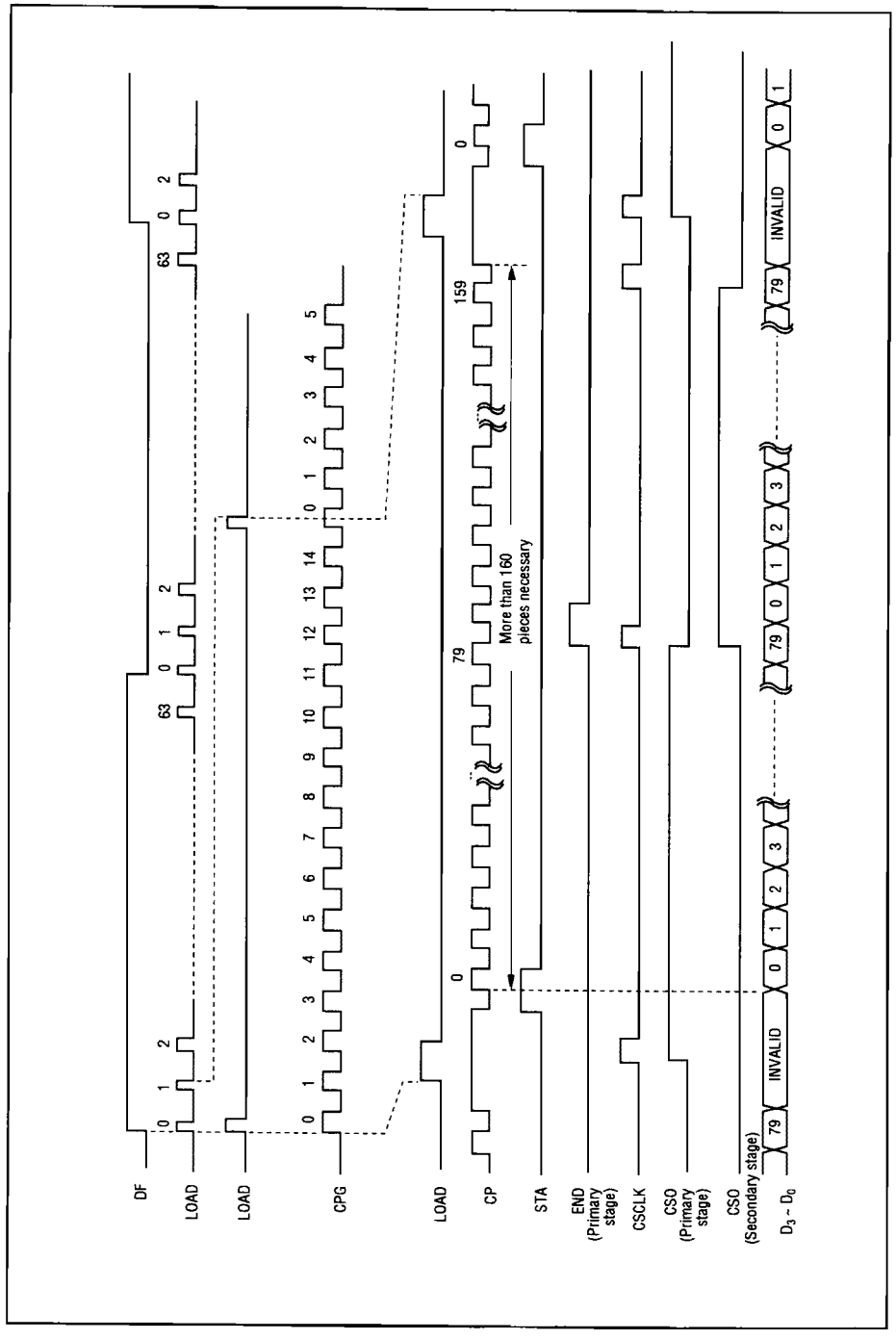
- **Supply to V_1, V_3, V_4, V_{EE} (Example)**
  V_1, V_3, V_4, and V_{EE} employ bias power by the general resistance potential.
  The following is an example:



Alternatively, bias voltage may be supplied by the operational amplifier as shown below:



TIMING CHART



APPLICATION CIRCUIT