HARRIS SEMICONDUCTOR

HS-82C55ARH

Radiation Hardened CMOS Programmable Peripheral Interface

December 1992

Features

- Radiation Hardened
  - Total Dose >10^5 RAD(Si)
  - Transient Upset <10^8 RAD(Si)/s
  - Functional After Total Dose 1 x 10^6RAD(Si)
  - Latch Up Free EPI-CMOS
- Low Power Consumption
  - IDDSB = 20μA
- Pin Compatible with NMOS 8255A and the Harris 82C55A
- High Speed, No "Wait State" Operation with 5MHz HS-80C86RH
- 24 Programmable I/O Pins
- Bus-Hold Circuitry on All I/O Ports Eliminates Pull-Up Resistors
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- 2.0mA Drive Capability on All I/O Port Outputs
- Military Temperature range -55°C to +125°C

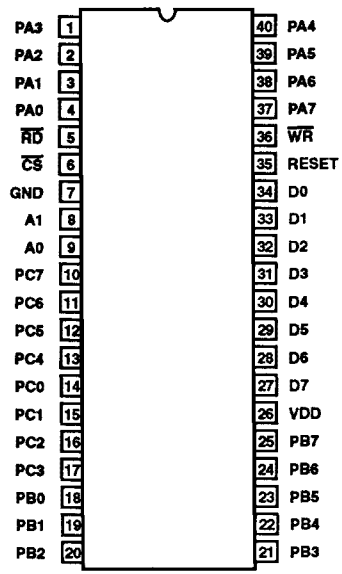
Description

The Harris HS-82C55ARH is a high performance, radiation hardened CMOS version of the industry standard 8255A and is manufactured using a hardened field, self-aligned silicon-gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which are organized into two 8-bit and two 4-bit ports. Each port may be programmed to function as either an input or an output. Additionally, one of the 8-bit ports may be programmed for bi-directional operation,and the two 4-bit ports can be programmed to provide handshaking capabilities. The high performance, radiation hardness, and industry standard configuration of the HS-82C55ARH make it compatible with the HS-80C86RH radiation hardened microprocessor.

Static CMOS circuit design insures low operating power. Bus hold circuitry eliminates the need for pull-up resistors. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinout

40 PIN DIP
CASE OUTLINE D-5, CONFIGURATION 3
TOP VIEW



PIN	DESCRIPTION
D7 - D0	Data Bus (Bi-Directional
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0 - A1	Port Address
PA7 - PA0	Port A (Bit)
PB& - PB0	Port B (Bit)
PC7 - PC0	Port C (Bit)
VDD	+5 volts
GND	0 volts

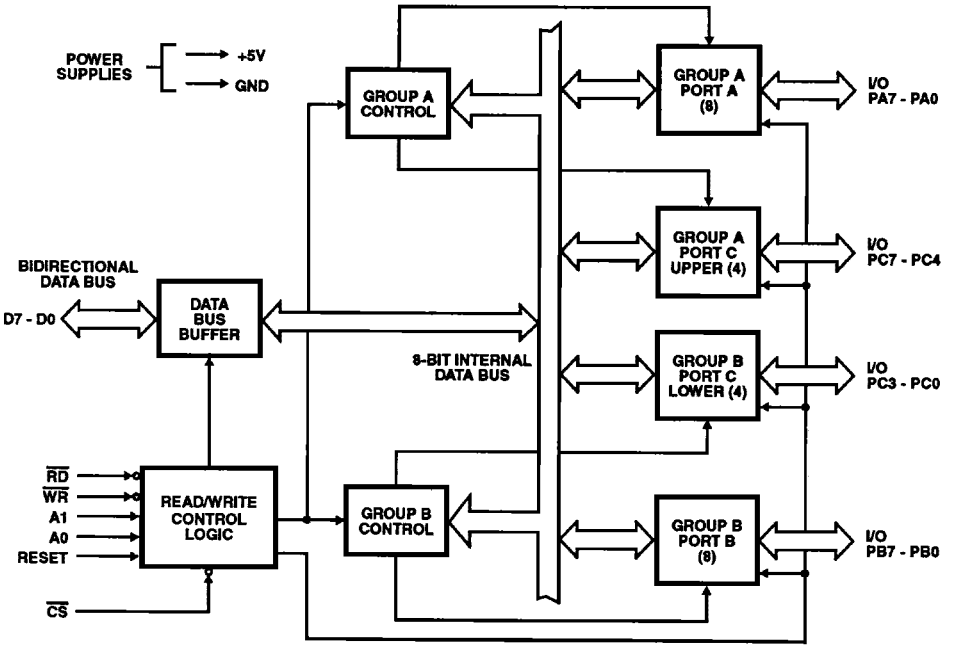
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3191

Pin Description

SYMBOL	PIN NUMBERS	TYPE	DESCRIPTION
PA0-7	1-4, 37-40	I/O	**Port A:** General purpose I/O Port. Data direction and mode is determined by the contents of the Control Word.
PB0-7	18-25	I/O	**Port B:** General purpose I/O port. See Port A.
PC0-3	14-17	I/O	**Port C (Lower):** Combination I/O port and control port associated with Port B. See Port A.
PC4-7	10-13	I/O	**Port C (Upper):** Combination I/O Port and control port associated with Port A. See Port A.
D0-7	27-34	I/O	**Bidirectional Data Bus:** Three-State data bus enabled as an input when $\overline{CS}$ and $\overline{WR}$ are low and as an output when $\overline{CS}$ and $\overline{RD}$ are low.
VDD	26	I	**VDD:** The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7	I	**Ground.**
CS	6	I	**Chip Select:** A "low" on this input pin enables the communication between the HS-82C55ARH and the CPU.
RD	5	I	**Read:** A "low" on this input pin enables the HS-82C55ARH to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the HS-82C55ARH.
WR	36	I	**Write:** A "low" on this input pin enables the CPU to write data or control words into the HS-82C55ARH.
A0 and A1	8, 9	I	**Port Select 0 and Port Select 1:** These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the Least Significant Bits of the address bus (A0 and A1).
Reset	35	I	**Reset:** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the HS-82C55ARH will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400µA.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Brazed Seal DIP Package	26.7°C/W	10.7°C/W
Brazed Seal Flatpacke Package	61.1°C/W	13.6°C/W

Maximum Package Power Dissipation at +125°C
Brazed Seal DIP Package 1.87W
Brazed Seal Flatpack Package 0.82W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TTL Output High Voltage	VOH1	VDD = 4.5V, IO = -2.5mA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	3.0	-	V
CMOS Output High Voltage	VOH2	VDD = 4.5V, IO = -100µA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD-0.4	-	V
Output Low Voltage	VOL	VDD = 4.5V, IO = 2.5mA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Input Current Bus Hold High	IBHH	VDD = 4.5V or 5.5V, VIN = 3.0V (See Note 1) Ports A, B, C	1, 2, 3	-55°C, +25°C, +125°C	-800	-60	µA
Input Current Bus Hold Low	IBHL	VDD = 4.5V or 5.5V, VIN = 1.0V (See Note 2) Port A	1, 2, 3	-55°C, +25°C, +125°C	60	800	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VIN =GND or VDD	1, 2, 3	-55°C, +25°C, +125°C	-	20	µA
Darlington Drive Voltage	VDAR	VDD = 4.5V, IO = -2.0mA, VIN = GND or VDD	1, 2, 3	-55°C, +25°C, +125°C	3.9	-	V
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test (Note 4)	FN	VDD = 5.5V, VIN = GND or VDD - 1.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTES:

1. IBHH should be measured after raising VIN and then lowering to 3.0V.
2. IBHL should be measured after lowering VIN to VSS and then raising to 0.8V.
3. No internal current limiting exists on the Port Outputs. A resistor must be added externally to limit the current.
4. For VIH (VDD = 5.5V) and VIL (VDD = 4.5V) each of the following groups is tested separately with all other inputs using VIH = 2.6V, VIL = 0.4V: PA, PB, PC, Control Pins (Pins 5, 6, 8, 9, 35, 36).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS T_A = -55°C to +125°C

PARAMETERS	SYMBOL	CONDITIONS	SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
READ							
Address Stable Before $\overline{RD}$	TAVRL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Stable After $\overline{RD}$	TRHAX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{RD}$ Pulse Width	TRLRH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	250	-	ns
Data Valid From $\overline{RD}$	TRLDV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Data Float After $\overline{RD}$	TRHDX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Time Between $\overline{RD}$s and/or $\overline{WR}$s	TRWHRWL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns
WRITE							
Address Stable Before $\overline{WR}$	TAVWL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Stable After $\overline{WR}$	TWHAX	VDD = 4.5, 5.5V, Ports A and B	9, 10, 11	-55°C, +25°C, +125°C	20	-	ns
		VDD = 4.5, 5.5V, Port C	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
$\overline{WR}$ Pulse Width	TWLWH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Data Valid to $\overline{WR}$ High	TDVWH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Data Valid After $\overline{WR}$ High	TWHDX	VDD = 4.5, 5.5V, Ports A and B	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
		VDD = 4.5, 5.5V, Port C	9, 10, 11	-55°C, +25°C, +125°C	100	-	
OTHER TIMINGS							
$\overline{WR}$ = 1 to Output	TWHPV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	350	ns
Peripheral Data Before $\overline{RD}$	TPVRL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Peripheral Data After $\overline{RD}$	TRHPX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{ACK}$ Pulse Width	TKLKH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
$\overline{STB}$ Pulse Width	TSLSH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Peripheral Data Before $\overline{STB}$ High	TPVSH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	20	-	ns
Peripheral Data After $\overline{STB}$ High	TSHPX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
$\overline{ACK}$ = 0 to Output	TKLPV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	175	ns
$\overline{ACK}$ = 1 to output Float	TKHPZ	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS T_A = -55°C to +125°C (Continued)

PARAMETERS	SYMBOL	CONDITIONS	SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	TWHOL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	TKLOH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{STB}$ = 0 to IBF = 1	TSLIH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{RD}$ = 1 to IBF = 0	TRHIL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{RD}$ = 0 to INTR = 1	TRLNL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
$\overline{STB}$ = 1 t INTR = 1	TSHNH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{ACK}$ = 1 to INTR = 1	TKHNH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{WR}$ = 0 to INTR = 0	TWLNL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
RESET Pulse Width	TRSHRSL	VDD = 4.5, 5.5V (Note 2)	9, 10, 11	-55°C, +25°C, +125°C	500	-	ns

NOTES:

1. AC's tested at worst case VDD, guaranteed over full operating range.
2. Period of initial RESET pulse after power-on must be at least 50µs. Subsequenct RESET pulses may be 500ns minimum.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground	T_A = +25°C	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz, All measurements referenced to device ground	T_A = +25°C	-	20	pF
Data Float After $\overline{RD}$	TRHDX	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	75	ns
$\overline{ACK}$ = 1 to Output Float	TKHPZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	250	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics

TALBE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

See +25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7, 9)

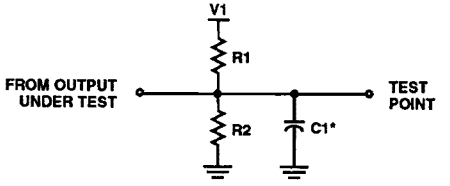
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	±10µA
Input Leakage Current	IIL, IIH	±200nA
Output Leakage Current	IOZL, IOZH	±2µA
Low Level Output Voltage	VOL	±80mV
TTL Output High Voltage	VOH1	±600mV
CMOS Output High Voltage	VOH2	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	-
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
	Others	Samples/5004	1, 7	-
Group C		Samples/5004	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D		Samples/5004	1, 7	1, 7
Group E, Subgroup 2		Samples/5004	1, 7, 9	1, 7, 9

AC Test Circuit

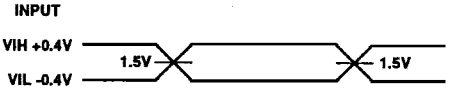


* Includes stray and jig capacitance

TEST CONDITIONS DEFINITION TABLE

V1	R1	R2	C1
1.7V	523Ω	Open	150pF

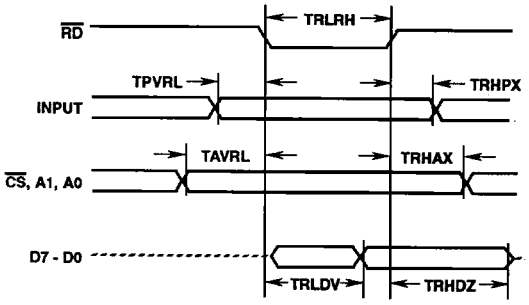
AC Testing Input, Output Waveforms



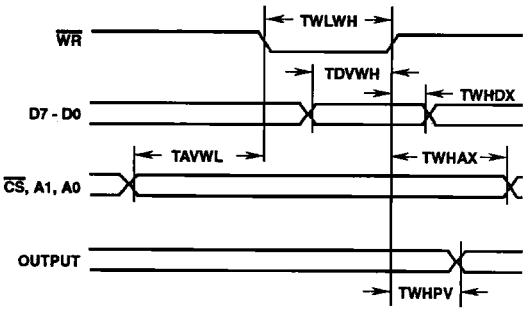
NOTE: AC Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V.

Waveforms

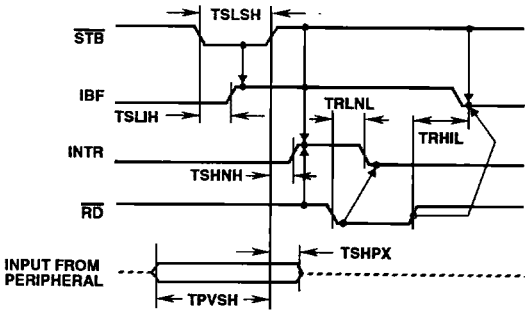
MODE 0 (BASIC INPUT)



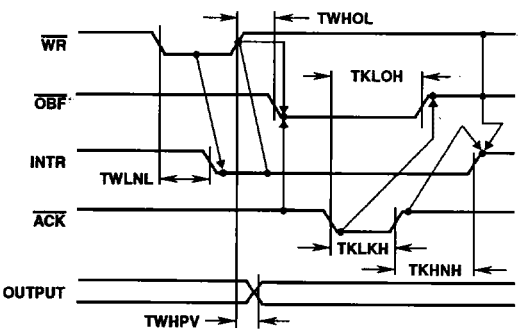
MODE 0 (BASIC OUTPUT)



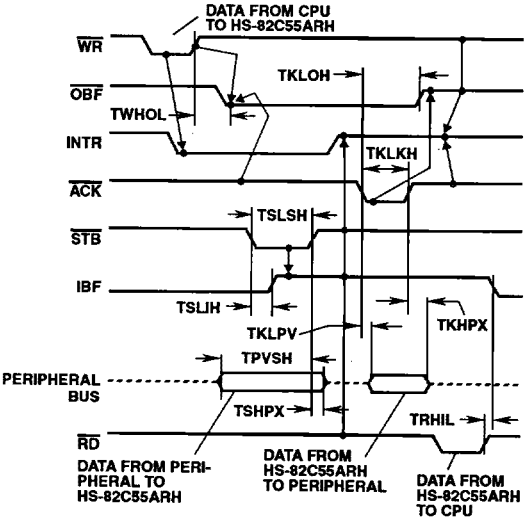
MODE 1 (STROBED INPUT)



MODE 1 (STROBED OUTPUT)

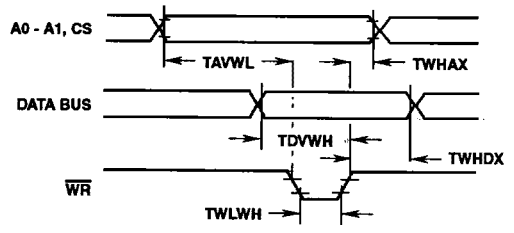


MODE 2 (BIDIRECTIONAL)

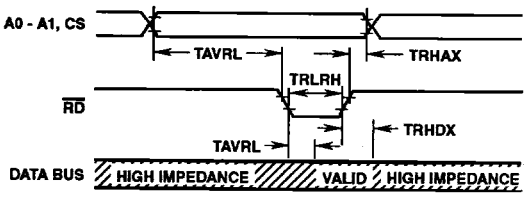


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

WRITE TIMING

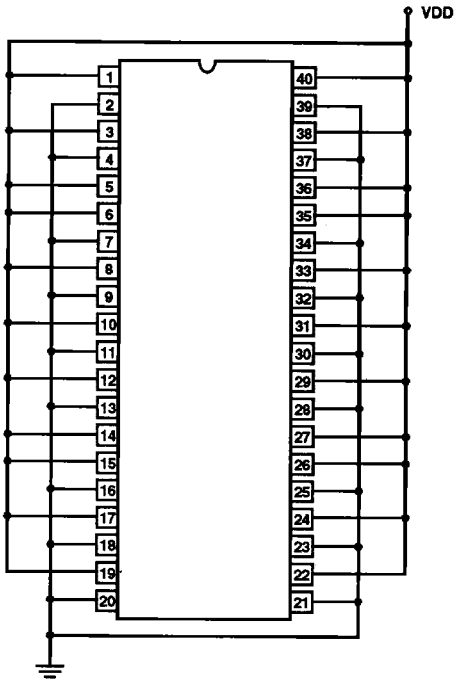


READ TIMING



Burn-In Circuits

PROGRAMMABLE PERIPHERAL INTERFACE

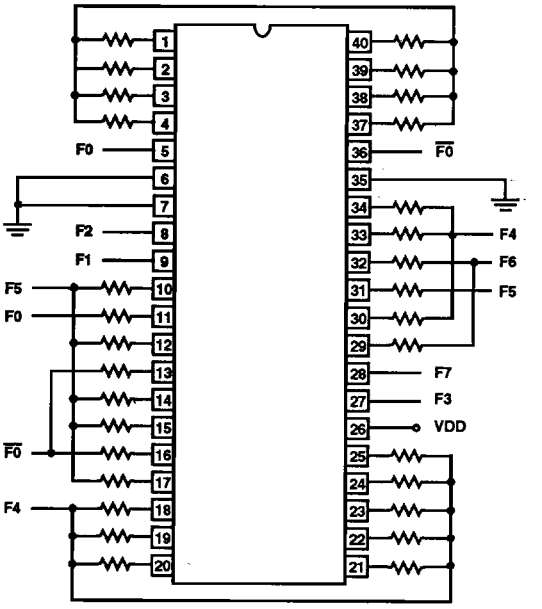


STATIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0. 5%
IDD <500µA
T_A Min = +125°C

PROGRAMMABLE PERIPHERAL INTERFACE



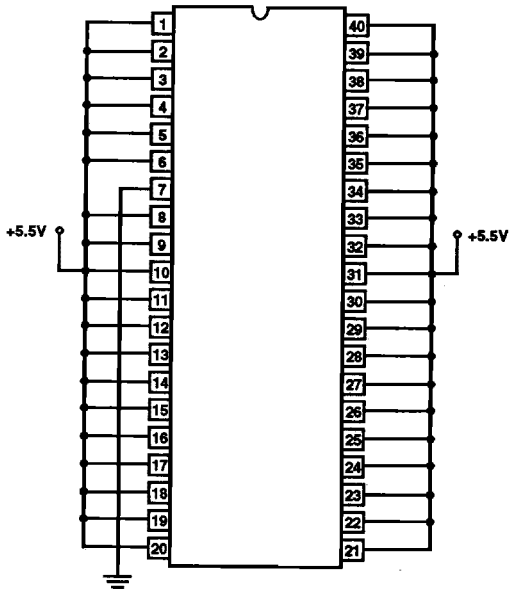
DYNAMIC CONFIGURATION

NOTES:

VDD = 6.0V ± 5% for Burn-In
VDD = 5.0V ± 5% for Life Test
All resistors are 10KΩ ± 5%
-0.3V ≤ VIL ≤ 0.8V
VDD - 1.0V ≤ VIH ≤ VDD
IDD < 5mA
F0 = 10KHz, 50% Duty cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F7 = F6/2
T_A Min = +125°C

Irradiation Circuit

CMOS PROGRAMMABLE PERIPHERAL INTERFACE



NOTES:

VDD = 5.5V

All Group E Testing is performed in a ceramic side brazed DIP

Group E Sample Size is 2 die/wafer

Harris - Space Level '-Q' Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection Method 2020, Condition A 20G
Serialization
X-Ray Inspection Method 2012 (Two Views)
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C, Method 1015 Condition A
+25°C Interim Electrical Tests Subgroups 1, 7, 9 (T1)
Burn-In Delta Calculation (T0 - T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests (T2) Subgroups 1, 7, 9 (T2)
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Fine and Gross Leak Tests Method 1014
Brand
Customer Source Inspection (Note 1)
Group B Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-Q' Data Pack Contains:
   Cover Sheet:
   a) Purchase Order Number
   b) Customer Part Number
   c) Lot Date Code
   d) Harris Part Number
   e) Lot Number
   f) Quantity
   Certificate of Conformance (as found on shipper).
   Shippable serial number list.
   Test Attributes (including Group A) for all test temperatures.
5. Test Variables data for all read/record and delta operations.
   +25°C Initial Test (T0)
   +25°C Interim Test (T1)
   +25°C Final Test (T2)
   All +25°C Delta's (T1-T0, T2-T0)
   +125°C Final Test
   -55°C Final Test
   Wafer Lot Acceptance Report (includes SEM).
   X-Ray report and Film.
   Radiation Testing Certificate of Conformance.
   Assembly Attributes (Post seal).

Harris - '-8' Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests Subgroups 1, 7, 9
PDA Calculation: 5% Subgroups 1, 7
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data Pack Contains:
   Assembly Attributes (Post Seal).
   Test Attributes (Including Group A).
   Radiation Testing Certificate of Conformance.
   Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
3420µm x 4350µm x 485µm ± 25µm

METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

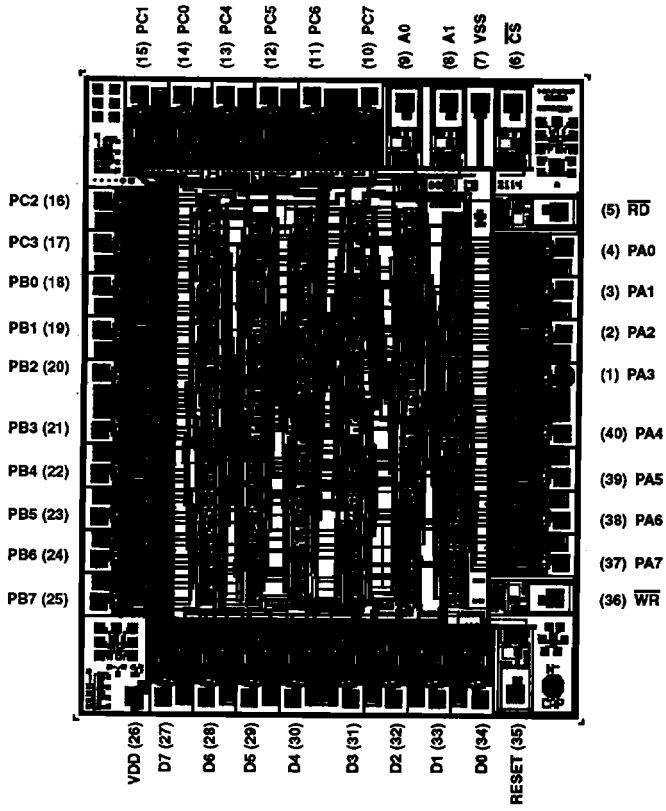
GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy

WORST CASE CURRENT DENSITY:
7.7×10^4 A/cm^2

Metallization Mask Layout

HS-82C55ARH



Functional Description

The HS-82C55ARH is a programmable peripheral interface designed to allow microcomputer systems to control and interface with all types of peripheral devices.It has the ability to generate and respond to all asynchronous handshaking signals necessary to transfer data to and from peripheral devices, and it can also interrupt the processor when a peripheral needs servicing. These capabilities allow the HS-82C55ARH to be used in an unlimited number of applications including EXTERNAL SYSTEM CONTROL, ASYNCHRONOUS DATA TRANSFER, and SYSTEMS MONITORING.

Data Bus Buffer

This tri-state bidirectional 8-bit buffer is used to interface the HS-82C55ARH to the system data bus (see Figure 1). Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

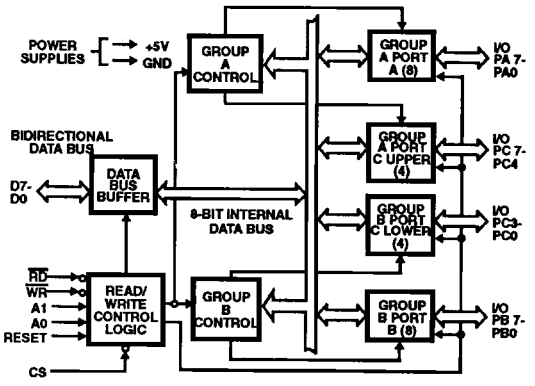


FIGURE 1. BLOCK DIAGRAM DATA BUS BUFFER, READ/WRITE, GROUP A AND B CONTROL LOGIC FUNCTIONS

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfer of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU writes a control word to the HS-82C55ARH. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the HS-82C55ARH.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group - Port A and Port C upper (C7 - C4)

Control Group - Port B and Port C lower (C3 - C0).

Ports A, B, C

The HS-82C55ARH contains three 8-bit ports (A, B and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the HS-82C55ARH.

Port A — One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus hold devices are present on Port A. See Figure 2A.

Port B — One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C — One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B. See Figure 2B.

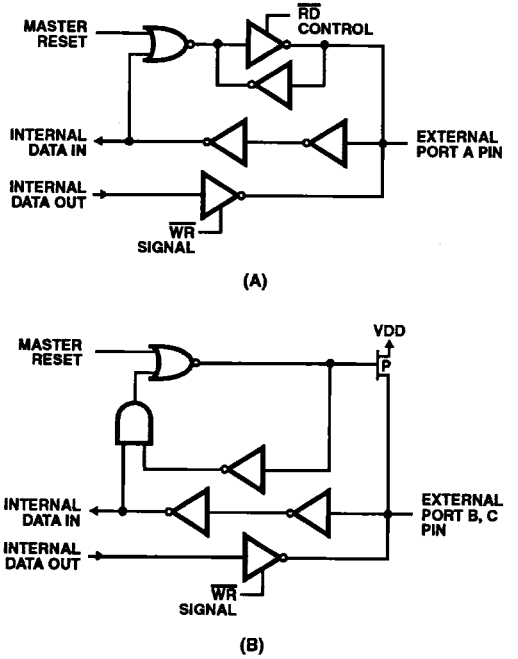


FIGURE 2. I/O PORT CONFIGURATION

Operational Description

Control Word

The data direction and mode of Ports A, B and C are determined by the contents of the Control Word. See Figure 4. The Control Word can be both written and read as shown in Table 1 and 2. During write operations, the function of the Control Word being written is determined by data bit D7. If D7 is low, the data on D0 - D3 will set or reset one of the bits of Port C. See Figure 5. During read Operations, the Control

Word will always be in the format illustrated in Figure 4 with Bit D7 high to indicate Control Word Mode Information.

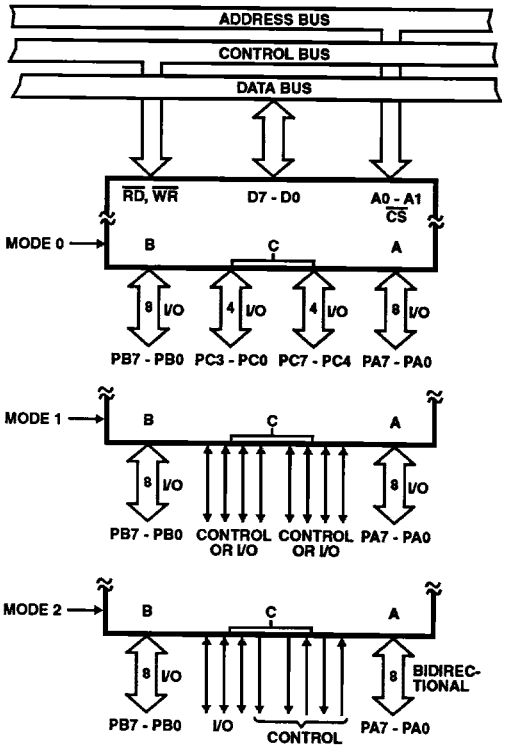


FIGURE 3. BASIC MODE DEFINITIONS & BUS INTERFACE

TABLE 1.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus

TABLE 2.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control Word

TABLE 3.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	DISABLE FUNCTION
X	X	X	X	1	Data Bus - 3-State
X	X	1	1	0	Data Bus - 3-State

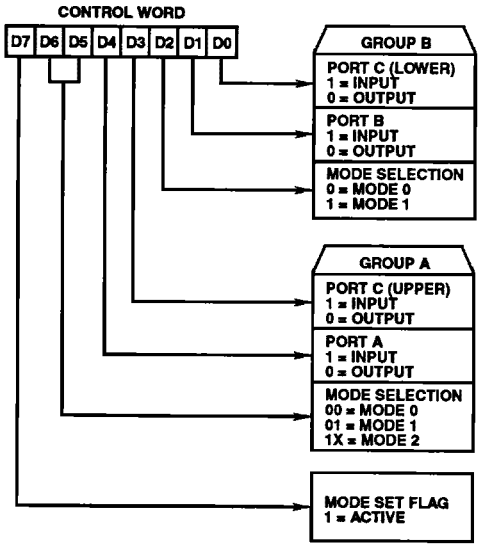


FIGURE 4. MODE SET CONTROL WORD FORMAT

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output

Mode 1 - Strobed Input/Output

Mode 2 - Bidirectional Bus

When the RESET input goes "high", all ports will be set to the input mode with all 24 port lines held at the logic "one" level by internal bus hold devices. After reset, the HS-82C55ARH can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single HS-82C55ARH to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape recorder on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the HS-82C55ARH has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

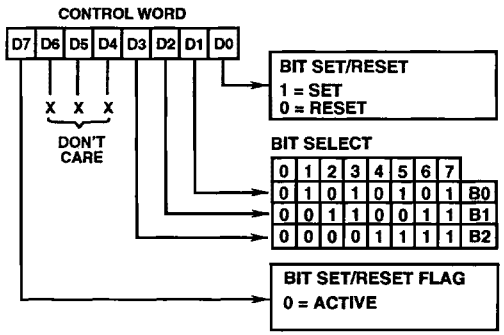


FIGURE 5. BIT SET/RESET CONTROL WORD FORMAT

Single Bit/Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. See Figure 5. This feature reduces software requirements in control-based applications.

Interrupt Control Functions

When the HS-82C55ARH is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enable by setting or resetting the associated INTE flip-flop, using the Bit Set/Reset function of Port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition:

(BIT-SET) - INTE is SET - Interrupt enable.

(BIT-RESET) - INTE is RESET - Interrupt disable.

NOTE: All mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

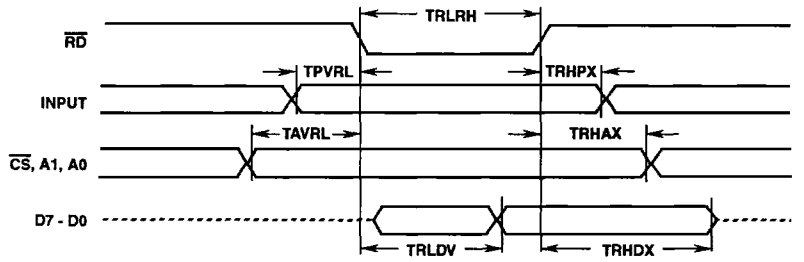
Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the three ports. No handshaking it required, data is simply written to or read from a specific port.

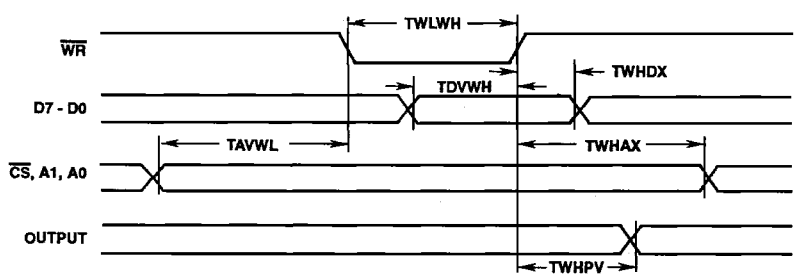
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

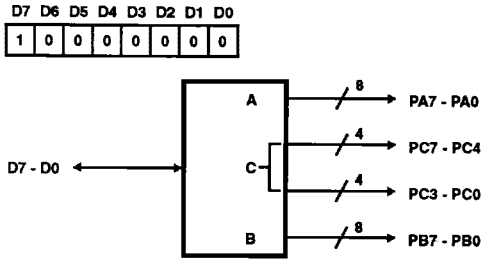


Mode 0 Port Definition

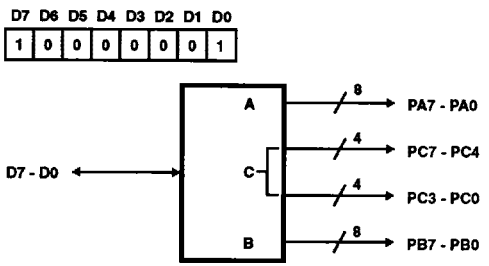
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (UPPER)	NO.	PORT B	PORT C (LOWER)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 Configurations

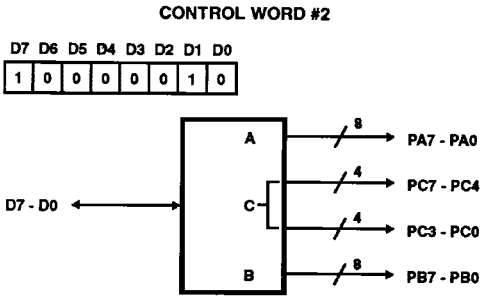
CONTROL WORD #0



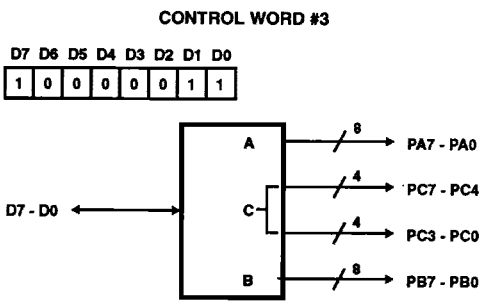
CONTROL WORD #1



CONTROL WORD #2



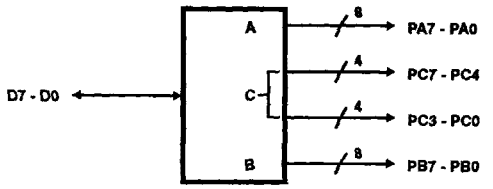
CONTROL WORD #3



Mode 0 Configurations (Continued)

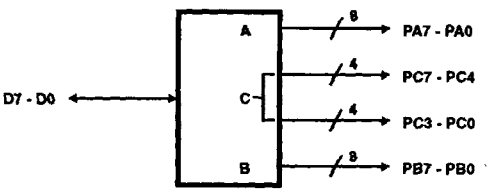
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



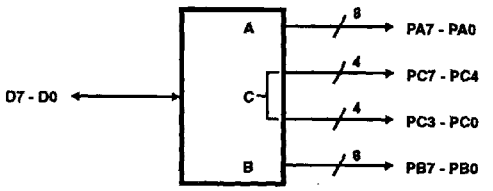
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	1



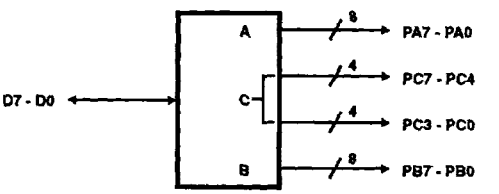
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



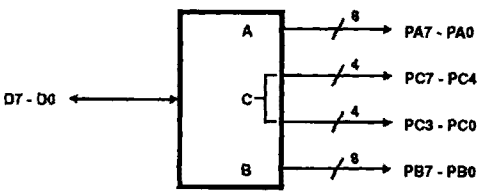
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



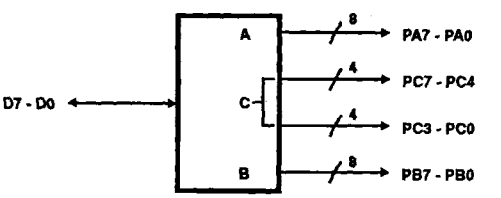
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



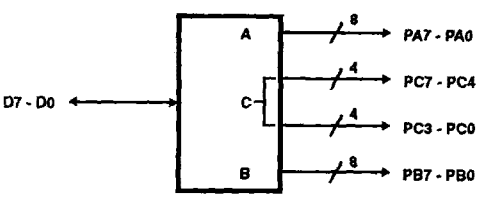
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



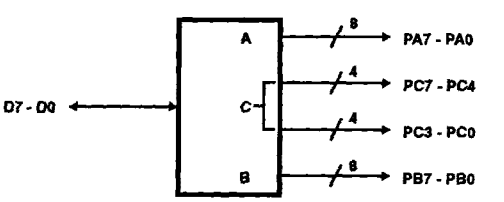
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



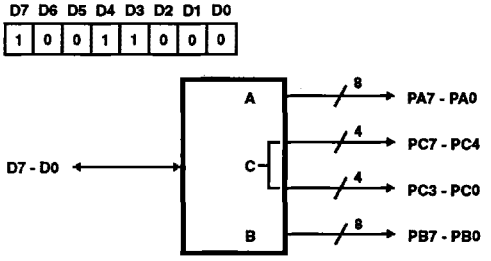
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

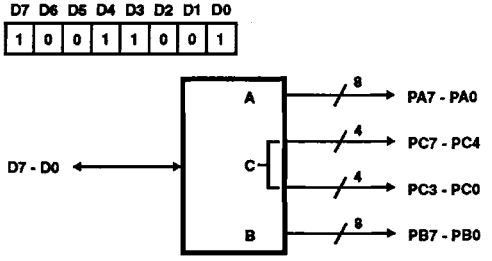


Mode 0 Configurations (Continued)

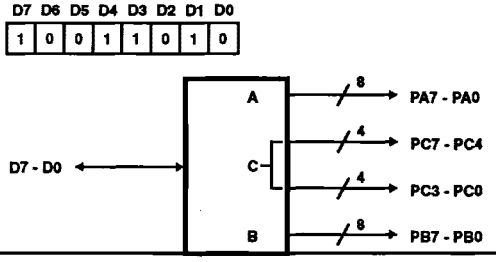
CONTROL WORD #12



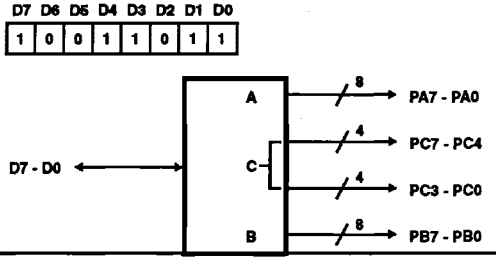
CONTROL WORD #13



CONTROL WORD #14



CONTROL WORD #15



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ and reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by Bit Set/Reset of PC4.

INTE B

Controlled by Bit Set/Reset of PC2.

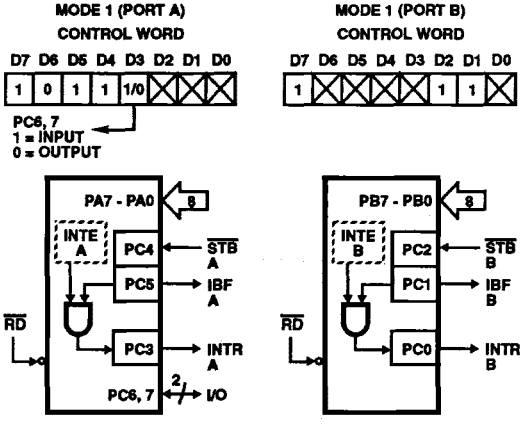


FIGURE 6. MODE 1 INPUT

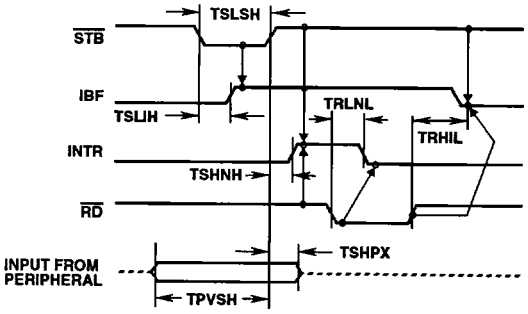


FIGURE 7. MODE 1 (STROBED INPUT)

Output Control Signal Definition

OBF (Output Buffer Full F/F)

The OBF output will go "low" to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the port at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF. See Note 1. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

ACK (Acknowledge Input)

A "low" on this input informs the HS-82C55ARH that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data. See Note 1.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of ACK and reset by the falling edge of WR.

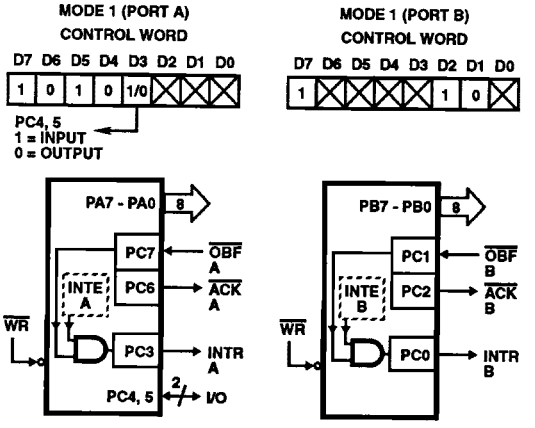


FIGURE 8. MODE 1 OUTPUT

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

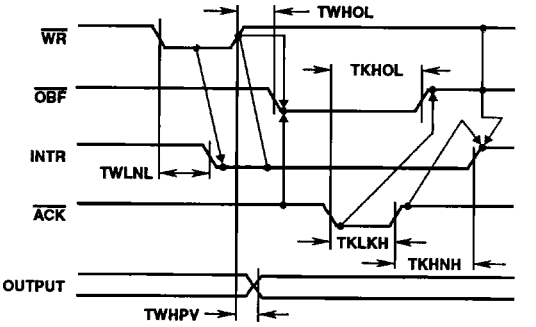


FIGURE 9. MODE 1 (STROBED OUTPUT)

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generate an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

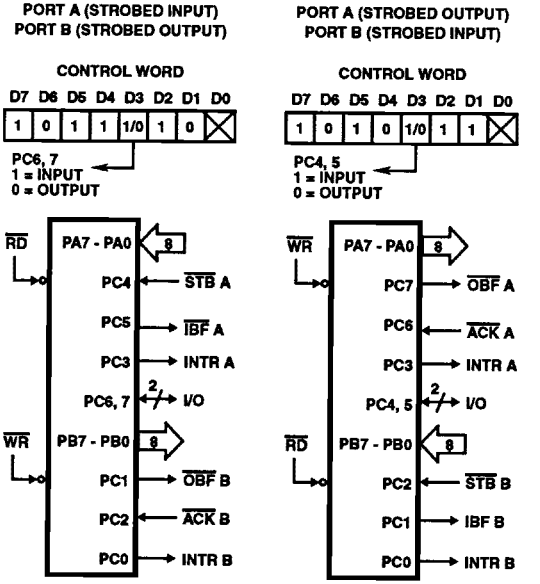


FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bidirectional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bidirectional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations. INTR will be set either by the rising edge of $\overline{ACK}$ (INTE1 = 1) or the rising edge of $\overline{STB}$ (INTE2 = 1). INTR will be reset by the falling edge of $\overline{WR}$ (if previously set by the rising edge or $\overline{ACK}$), the falling edge of $\overline{RD}$ (if previously set by the rising edge of $\overline{STB}$), or the falling edge of $\overline{WR}$ when immediately following a low $\overline{RD}$ pulse or the falling edge of $\overline{RD}$ when immediately following a low $\overline{WR}$ pulse (if previously set by the rising edges of both $\overline{ACK}$ and $\overline{STB}$).

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$)

Controlled by Bit Set/Reset of PC6.

Input Operations

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF)

Controlled by Bit Set/Reset of PC4.

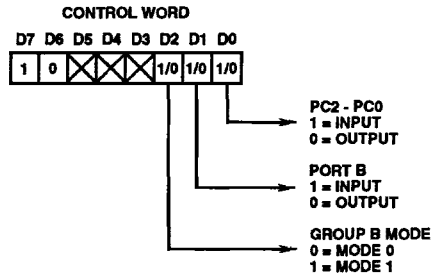


FIGURE 11. MODE CONTROL WORD

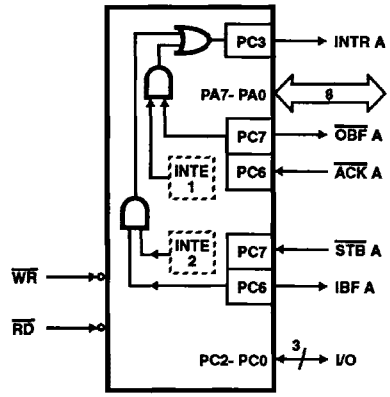
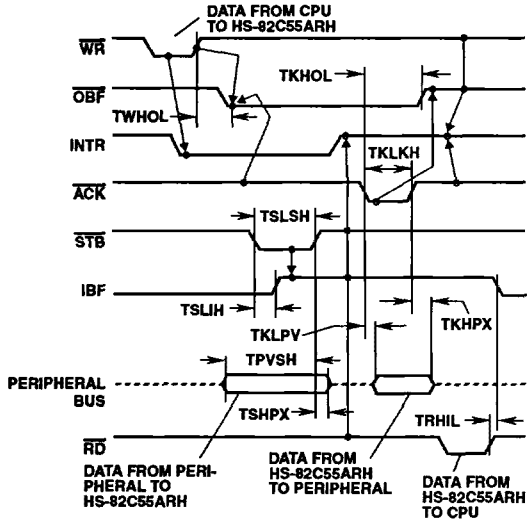


FIGURE 12. MODE 2 (BIDIRECTIONAL)



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

FIGURE 13. MODE 2 (BIDIRECTIONAL)

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	← →	
AP1	In	Out	In	Out	← →	
PA2	In	Out	In	Out	← →	
PA3	In	Out	In	Out	← →	
PA4	In	Out	In	Out	← →	
PA5	In	Out	In	Out	← →	
PA6	In	Out	In	Out	← →	
PA7	In	Out	In	Out	← →	
PB0	In	Out	In	Out	-	Mode 0 or Mode 1 Only
PB1	In	Out	In	Out	-	
PB2	In	Out	In	Out	-	
PB3	In	Out	In	Out	-	
PB4	In	Out	In	Out	-	
PB5	In	Out	In	Out	-	
PB6	In	Out	In	Out	-	
PB7	In	Out	In	Out	-	
PC0	In	Out	INTR B	INTR B	I/O	
PC1	In	Out	IBF B	$\overline{OBF}$ B	I/O	
PC2	In	Out	$\overline{STB}$ B	$\overline{ACK}$ B	I/O	
PC3	In	Out	INTR A	INTR A	INTR A	
PC4	In	Out	$\overline{STB}$ A	I/O	$\overline{STB}$ A	
PC5	In	Out	IBF A	I/O	IBF A	
PC6	In	Out	I/O	$\overline{ACK}$ A	$\overline{ACK}$ A	
PC7	In	Out	I/O	$\overline{OBF}$ A	$\overline{OBF}$ A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}$A	INTEA	I/O	I/O	INTRA	INTEB	$\overline{OBF}$B	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}$A	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

NOTE: (Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG*	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or STBB (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2