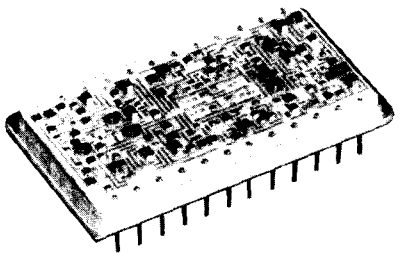
VIDEO TRACK/HOLD HYBRID 10 NSEC ACQUISITION TIME 0.1% LINEARITY ERROR



FEATURES

- *20 PSEC APERTURE JITTER*
- *100 MHz BANDWIDTH*
- *50 MHz SAMPLING RATE*
- *9 NSEC SETTLING TIME*
- *-55°C TO +125° C OPERATING TEMPERATURE RANGE*
- *MIL-STD-883 SCREENING AVAILABLE*
- *ECL COMPATIBLE*

C

DESCRIPTION

The TH-8530 is a video speed track/hold amplifier packaged in a hermetic 24 pin DDIP. Its 10 nanosecond acquisition time to 0.1% of final value makes it the fastest track/hold of its type. With 0.1% linearity error and 100 MHz bandwidth, the TH-8530 is ideal for applications with sampling rates to 50MHz. For military requirements, models are available with -55°C to +125°C operating temperature range and screening in accordance with MIL-STD-883. Additional features include 9 nanosecond track-to-hold mode settling time, 1 millivolt per microsecond droop rate, and a slew rate of 400 volts per microsecond.

With its high speed and accuracy, wide operating temperature range, and small hermetic package, the TH-8530 is ideal for the most demanding military and commercial data acquisition requirements. Typical applications include pulse processing, radar and TV digitizing and very high speed instrumentation.

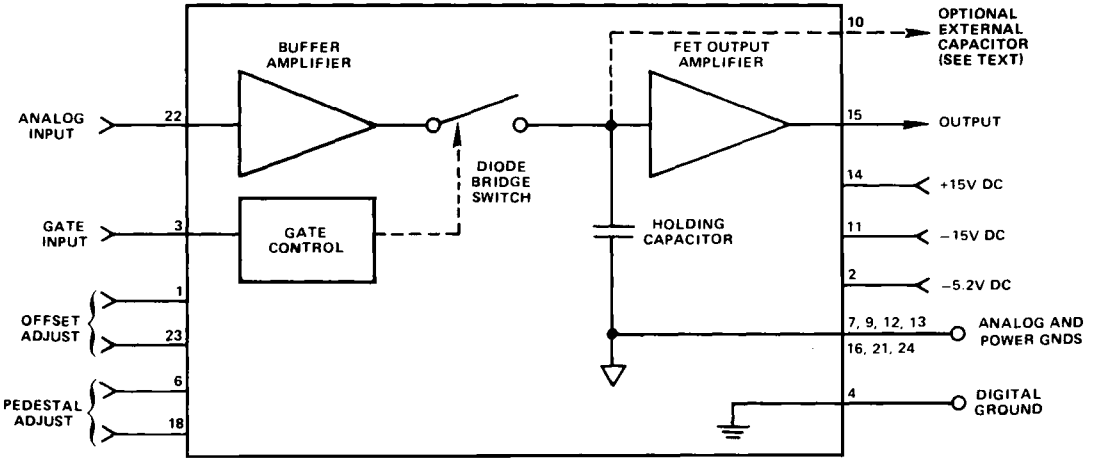


FIGURE 1. TH-8530 BLOCK DIAGRAM

TH-8530 SPECIFICATIONS
At 25°C case temperature and rated supplies unless otherwise indicated.

PARAMETER	UNITS	VALUE
ACCURACY		
Gain		
No load		+0.97 typ
With 200 Ω Rated Load		+0.95 typ; +0.92 min
Gain Tempco	ppm/°C	25 typ; 50 max
Linearity Error		
1mA max load	% of F.S.	0.012
At Rated Load	% of F.S.	0.2 max
Linearity Tempco	ppm/°C	5 typ; 15 max
Offset (1)	mV	25 typ; 100 max
(Trimmable to Zero)		
Offset Tempco (1)	mV/°C	0.2 typ; 0.5 max
Pedestal	mV	25 typ; 100 max
(Trimmable to Zero)		
Pedestal Tempco	μV/°C	60 typ; 150 max
DYNAMICS		
Small-Signal Bandwidth (f_t)	MHz	100 typ; 80 min
Slew Rate	V/μsec	400 min
Update Change	V	2 max
Max Sampling Rate (2)	MHz	50 typ; 33 min.
Min Cycle Time	ns	20 typ; 33 max
Aquisition Turn-On Delay	ns	3.5 typ; 7 max
Acquisition Time to		
0.1% of Final Value		
2V Input Change	ns	10 typ; 15 max
0.2V Input Change	ns	5 typ; 8 max
Aperture Time Delay	ns	3.5 typ; 5 max
Aperture Time Uncertainty (Jitter)	ps	20 typ; 35 max
Feedthrough Attenuation in Hold Mode	dB	60 min through 10 MHz
Settling Time to 0.1% of Final Value (3)	ns	9 typ; 15 max
Droop Rate at 25°C (Case)	mV/μs	1 typ; 10 max
Droop Rate Vs. Temp		Doubles every 10°C
Glitch (From Track to Hold)		
Amplitude	mV	20
Duration	ns	15 (to less than 2mV)

TH-8530 SPECIFICATIONS CONTINUED

PARAMETER	UNITS	VALUE
ANALOG INPUT		
Range For Rated Accuracy	V	±1 max
Absolute Max Without Damage	V	±2.5
Input Impedance	KΩ	100 typ; 20 min
Capacitance	pF	5 typ; 8 max
Bias Current	mA	±0.1 typ; ±0.5 max
GATE INPUT		
Type		ECL compatible (external pulldown req'd.)
Logic Levels	V	-0.8 = Logic 1 = Hold -1.6 = Logic 0 = Track
OUTPUT		
Voltage Range	V	±1 max
Steady State Current	mA	±5 max
Transient Current	mA	±50 max
Output Impedance	Ω	4 typ; 10 max
POWER SUPPLIES		
Supply Voltages	V	+15 -15 -5.2
Voltage Tolerance	%	±5 ±5 ±5
Absolute Max Voltage	V	+18 -18 -7
Current	mA	55typ 55typ 45typ 65max 65max 65max
Power Dissipation	W	1.9 average
TEMPERATURE RANGE [CASE]		
Operating		
—1 Option	°C	-55 to +125
—3 Option	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL		
Type		24 pin DDIP
Size	inch (mm)	1.4 x 0.8 x 0.2 (36 x 20.5 x 5)
Weight	oz (g)	.42 typ (11.9)

Notes:
(1) Measured during 50ns track time with input grounded.
(2) Sampling rate for 0.1% dynamic error.
(3) Settling time into Hold mode.

GENERAL

The TH-8530 track and hold amplifier (figure 1) includes a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltages are both buffered by amplifiers. The switch is controlled by an ECL logic gate signal which determines whether the holding capacitor voltage and output voltage will track the input signal (switch closed, logic 0) or will be held constant, retaining the value of the input at the moment the switch opens (switch open, logic 1).

The TH-8530 is available in several optional configurations. Provision for the use of an external holding capacitor has been made available on pin 10 (see Pin Connection Table). Because the external capacitor is connected in parallel with the internal capacitor, this option reduces the effects of droop and extends holding time. Acquisition time, however, is increased by the presence of additional capacitance created by this circuitry. This option is designated as "-10" when ordering the TH-8530 (see Ordering Information).

Unipolar voltage outputs may be ordered, which provide internal offsets of the specified ±1V input range. Option "P" produces 0 to +2V and option "N" produces 0 to -2V at the output (pin 15). A bipolar output range is available as option "B" (see Ordering Information).

TRIM ADJUSTMENTS

The offset and pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made using the trim adjustments shown in figure 2. Connect the output (pin 15) to an oscilloscope and ground the analog input (pin 22). Apply a 50 nsec negative ECL pulse at a 1 MHz rate to the gate input. Vary the pedestal adjust potentiometer to minimize the pedestal and the offset potentiometer to trim the offset as shown in figure 3.

GROUNDING

To minimize coupling of a gate signal into an output signal, connect the gate signal ground to pin 4 only. Do not connect other grounds to pin 4. Analog input/output and supply voltage grounds can be connected to any of the analog

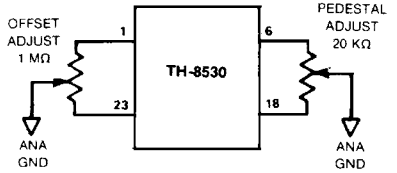


FIGURE 2. TRIM ADJUSTMENT CIRCUITS

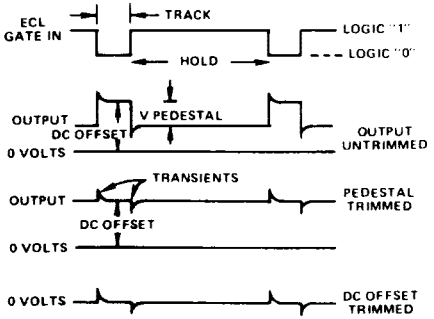


FIGURE 3. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

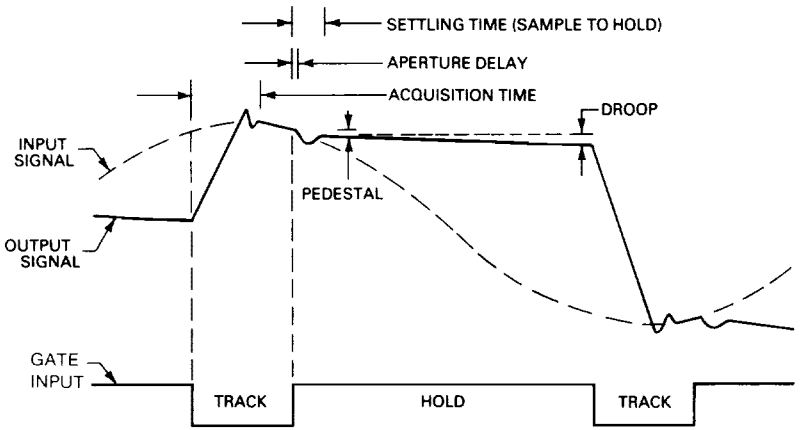


FIGURE 4. INPUT/OUTPUT CHARACTERISTICS

ground pins. The analog grounds are connected together internally and tied to the case. It is best to also connect these grounds together externally to minimize impedances. The analog and digital grounds are separated internally to avoid crosstalk between them and must be tied together externally.

Attention must be paid to proper high frequency grounding techniques in order to get the most performance from the TH-8530. It is highly desirable to use a large area ground plane under the track/hold. This will maintain a low impedance return path at all frequencies of interest. Each of the ground pins on the track/hold package must be connected to ground as close to the package as possible, in order to avoid voltage differences between the ground pins.

POWER SUPPLY DECOUPLING

The TH-8530 provides internal ceramic decoupling capacitors on the power supply lines. In most applications it is desirable to add external 1μf tantalum capacitors. These decoupling capacitors should be mounted as close as possible to the hybrid package to avoid high frequency power supply line drops.

INPUT/OUTPUT CHARACTERISTICS

As shown in the diagram of figure 4, the track interval is initiated when the Gate Input is brought LOW. The output slews as the hold capacitor is charged to a new value. Acquisition time is defined as the time required for the output to settle to within a given error band of its final value. Acquisition time for any interval depends on the magnitude of the voltage change since the last interval. The minimum track time must be at least as long as the acquisition time for the largest possible input change.

The hold interval is initiated when the Gate Input is brought HIGH. As shown in Figure 4, there is a short delay, the Aperture Delay, before the series switch opens to isolate the hold capacitor from the analog input. The uncertainty in this delay, called Aperture Jitter, causes an error in the output when the input slews fast.

After the Gate Input goes HIGH, a transient appears on the output due to charge transfer across the series switch. A Settling Time (Sample to Hold) interval elaspses before the output reaches a given error band of its final value. The track/hold output has not achieved rated performance until after this settling time interval has elapsed.

The charge transferred across the series switch onto the hold capacitor when the Gate Input goes HIGH causes a step error at the output. This Pedestal error is constant for every hold interval and does not vary with input voltage.

During the hold interval, the output voltage will increase or decrease linearly with time. This Droop error is caused by charging of the hold capacitor by bias current or series switch leakage current.

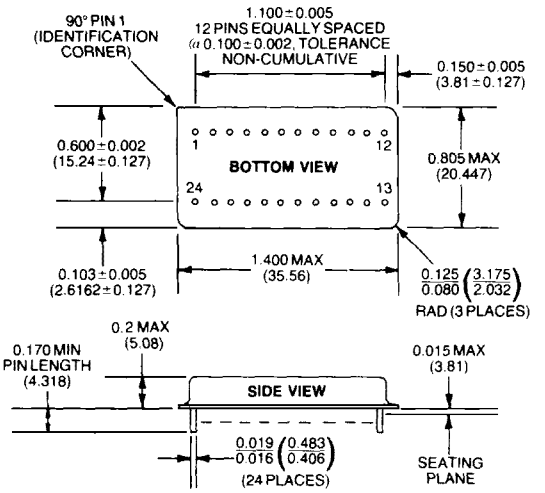
Another source of error, during the hold interval, is Feedthrough. Even though the series switch is open, fast slewing input signals can cause the output to change by voltage division across the open switch capacitance. The output error that results will be equal to the input voltage divided by the feedthrough attenuation.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Offset Adjust	13	Analog Ground
2	—5.2 VDC	14	+15 VDC
3	Gate Input	15	Output
4	Digital Ground	16	Analog Ground
5	NC	17	NC
6	Pedestal Adjust	18	Pedestal Adjust
7	Analog Ground	19	NC
8	NC	20	NC
9	Analog Ground	21	Analog Ground
10	NC (See Note)	22	Analog Input
11	—15 VDC	23	Offset Adjust
12	Analog Ground	24	Analog Ground

Note: Pin 10 for external capacitor on special order only.

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



Notes:
(1.) Dimensions are shown in inches (millimeters).
(2.) Load identification numbers are for reference only.
(3.) Lead spacing dimensions apply only at seating plane.
(4.) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
(5.) Case tied to analog ground.

ORDERING INFORMATION

TH-8530 - 1 - B - 10 - 883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL- STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- 10 = Pin 10 connected to the holding capacitor.
  - Blank = No Connection.
- Output Voltage Range (all with ± 1V input):
  - B = -1V to +1V
  - N = 0 to -2V
  - P = 0 to +2V
- Temperature Range (Case):
  - -1 = -55°C to +125°C
  - -3 = 0°C to +70°C

H