

# HD74AC257/HD74ACT257 • Quad 2-Input Multiplexer with 3-State Output.

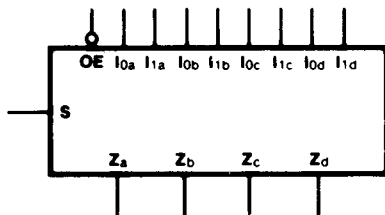
Preliminary

## Description

The HD74AC257/HD74ACT257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic High on the common Output Enable ( $\overline{OE}$ ) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- HD74ACT257 has TTL-Compatible Inputs

## Logic Symbol



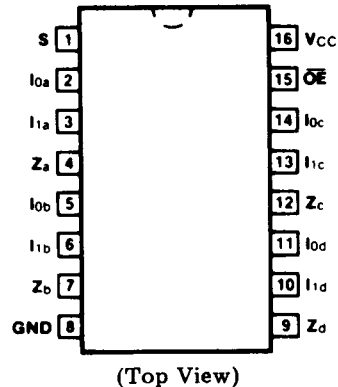
## Pin Names

S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
$I_{0a}$ - $I_{0d}$	Data Inputs from Source 0
$I_{1a}$ - $I_{1d}$	Data Inputs from Source 1
$Z_a$ - $Z_d$	3-State Multiplexer Outputs

## Functional Description

The HD74AC257/HD74ACT257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is Low, the  $I_{0x}$  inputs are selected and when Select is High, the  $I_{1x}$  inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

## Pin Assignment



$$Z_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

$$Z_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$Z_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input ( $\overline{OE}$ ) is High, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

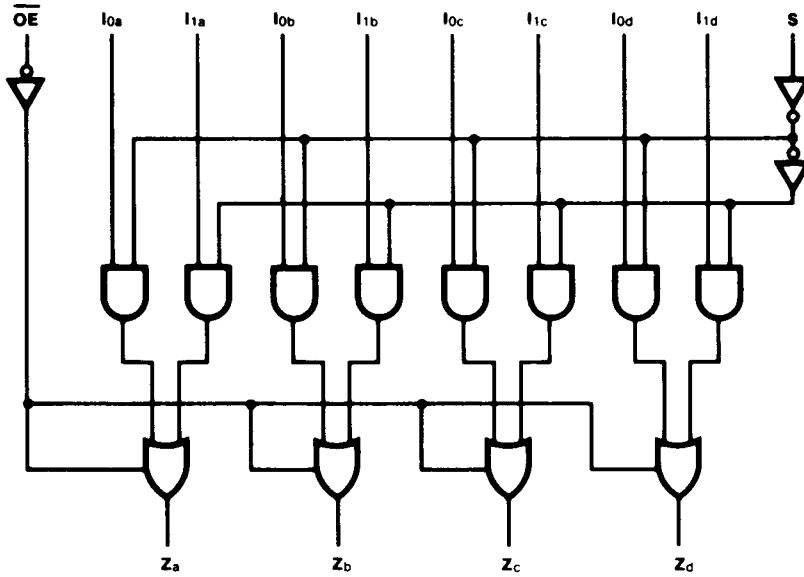
## Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	$I_0$	$I_1$	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High Voltage Level  
 L = Low Voltage Level  
 X = Immaterial  
 Z = High Impedance

# HD74AC257/HD74ACT257

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
$I_{CC}$	Maximum Quiescent Supply Current	80	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5V$ , $T_a = \text{Worst Case}$
$I_{CC}$	Maximum Quiescent Supply Current	8.0	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5V$ , $T_a = 25^\circ C$
$I_{CC_T}$	Maximum Additional $I_{CC}$ /Input (HD74ACT257)	1.5	mA	$V_{IN} = V_{CC} - 2.1V$ , $V_{CC} = 5.5V$ , $T_a = \text{Worst Case}$

**AC Characteristics: HD74AC257**

Symbol	Parameter	V <sub>CC</sub> * (V)	T <sub>a</sub> = +25°C C <sub>L</sub> = 50pF			T <sub>a</sub> = -40°C to +85°C C <sub>L</sub> = 50pF		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay In to Zn	3.3 5.0		5.0 4.0				ns
t <sub>PHL</sub>	Propagation Delay In to Zn	3.3 5.0		6.0 4.5				ns
t <sub>PLH</sub>	Propagation Delay S to Zn	3.3 5.0		7.0 5.0				ns
t <sub>PHL</sub>	Propagation Delay S to Zn	3.3 5.0		7.5 5.5				ns
t <sub>PZH</sub>	Output Enable Time	3.3 5.0		6.5 5.0				ns
t <sub>PZL</sub>	Output Enable Time	3.3 5.0		5.5 5.0				ns
t <sub>PHZ</sub>	Output Disable Time	3.3 5.0		5.5 5.0				ns
t <sub>PLZ</sub>	Output Disable Time	3.3 5.0		5.5 5.0				ns

\*Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

**AC Characteristics: HD74ACT257**

Symbol	Parameter	V <sub>CC</sub> * (V)	T <sub>a</sub> = +25°C C <sub>L</sub> = 50pF			T <sub>a</sub> = -40°C to +85°C C <sub>L</sub> = 50pF		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay In to Zn	5.0	1.0	5.0	7.0	1.0	7.5	ns
t <sub>PHL</sub>	Propagation Delay In to Zn	5.0	1.0	6.0	7.5	1.0	8.5	ns
t <sub>PLH</sub>	Propagation Delay S to Zn	5.0	1.0	7.0	9.5	1.0	10.5	ns
t <sub>PHL</sub>	Propagation Delay S to Zn	5.0	1.0	7.0	10.5	1.0	11.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	1.0	6.0	8.0	1.0	9.0	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.0	6.0	8.0	1.0	9.0	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.0	6.5	9.0	1.0	10.0	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	6.0	7.5	1.0	8.5	ns

\*Voltage Range 5.0 is 5.0V ± 0.5V

**Capacitance**

Symbol	Parameter	Typ	Unit	Condition
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.5V
C <sub>PD</sub>	Power Dissipation Capacitance	50.0	pF	V <sub>CC</sub> = 5.0V

# Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.  
 To order, please refer to the following package code.

• Package code of Advanced CMOS Logic

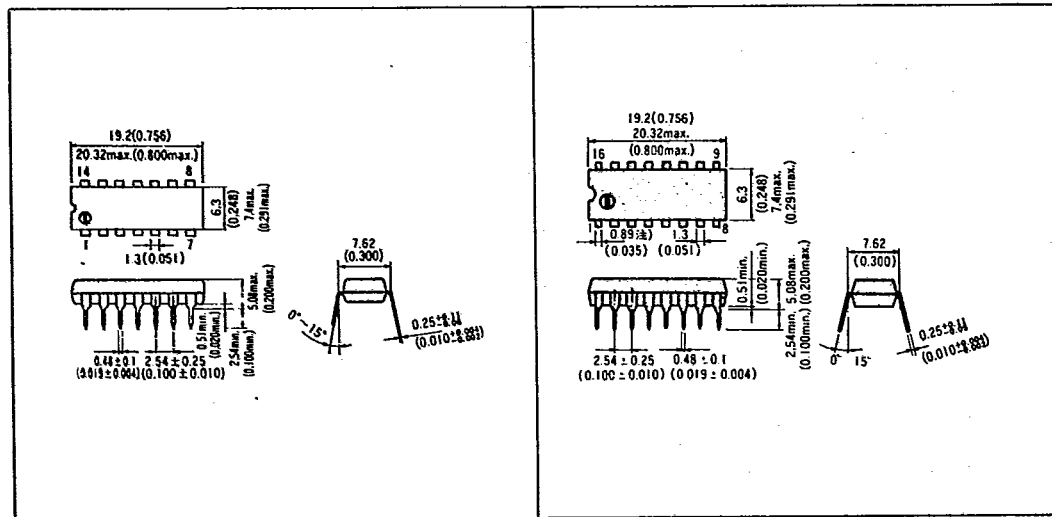
## HD74AC XXXX P

Package code  
 P: Plastic DIP,  
 FP: Small outline package  
 Individual device code  
 74AC: Commercial FACT  
 74ACT: Commercial  
 TTL-Compatible  
 Advanced CMOS  
 Initial cad of Hitachi  
 digital IC

Plastic DIP Package [Unit: mm (inch)]

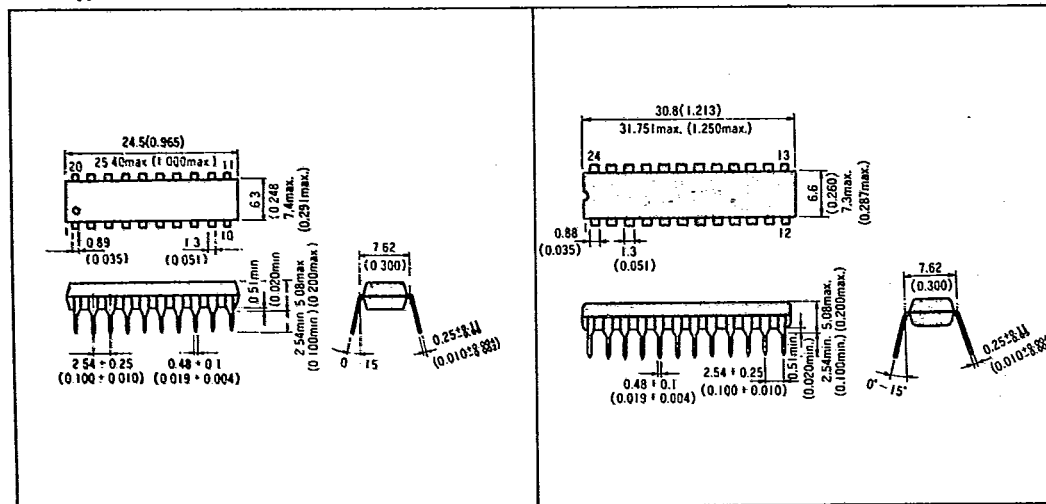
14 Pin type

16 Pin type



20 Pin type

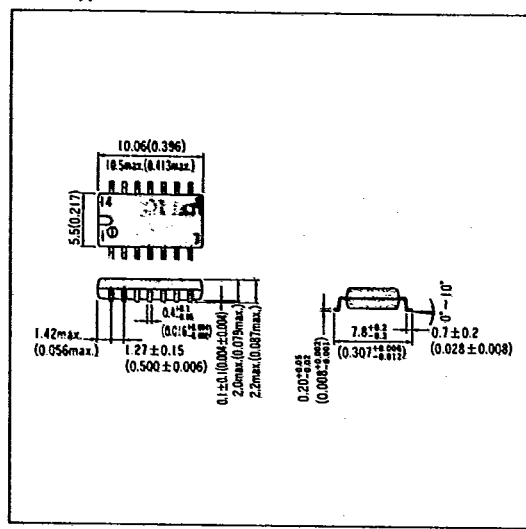
24 Pin type



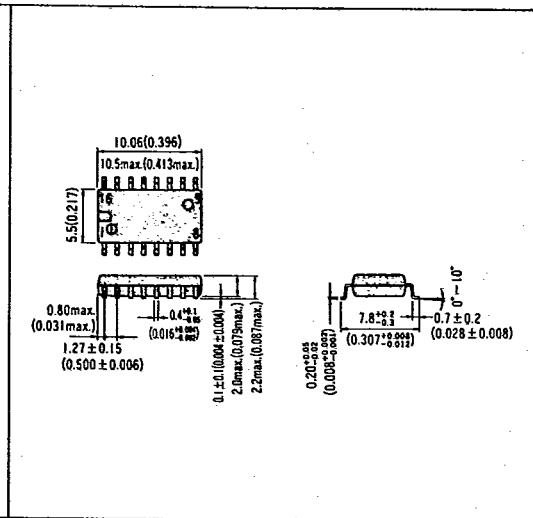
### Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



16 Pin type



20 Pin type

