AT&T Microelectronics

# 41LF, 41LR, 41LS, and 41LT Quad Differential Line Receivers

## Features

- Pin equivalent to the general-trade 26LS32 device, with improved speed and reduced power consumption
- High input impedance ≈ 8 kΩ*
- Four line receivers per package
- Logic which converts differential logic levels to TTL output logic levels
- 200 Mbits/s maximum data rate when used with the 41L*x* or 41M*x* drivers
- Meets ESDI standards
- 7 ns maximum propagation delay
- <0.20 V input sensitivity (typical)
- −1.2 V to +7.2 V common-mode range
- 0 °C to 85 °C ambient operating temperature range (See Section 9.)
- Single 5 V supply
- Output defaults to logic 1 when inputs are left open†

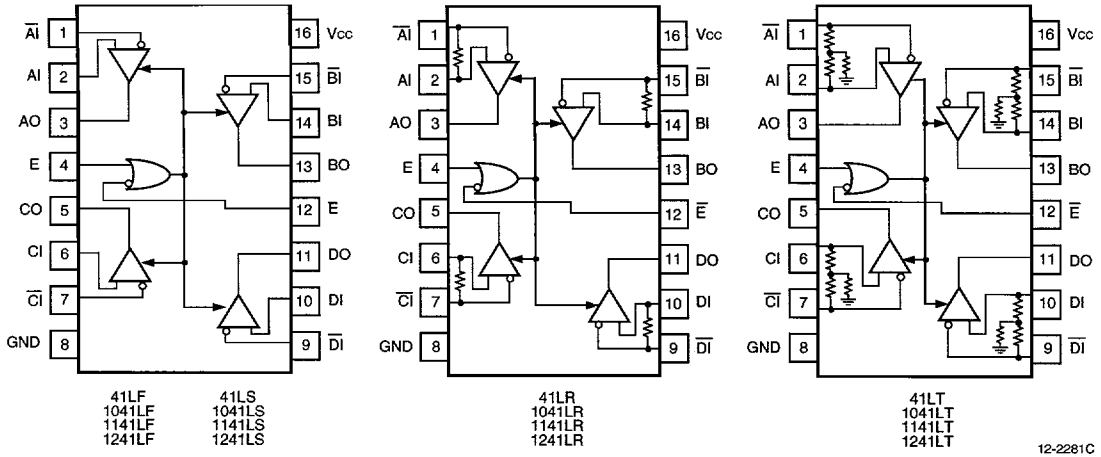
* Except 41LR and 41LT which have built-in resistors.
† This feature is available on all device types except the 41LF.

## Description

The 41LF, 41LR, 41LS, 41LT Quad Differential Line Receiver integrated circuits receive digital data over balanced transmission lines. They translate differential input logic levels to TTL output logic levels. All devices in this family have four receivers with a common enable function. The 41LF, 41LR, 41LS, 41LT receivers are pin equivalent to the general-trade 26LS32 devices, but offer increased speed and decreased power consumption. The 41LF and 41LS receivers require the customer to supply external termination resistors on the circuit board. The 41LR receivers have a 110 Ω termination resistor between the differential inputs of each receiver. The 41LT receivers have a 120 Ω termination resistor, which is centertapped by a 90 Ω resistor to ground, between the differential inputs of each receiver. The 41LS is functionally equivalent to the 41LF except that the 41LS has the output default feature listed on the left.

The packaging options that are available for the quad differential line receivers include a 16-pin DIP (41LF, 41LR, 41LS, 41LT), a 16-pin J-lead SOJ (1041LF, 1041LR, 1041LS, 1041LT), a 16-pin gull-wing SOIC (1141LF, 1141LR, 1141LS, 1141LT), and a 16-pin narrow-body gull-wing SOIC (1241LF, 1241LR, 1241LS, 1241LT).

## Pin Information




Note: The device is disabled when E = 0 and Ē = 1.

**Figure 4-1. 41LF, 41LR, 41LS, and 41LT Logic Diagrams**

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage | Vcc | — | 7.0 | V |
| Ambient Operating Temperature | $T_A$ | 0 | 85 | °C |
| Storage Temperature | $T_{stg}$ | –40 | 125 | °C |

## Handling Precautions

**CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).**

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. 41 Series receiver differential inputs are not equipped with ESD protection. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltages presented here were obtained using this circuit.

| HBM ESD Threshold Voltage | |
|---|---|
| **Device** | **Rating** |
| 41 Series Receiver | |
| Differential Inputs (LF, LS) | >100 V |
| (LR, LT) | >1000 V |
| All other pins | >2000 V |

# Electrical Characteristics

### Table 4-1. 41LF, 41LR, 41LS, and 41LT Power Supply Current Characteristics

$T_A$ = 0 °C to 85 °C, $V_{CC}$ = 5 V ± 0.5 V.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Current: | | | | | |
| 41LF, 41LR, 41LS, and 41LT | | | | | |
| All Outputs Disabled | $I_{CC}$ | — | 35 | 50 | mA |
| All Outputs Enabled | $I_{CC}$ | — | 25 | 40 | mA |

### Table 4-2. 41LF, 41LR, 41LS, and 41LT Voltage and Current Characteristics

$T_A$ = 0 °C to 85 °C.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage, $V_{CC}$ = 4.5 V: | | | | | |
| Low, $I_{OL}$ = 8.0 mA | $V_{OL}$ | — | — | 0.5 | V |
| High, $I_{OH}$ = –400 µA | $V_{OH}$ | 2.5 | — | — | V |
| Enable Input Voltages: | | | | | |
| Low, $V_{CC}$ = 5.5 V | $V_{IL}$* | — | — | 0.7 | V |
| High, $V_{CC}$ = 4.5 V | $V_{IH}$* | 2.0 | — | — | V |
| Minimum Differential Input Voltage, $V_{IH} - V_{IL}$:† | | | | | |
| –0.80 V < $V_{IH}$ < 7.2 V, –1.2 V < $V_{IL}$ < 6.8 V | $V_{TH}$* | — | 0.1 | 0.20 | V |
| Input Offset Voltage | $V_{OFF}$‡ | — | 0.15 | — | V |
| Output Currents, $V_{CC}$ = 5.5 V: | | | | | |
| Off-state (high Z), $V_O$ = 0.4 V | $I_{OZL}$ | — | — | –20 | µA |
| Off-state (high Z), $V_O$ = 2.4 V | $I_{OZH}$ | — | — | 20 | µA |
| Short Circuit | $I_{OS}$§ | –25.0 | — | –100 | mA |
| Enable Input Currents, $V_{CC}$ = 5.5 V: | | | | | |
| Low, $V_{IN}$ = 0.4 V | $I_{IL}$ | — | — | –400 | µA |
| High, $V_{IN}$ = 2.7 V | $I_{IH}$ | — | — | 20 | µA |
| Reverse, $V_{IN}$ = 5.5 V | $I_{IH}$ | — | — | 100 | µA |
| Differential Input Currents (41LF, 41LS): | | | | | |
| Low, $V_{IN}$ = –1.2 V | $I_{IL}$ | — | — | –1.0 | mA |
| High, $V_{IN}$ = 7.2 V | $I_{IH}$ | — | — | 1.0 | mA |
| Differential Input Impedance (41LR) | | | | | |
| Connected Between $RI^+$ and $RI^-$ | $R_0$ | — | 110 | — | Ω |
| Differential Input Impedance (41LT)** | $R_1$ | — | 60 | — | Ω |
| | $R_2$ | — | 90 | — | Ω |

* The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

† Outputs of unused receivers assume a logic 1 level when the inputs are left open. (This feature is available on all devices except the 41LF receivers.)

‡ Input offset is not applicable to 41LF devices.

§ Test must be performed one lead at a time to prevent damage to the device

** See Figure 4-2.

Note: It is recommended that all unused positive inputs be tied to the positive power supply for the 41LF and 41LS parts.

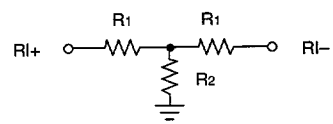



**Figure 4-2. 41LT Termination Resistor Configuration**

## Timing Characteristics

**Table 4-3. 41LF, 41LR, 41LS, and 41LT Timing Characteristics** (See Figures 6-3 and 6-4.)

Output propagation-delay test circuit connected to output (see Figure 6-8).

$T_A$ = 25 °C, $V_{CC}$ = 5 V.

| Symbol | Parameter | Typ | Max | Unit |
|---|---|---|---|---|
| | Propagation Delay: | | | |
| $t_{PLH}$ | Input to Output High | 3.5 | 7.0 | ns |
| $t_{PHL}$ | Input to Output Low | 4.5 | 7.0 | ns |
| | Disable Time, $C_L$ = 5 pF: | | | |
| $t_{PHZ}$ | High to High Impedance | 10 | 15 | ns |
| $t_{PLZ}$ | Low to High Impedance | 10 | 15 | ns |
| | Enable Time, $C_L$ = 5 pF: | | | |
| $t_{PZH}$ | High Impedance to High | 10 | 15 | ns |
| $t_{PZL}$ | High Impedance to Low | 10 | 15 | ns |