MSM6310

PCM RECORDING & PLAYBACK LSI

GENERAL DESCRIPTION

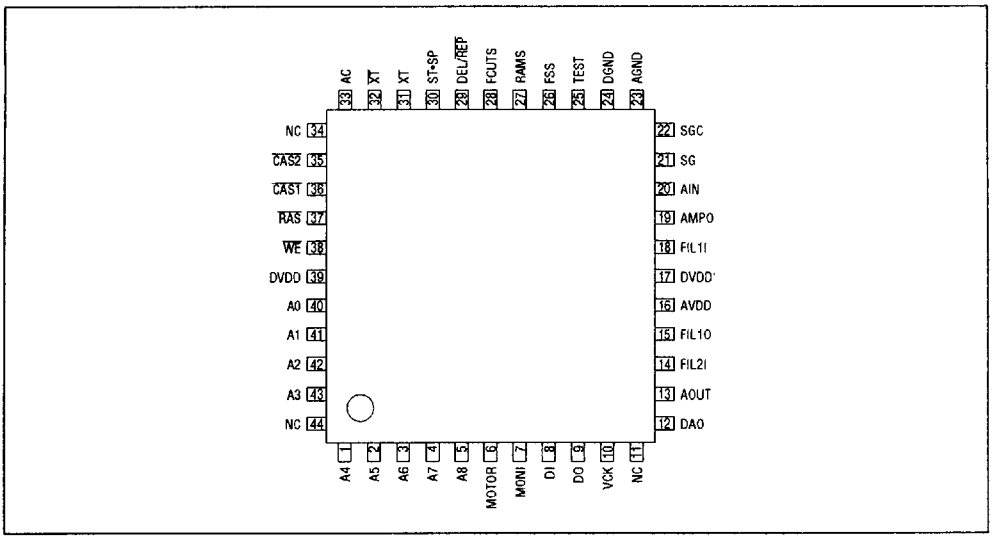
The MSM6310 is a PCM recording & playback LSI which is manufactured using Oki's low power CMOS silicon gate technology. The MSM6310 is designed for the purpose of endless loop recording by 8-bit PCM.

The internal circuit is made up of following three units. The first one is an input unit which consists of line amplifier, low pass filter and 8-bit AD converter. The second one is an output unit which consists of 8-bit DA converter and low pass filter. The third one is a control unit for external DRAMs.

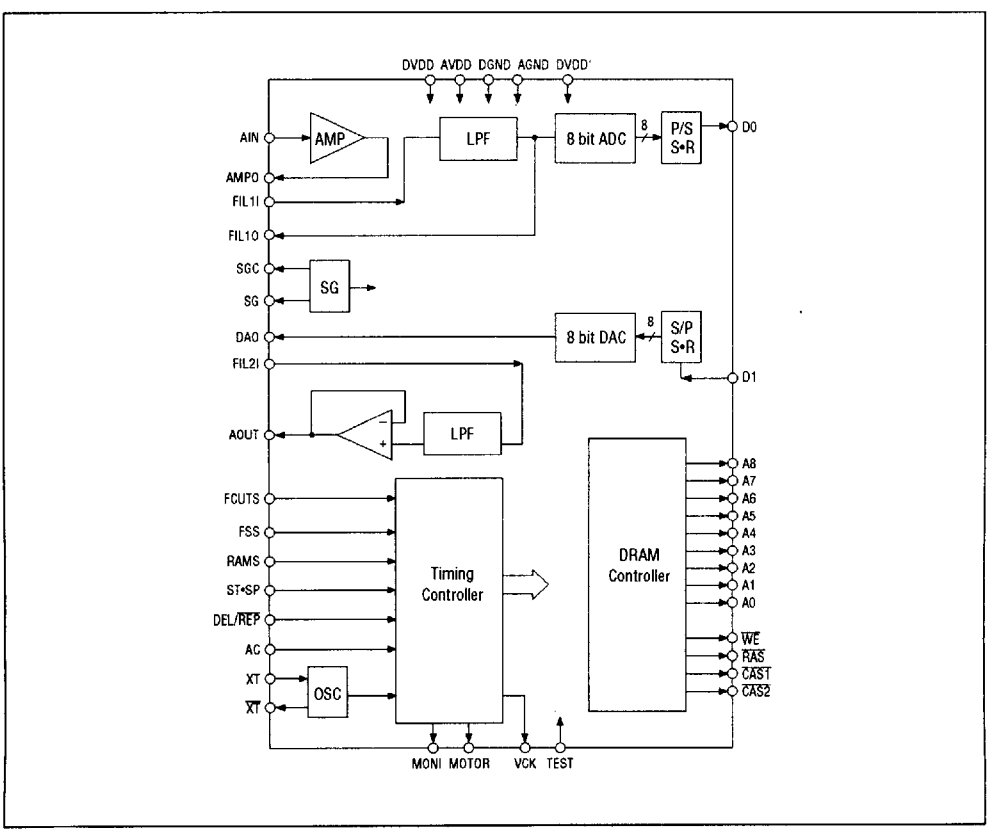
FEATURES

- 8-bit PCM
  (built-in 8-bit AD/DA converter)
- External DRAM driving capability 256K, 2 pcs.
  *256K DRAM type → 256KW x 1 bit
  (MSM41256A) $\overline{CAS}$ before $\overline{RAS}$ refresh
- Sampling frequency:
  4 kHz (f_{osc}=4.096 MHz)
- Oscillation frequency:
  4 to 8.2 MHz (nominally 4.096 MHz)
- Supply voltage: +5V
- Analog line input
- Motor driving signal output
- Recording/Playback period:
  4 sec (f_S=4kHz, 1 x 256K DRAM)
  8 sec (f_S=4kHz, 1 x 256K DRAM or f_S=8kHz, 2 x 256K DRAM)
  16 sec (f_S=4kHz, 2 x 256 K DRAM)
- 44 pin plastic QFP
  (QFP44-P-910-K)

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	V_{DD}	T_a = 25°C	−0.3 to 7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–	−55 to + 150	°C

Operating Range

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	V_{DD}	DGND = AGND = 0V	+4.5 to +5.5	V
Operating temperature range	T_{OP}	–	−40 to 85	°C
Oscillator frequency	F_{OSC}	–	4.0 to 8.2	MHz

• DC Electrical Characteristics

(DVDD=AVDD=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage (Note 1)	V_{IH1}	—	3.6	—	—	V
High input voltage (Note 2)	V_{IH2}	—	0.8xV_{DD}	—	—	v
Low input voltage	V_{IL}	—	—	—	0.8	v
High output voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	v
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	v
High input current (Note 3)	I_{IH1}	V_{IH} = V_{DD}	20	—	400	μA
High input current (Note 4)	I_{IH2}	V_{IH} = V_{DD}	—	—	10	μA
Low input current	I_{IL}	V_{IL} = V_{SS}	−10	—	—	μA
Output leak current	I_{LO}	$V_{SS} \leqq V_{OUT} \leqq V_{DD}$	−10	—	10	μA
Operating consumed current	I_{OD}	f_{OSC} = 4.096MHz	—	—	10	mA
DA output relative precision	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
AD conversion relative precision	$\lvert V_{ADE} \rvert$	—	—	—	40	mV

Note 1: Applicable to the input terminal excluding the XT terminal.
Note 2: Applicable to the XT terminal.
Note 3: Applicable to the terminals (ST, SP, TEST1) with a pulldown resistance.
Note 4: Applicable to the terminal without a pulldown resistance.

• AC Electrical Characteristics

f_{OSC}=4.096MHz, f_S=8.0kHz, V_{DD}=4.5~5.5V, DGND=AGND=0V, Ta=–40~+85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
ST-SP pulse amplitude	t_{STP}	35	—	—	ms
When DEL/$\overline{REP}$=L, time from start pulse input to the waveform output from the AOUT terminal	t_{SRA}	16	—	256	ms
When DEL/$\overline{REP}$=L, time from start pulse input to the rising edge of MOTOR terminal	t_{STM}	16	—	35	ms
When DEL/$\overline{REP}$=L, non-sound time from stop pulse input to rising edge of MOTOR terminal	t_{MS}	—	256	—	ms
When DEL/$\overline{REP}$=L, time from stop pulse input to MOTOR terminal	t_{SPM}	16	—	35	ms
Time from strat pulse input to rising edge of MONI terminal	t_{SMN}	16	—	35	ms
Time from strat pulse input to falling edge of MONI terminal	t_{PMN}	16	—	35	ms
Under condition 2.2), time from start pulse input to time from rising edge of MOTOR terminal	t_{SMT}	16	—	35	ms
Time from rising edge of DEL/$\overline{REP}$ to falling edge of MOTOR terminal	t_{DPM}	—	2	—	µs
Time from falling edge of DEL/$\overline{REP}$ to falling edge of MOTOR terminal	t_{RPM}	—	2	—	µs
VCK H level amplitude, VCK L level amplitude	t_{VH}, t_{VL}	—	62.5	—	µs
Time from falling edge of MONI terminal to rising edge of DEL/REP	t_{DRM}	—	2	—	µs
$\overline{RAS}$ pulse amplitude	t_{RAS}	—	4.4	—	µs
$\overline{CAS}$ pulse amplitude	t_{CAS}	—	3.9	—	µs
$\overline{WE}$ pulse amplitude	t_{WE}	—	1.0	—	µs
$\overline{RAS}$ precharge time	t_{RP}	—	0.5	—	µs
Time from rising edge of VCK to falling edge of $\overline{RAS}$	t_{VRP}	—	2.9	—	µs
Time from rising edge of VCK to falling edge of $\overline{CAS}$	t_{VCF}	—	4.9	—	µs
Time from rising edge of VCK to falling edge of $\overline{WE}$	t_{VWE}	—	6.8	—	µs

Note: All items are proportional to f_{OSC}. (If f_{OSC} is higher, the time is shorter.)

FUNCTIONAL DESCRIPTION

This description is based on the following conditions.

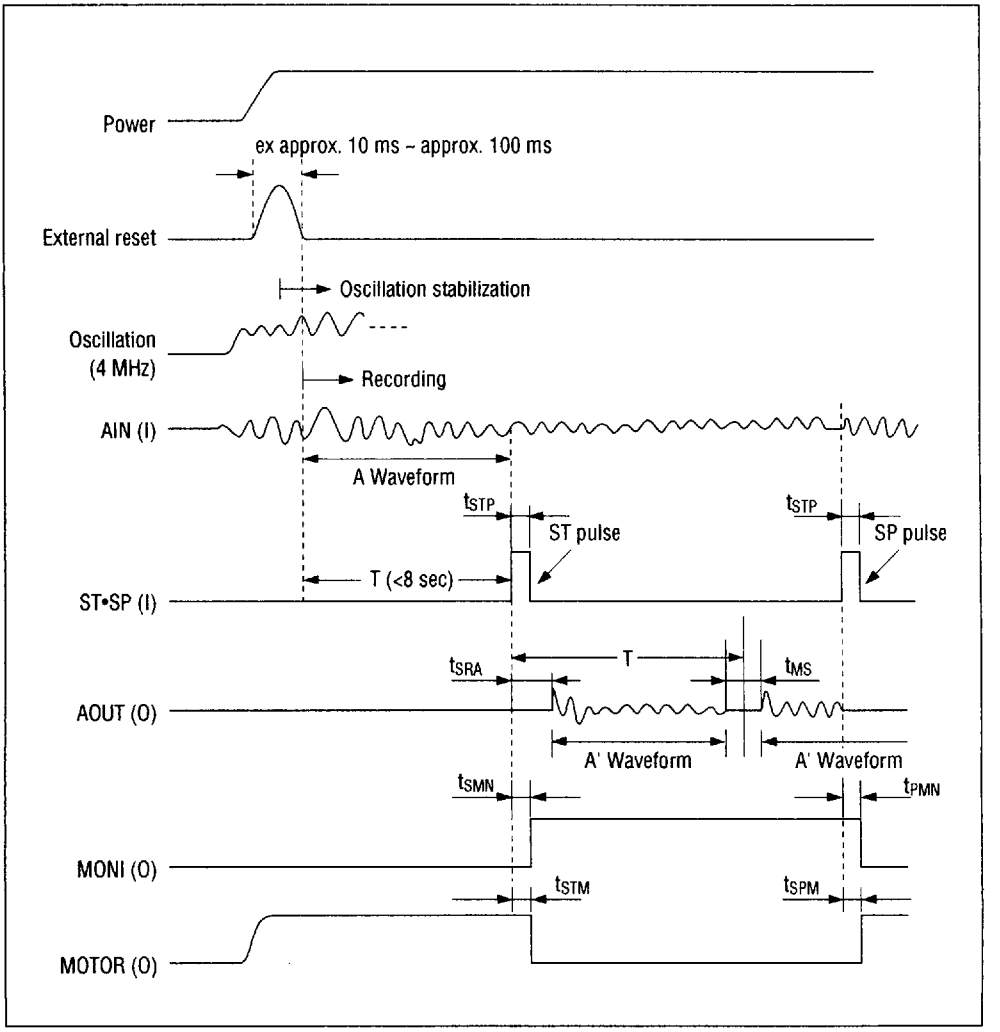
{ Sampling Frequency 8kHz
{ DRAM(256K bit) 2pcs

Basic Operation

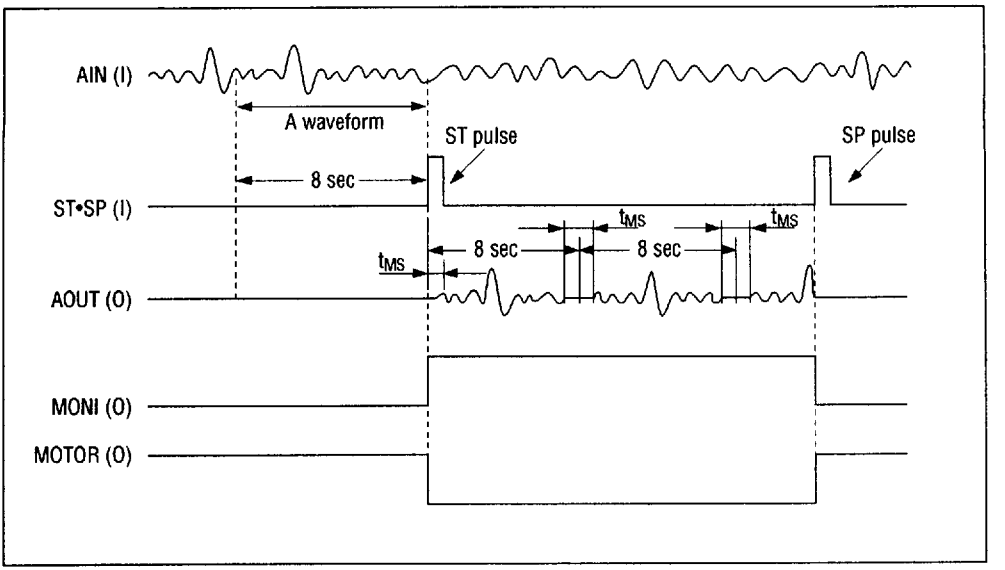
1. DEL/$\overline{\text{REP}}$="L" ..... REPEAT mode

1) After power is turned on, ST pulse is output within 8 sec.

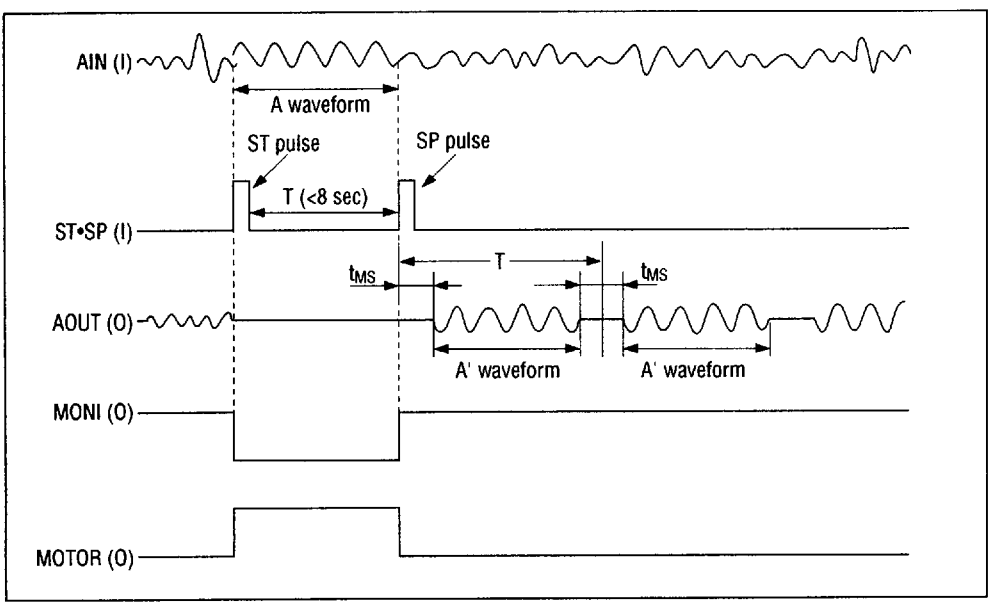
Basic Operation



2) After power is turned on, ST pulse is input 8 sec. later.



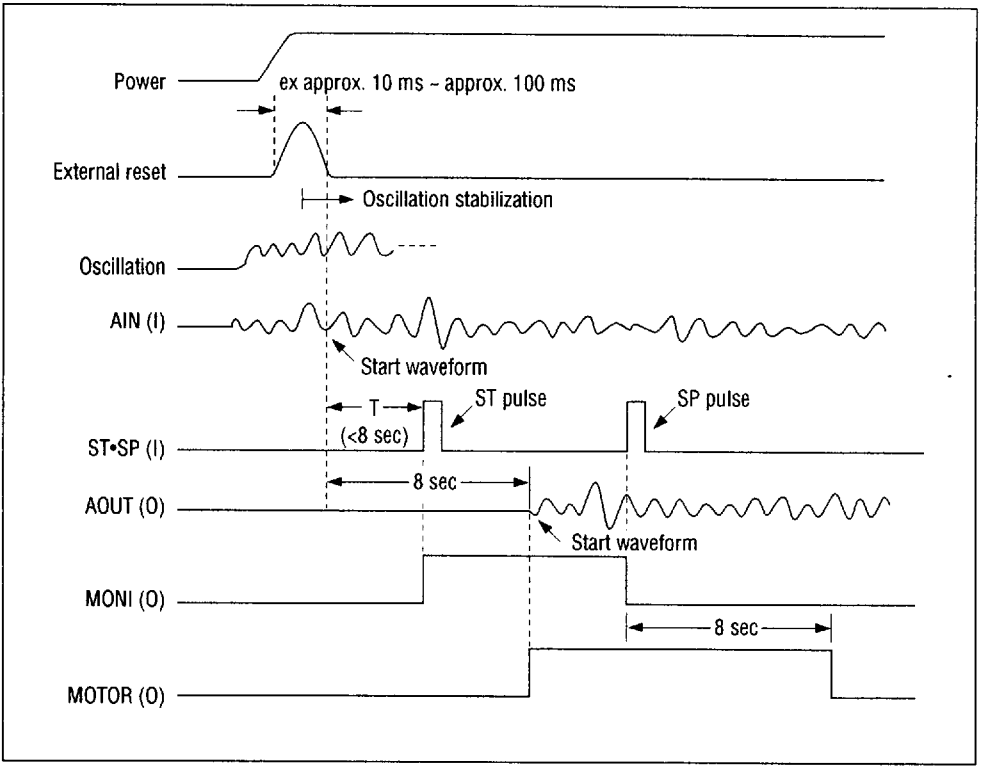
3) After inputting SP pulse, ST pulse is input within 8 sec.



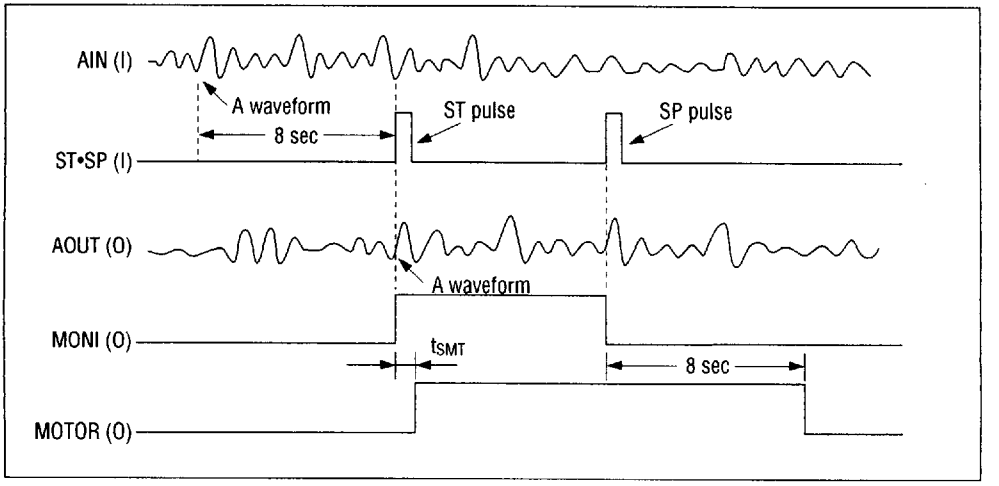
4) After inputting SP pulse, ST pulse is input 8 sec. later. Same as 2).

2. DEL/$\overline{\text{REP}}$="H" ..... DELAY mode

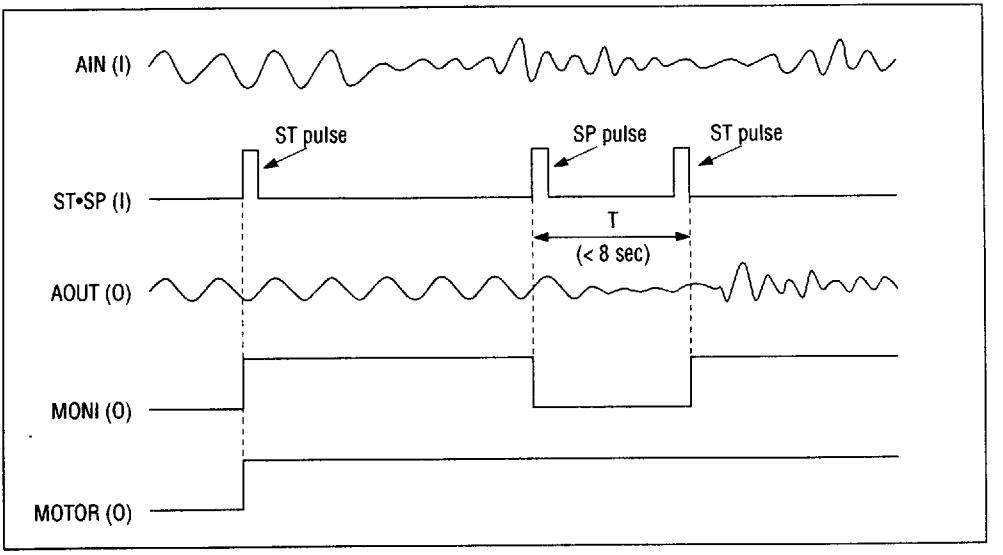
1) After power is turned on, ST pulse is input within 8 sec.



2) After powe is turned on, ST pulse is input 8 sec. later.



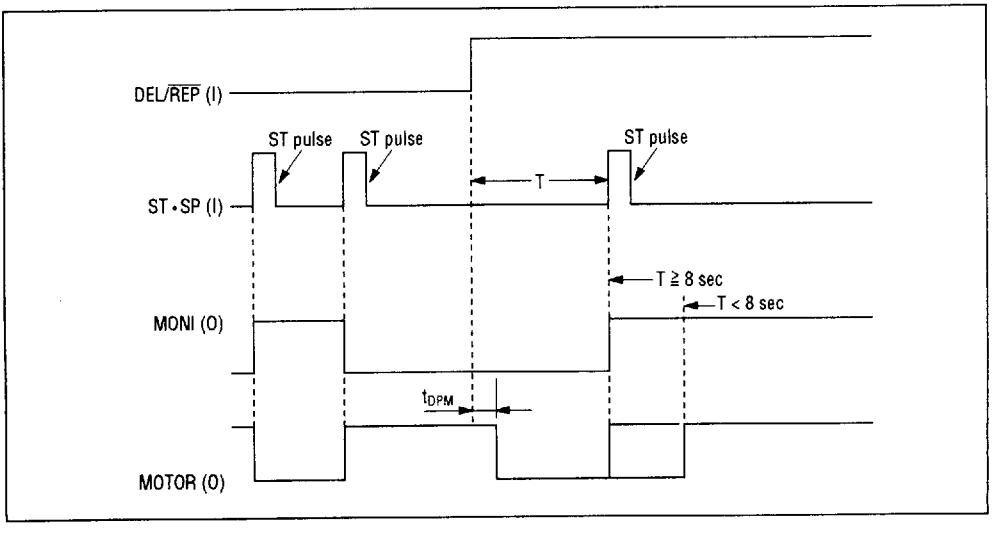
3) After SP pulse is input, ST pulse is input within 8 sec.



Change Operation during DEL/$\overline{\text{REP}}$

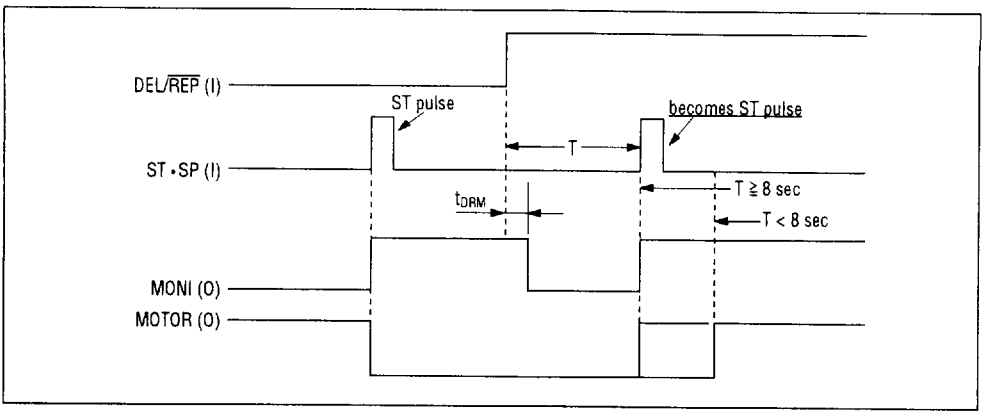
1. DEL/$\overline{\text{REP}}$="L" → "H"
   .....from REPEAT mode
   to DELAY mode

1) Change operation is activated after SP pulse (before ST pulse)



Note 1: If T is 8 sec. or longer, MOTOR rises at the same time when ST pulse is input.
Note 2: If T is 8 sec. or shorter, MOTOR rises 8 seconds after DEL/$\overline{\text{REP}}$ is selected.

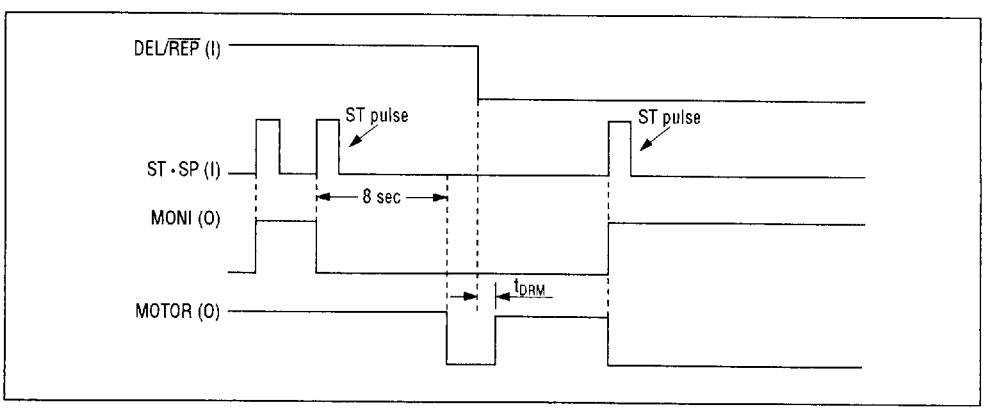
2) Change operation is activated after ST pulse (before SP pulse)



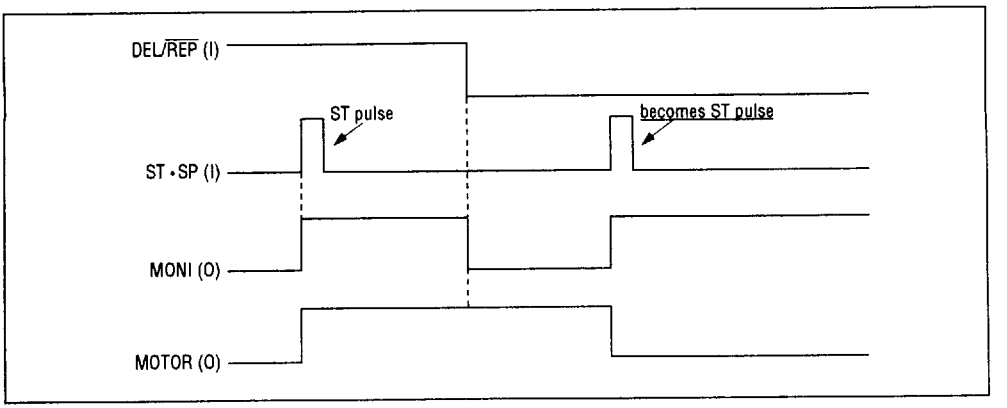
Note 1: If T is 8 sec. or longer, MOTOR rises at the same time when ST pulse is input.
Note 2: If T is 8 sec. or shorter, MOTOR rises 8 seconds after DEL/$\overline{REP}$ is selected.

2. DEL/$\overline{REP}$="L" → "H"
..... from REPEAT mode
to DELAY mode

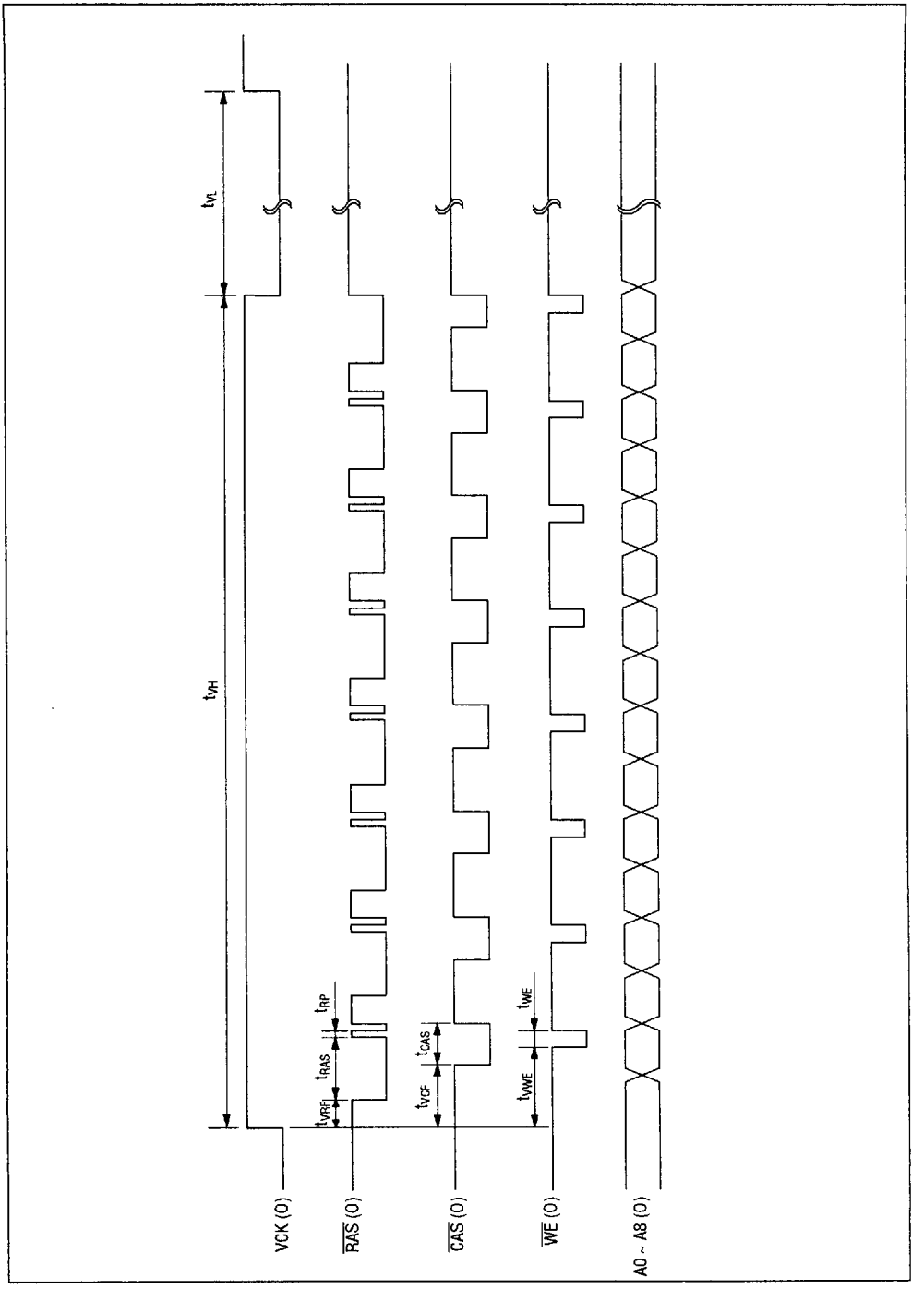
1) Change operation is activated after SP pulse (before ST pulse)



2) Change operation is activated after ST pulse (before SP pulse)



DRAM DRIVING TIMING



MSM6310 performs read/write and CAS before RAS refresh of voice data with the above timing (hidden refresh cycle).

PIN DESCRIPTION

Pin symbol	Pin No.	Function
A_0	40	Address outputs to the DRAM.
A_1	41	
A_2	42	
A_3	43	
A_4	1	
A_5	2	
A_6	3	
A_7	4	
A_8	5	
AIN	20	Analog input terminal. The external line level source, microphone, tape or similar is connected to this pin via adequate signal coupling circuits, that are matched to the pick up.
AMPO	19	The output of the input amplifier, which is usually bonded to FIL 1 I.
FIL1T	18	The direct access input to the internal low-pass filer. In case of external audio amplifier this is the input for the analog source. Usually, FIL 1 I is bonded to AMPO.
FIL1O	15	The output of the internal low-pass filter and at the same time the input of the internal ADC. Usually, this pin is left open.
DO	9	The serial data output to the data input of the external DRAMs.
DI	8	The serial data input from the data output of the external DRAMs.
DAO	12	The output of the internal DAC, which is usually bonded to FIL2I, when the internal filter is used.
FIL2I	14	The input of the internal playback LPF, receiving the signal from DAO.
AOUT	13	This is the terminal that provides the actual output of the regenerated analog waveform. The signal presented has passed the low-pass filter and is buffered.
FSS	26	On this input, the sampling frequency is selectable: H=f_{osc}/512, L=f_{osc}/1024.
RAMS	27	The level to this input informs the chip how many pieces of DRAM devices are externally connected. H=1, L=2.
ST•SP	30	When this chatter-free input receives a H pulse, the LSI starts replaying or stops the reproduction of the recorded analog source. This operation can be cancelled any time with another pulse to ST•SP. The input is internally pulled down. The LSI recognizes which is a START and which is a STOP pulse.
DEL/$\overline{REP}$	29	On this input the playback modes, delayed or repeated, are determined: H-delayed, L=repeated.
AC	33	The "all clear" input. When receiving H level, the internal circuitry is reset. Auto-reset is activated when power is engaged. See application circuit.
XT	31	The crystal connector input. In case of external supply, the source is input here.
$\overline{XT}$	32	The crystal connector output. It is to be left open, when the clock is supplied from external.

PIN DESCRIPTION

Pin symbol	Pin No.	Function
$\overline{WE}$	38	This output provides the write enable signal to the DRAMs in the recording mode.
$\overline{RAS}$	37	The row address strobe signal to the DRAMs.
$\overline{CAS1}$	36	The column address strobe signal to DRAM #1.
$\overline{CAS2}$	35	The column address strobe signal to DRAM #2.
MONI	7	Between the interval of two pulses to ST•SP (start and stop instructions), this output goes to H. When connected to a buffer and a LED, the active state of the LSI can be optically displayed.
MOTOR	6	This signal output can be used to control a tape motor or equivalent equipment controls.
VCK	10	The selected sampling frequency is output here eventual peripheral controlling purposes.
FCUTS	28	On this input the cut-off frequency of the LPF is selectable.
TEST1	25	This is an input used exclusively for factory testing and must be grounded to DGND in applications. The input is internally pulled down.
AVDD	16	The analog supply voltage input, nominally + 5 Volts DC.
DVDD	39	The digital supply voltage input, nominally + 5 Volts DC.
DVDD'	17	This pin must not be drained to feed successive circuits. It can be bonded to DVDD (#39)
AGND	23	Analog ground terminal, nominally 0 Volts.
DGND	24	Digital ground terminal, nominally 0 Volts.
SG	21	Signal ground output providing about VDD/2 level. Connect a capacitor of 47μF across SG and AGND.
SGC	22	Signal ground control input. To stabilize the signal ground, connect a capacitor of > 10μF across SGC and AGND.
NC	11,34,44	These pins must be left open. Do not wire to power sources, ground or signal lines.

FUNCTIONAL DESCRIPTION

LSI operation takes place in basically two modes, one is the DELAY mode, the other the REPEAT mode, selectable on terminal DEL/$\overline{REP}$. The modes cannot be referred to as RECORD and PLAYBACK modes as such, since both recording & playback occurs in the two modes.

The repeat mode denotes that recording of analog data (for the time the memory offers at the selected bit-rate), is repeated again and again until stopped intentionally.

The delay mode denotes that after every recording (for the time the memory offers at the selected bit-rate), the recorded contents is replayed until another recording commences. So, the subsequent recording is "delayed".

THE REPEAT MODE

When applying power or switching over from DELAY to REPEAT, the LSI automatically converts the connected analog input to PCM data and stores it in the external DRAM. When the analog input presence exceeds the available memory, the DRAM is rewritten from the beginning while the old contents are erased, and so on. The output MOTOR issues a H level during recording.

When a H active pulse is applied to ST•SP, the LSI automatically interprets it as a START pulse for the replay of the memory contents. Here, we are talking about the last actual recording, or rather re-recording. The replay of that recording is stopped with another pulse to ST•SP. When ST•SP is not served with a pulse after the memory time has elapsed, the replay is repeated until the pulse is applied. During replay the MOTOR output issues L.

Right after that pulse to ST•SP, the LSI changes the mode from replay back to recordings as described above.

THE DELAY MODE

When applying power or switching over from REPEAT to DELAY, the DRAM changes its read/write mode. The LSI then reads out old data and writes new data, thus the address count up is controlled.

Consequently, the analog data on AIN is recorded and played back immediately after the memory time has elapsed. The reproduced data is available on terminal on terminal AOUT. During this continuous change between recording and playback the output MOTOR issues a H level.

The procedure starts with a H active pulse to ST•SP and MOTOR goes H. The operation is stopped with another pulse to the same pin.. Then MOTOR changes from H to L and AOUT goes to VDD/2 level.

THE SAMPLING FREQUENCY

Nominally, the sampling frequencies are 4 and 8 kHz resulting in a bit rate of 32 kbit/s and 64 kbit/s, respectively. Since the sampling frequencies are submultiples of the clock frequency, other than the nominal values can be adjusted. The LSI is specified for a clock ranging from 4.0 to 8.2 MHz. When the input FSS is L, the divisor is f_{OSC}/512, when H, f_{OSC}/1024. Practically, the available sampling range is from 3.9 kHz to 16 kHz.

RECORDING & PLAYBACK TIMES

The available time is determined by the memory capacity and the sampling frequency selected: memory capacity/bit-rate.

RAMS	FSS = H	FSS = L
L	8.2 sec	16.4 sec
H	4.1 sec	8.2 sec

Where f_s is the sampling frequency and the bit number is 8.

EXTERNAL SOLUTIONS

For maximum application convenience, the MSM6310 provides the user with internal analog circuits to prepare the source signal, amplifier and low-pass filter. However, the internal portions can be by-passed to favor external solutions if desired. This applies to the amplifier or the low-pass filter or both. The internal converters cannot be omitted.

SIGNAL GROUND

For the analog signal processing, the LSI contains a signal ground generation circuit providing a signal ground, SG, at approximately VDD/2. This level is stabilized by two capacitors connected to the inputs SG and SGC (Signal ground control).

NOISE IMMUNITY

It is strictly recommended to make use of the individual power supply inputs and grounds.

Carefully separate analog and digital lines and bond them together at a carefully chosen system point. Avoid the proximity of the LSI to high speed digital systems. Also connect a by-pass capacitor across DVDD and DGND in close proximity to the LSI and other integrated active devices, including memories.

Quantization noise is conditioned by the AD-converter. Through the digitalization of the analog signal, every sampling point is expressed by a value. The limited repertoire of the ADC provides a vertical resolution of 8 bits, i.e., 256 numbers. At quantization intervals, equal to the intervals between two adjacent digital values, inaccuracies result through the limitation of available values...the source of quantization noise. An 8-bit ADC is as accurate as 20mV analog intervals.

In order to minimize the noise, the use of low pass filters is inevitable and OKI has designed-in a filter with optimum characteristics that suited to efficient reduction of the conversion-conditioned noise and to smooth the output waveform.

THE LPF CUT-OFF FREQUENCY & ATTENUATION

Like the sampling frequency, also the cut-off frequency of the internal low-pass filter changes as the oscillation frequency changes.

When the nominal value is selected (4.096 MHz), the filter cuts off as the following table shows:

Sampling Frequency	FCUTS = H	FCUTS = L
4.0kHz	2200Hz	1700Hz
8.0 kHz	3600Hz	2700Hz

The attenuation characteristic of the internal LPF is reflected by the table below:

Band Width Frequency	Attenuation			Unit
	Min.	Typ.	Max.	
300~3400 Hz	−3	–	+3	dB
4000Hz	–	–	−3	dB
7500Hz	–	–	−25	dB

Measured at f_s = 8 kHz, VDD = 4.5~5.5V, Ta = 25°C, FCUTS = "L"

AMPLIFIER CHARACTERISTICS

AMPO maximum DC gain
.....40 dB
AMPO minimum drive impedance
.....200kΩ
AOUT minimum drive impedance
.....50kΩ

APPLICATION CIRCUIT