

Quad D-Type Register (3-State)

The TC74HC173A is a high speed CMOS D-TYPE REGISTER fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains a 4-bit register consisting of D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common clear input (CLEAR).

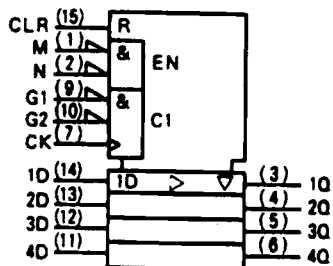
Signals applied to the data inputs (D1 ~ D4) are stored in the respective flip-flops on the positive going transition of CLOCK when clock control inputs (G1, G2) are held low.

The clear function is asynchronous to CLOCK and active on a high level. The stored data are enabled to each outputs when output control inputs (M, N) are held low, else the outputs are high impedance state.

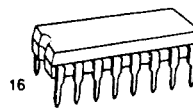
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features:

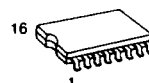
- High Speed: $t_{pd} = 47\text{MHz(Typ.)}$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%V_{CC}(\text{Min.})$
- Output Drive Capability: 15 LSTTL Loads
- Symmetrical Output Impedance: $I_{OH} = I_{OL} = 6\text{mA}(\text{Min.})$
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range: $V_{CC}(\text{opr}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS173



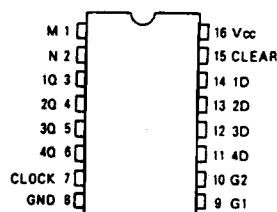
IEC Logic Symbol



P



F



(TOP VIEW)

Pin Assignment

Truth Table

CLEAR	CLOCK	Data Enable		Dn	Output Control		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L		X	X	X	L	L	Q0
L		H	X	X	L	L	Q0
L		X	H	X	L	L	Q0
L		L	L	H	L	L	H
L		L	L	L	L	L	L

X: Don't Care

Z: High Impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 - 6	V
Input Voltage	V_{IN}	0 - V_{CC}	V
Output Voltage	V_{OUT}	0 - V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000($V_{CC} = 2.0\text{V}$) 0 ~ 500($V_{CC} = 4.5\text{V}$) 0 ~ 400($V_{CC} = 6.0\text{V}$)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition	$T_a = 25^\circ\text{C}$				$T_a = -40 \sim 85^\circ\text{C}$		Unit	
			V_{CC}	Min.	Typ.	Max.	Min.	Max.		
High-Level Input Voltage	V_{IH}	-	2.0	1.5	-	-	1.5	-	V	
			4.5	3.15	-	-	3.15	-		
			6.0	4.2	-	-	4.2	-		
Low-Level Input Voltage	V_{IL}	-	2.0	-	-	0.5	-	0.5	V	
			4.5	-	-	1.35	-	1.35		
			6.0	-	-	1.8	-	1.8		
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
			$I_{OH} = -6\text{mA}$ $I_{OH} = -7.8\text{mA}$	4.5	4.18	4.31	-	4.13	-	
				6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
			$I_{OL} = 6\text{mA}$ $I_{OL} = 7.8\text{mA}$	4.5	-	0.17	0.26	-	0.33	
				6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	-	-	±0.5	-	±5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	±0.1	-	±1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	4.0	-	40.0		

Timing Requirements (Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C	Unit
			V _{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	-	2.0	-	75	95	ns
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$	-	2.0	-	75	95	
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Setup Time (G1, G2)	t_s	-	2.0	-	100	125	
			4.5	-	20	25	
			6.0	-	17	21	
Minimum Setup Time (D)	t_s	-	2.0	-	75	95	
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Hold Time (G1, G2, D)	t_h	-	2.0	-	0	0	
			4.5	-	0	0	
			6.0	-	0	0	
Minimum Removal Time (CLEAR)	t_{rem}	-	2.0	-	5	5	
			4.5	-	5	5	
			6.0	-	5	5	
Clock Frequency	f	-	2.0	-	9	7	MHz
			4.5	-	43	34	
			6.0	-	51	40	

AC Electrical Characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

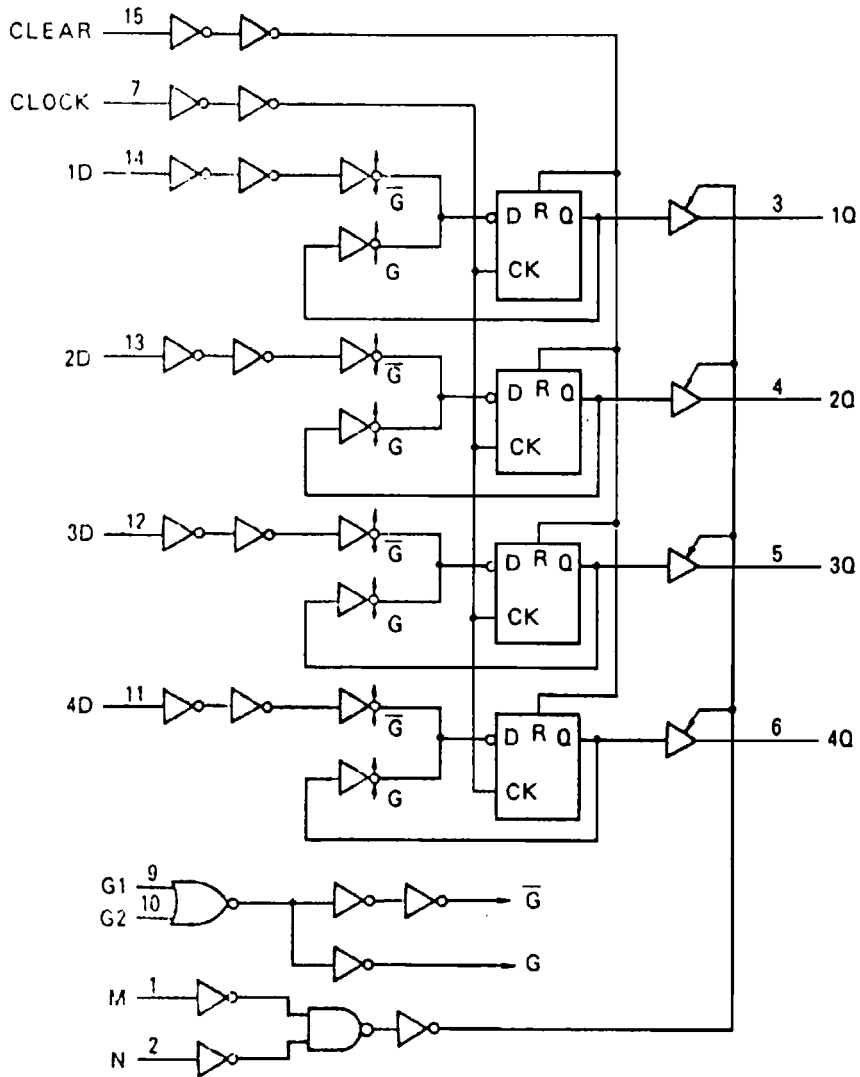
Parameter	Symbol	Test Condition				Ta = 25°C			Ta = -40 ~ 85°C		Unit
			CL	V _{CC}	Min.	Typ.	Max.	Min.	Max.		
Output Transition Time	t _{TLH} t _{THL}	-	50	2.0	-	20	60	-	75	ns	
				4.5	-	6	12	-	15		
				6.0	-	5	10	-	13		
Propagation Delay Time (CLOCK-Q)	t _{PLH} t _{PHL}	-	50	2.0	-	50	115	-	145	ns	
				4.5	-	15	23	-	29		
				6.0	-	12	20	-	25		
			150	2.0	-	65	155	-	195		
				4.5	-	20	31	-	39		
				6.0	-	16	26	-	33		
Propagation Delay Time (CLEAR-Q)	t _p t _{pHL}	-	50	2.0	-	50	115	-	145	ns	
				4.5	-	15	23	-	29		
				6.0	-	12	20	-	25		
			150	2.0	-	63	155	-	195		
				4.5	-	20	31	-	39		
				6.0	-	16	26	-	33		
Output Enable time	t _{pZL} t _{pZH}	R _L = 1kΩ	50	2.0	-	50	115	-	145	ns	
				4.5	-	15	31	-	29		
				6.0	-	12	26	-	25		
			150	2.0	-	63	115	-	195		
				4.5	-	20	23	-	39		
				6.0	-	16	20	-	33		
Output Disable time	t _{pLZ} t _{pHZ}	R _L = 1kΩ	50	2.0	-	36	135	-	170	ns	
				4.5	-	17	27	-	34		
				6.0	-	15	23	-	29		
Maximum Clock Frequency	f _{MAX}	-	50	2.0	9	20	-	7	-	MHz	
				4.5	43	67	-	34	-		
				6.0	51	84	-	40	-		
Input Capacitance	C _{IN}	-	-	-	-	5	10	-	10	pF	
Output Capacitance	C _{OUT}	-	-	-	-	10	-	-	-		
Power Dissipation Capacitance	C _{PD(1)}	-	-	-	-	45	-	-	-		

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation:

$$C_{PD(tot)} = 28 + 17 \cdot n$$



Logic Diagram

Notes