Signetics

FAST 74F194
Shift Register

FAST Products

4-Bit Bidirectional Universal Shift Register
Product Specification

FEATURES

- **Shift right and shift left capability**
- **Synchronous parallel and serial data transfer**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F194N
16-Pin Plastic SO	N74F194D

DESCRIPTION

The functional characteristics of the 74F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

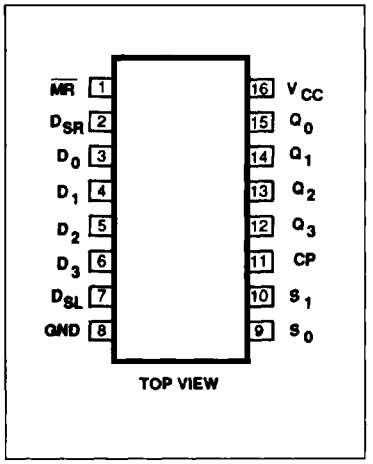
The 'F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select-Function Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. Mode Select and data inputs on the 'F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Select and selected data inputs must be stable one setup time prior to the Low-to-High transition of the clock pulse. Signals on the the Mode Select, Parallel Data (D_0 -D_3) and Serial Data (D_{SR}, D_{SL}) can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed. The four Parallel Data inputs (D_0 -D_3) are D-type inputs. Data appearing on (D_0 -D_3) inputs when S_0 and S_1 are High is transferred to the Q_0 -Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

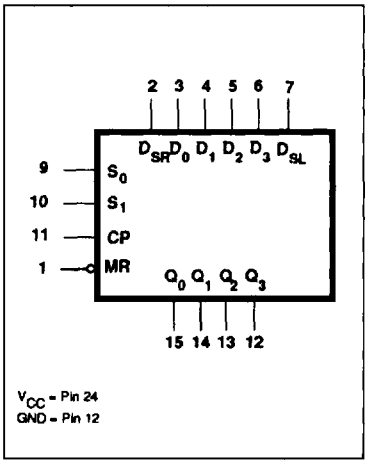
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

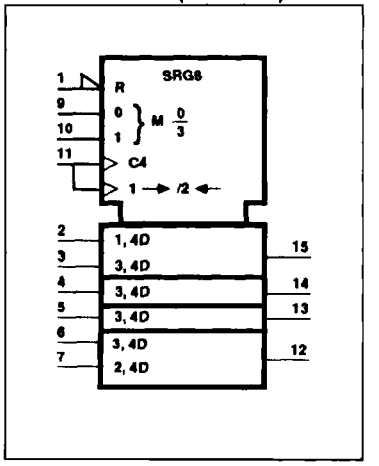
PIN CONFIGURATION



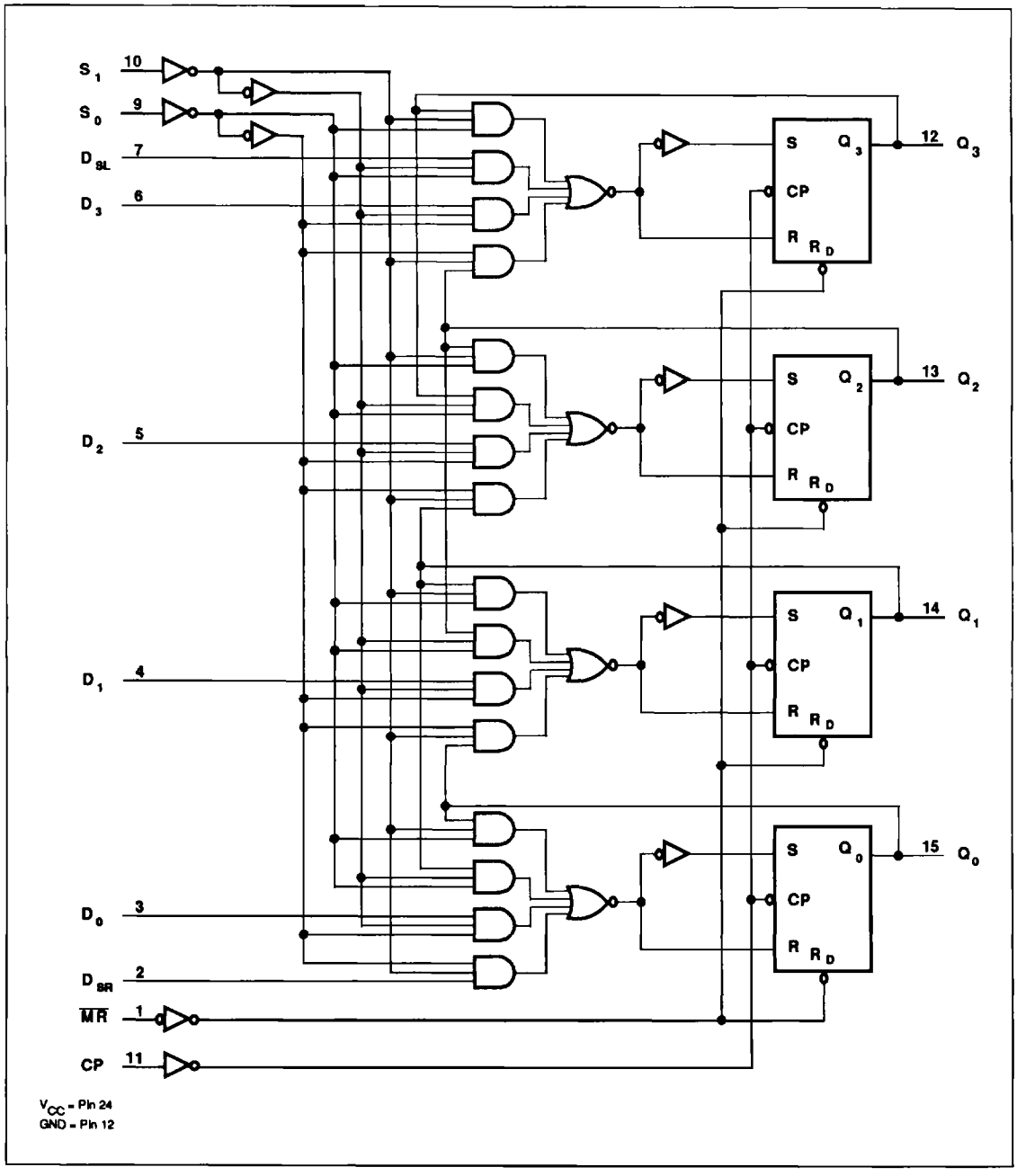
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODES
CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3	
X	L	X	X	X	X	X	L	L	L	L	Reset (clear)
X	H	l	l	X	X	X	q_0	q_1	q_2	q_3	Hold (do nothing)
↑	H	h	l	X	l	X	q_1	q_2	q_3	L	Shift left
↑	H	h	l	X	h	X	q_1	q_2	q_3	H	
↑	H	l	h	l	X	X	L	q_0	q_1	q_2	Shift right
↑	H	l	h	h	X	X	H	q_0	q_1	q_2	
↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3	Parallel load

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[4]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = MAX			33	46	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output High state will change to Low state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
5. With all outputs open, D_i inputs grounded and a 4.5V applied to S_0, S_1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

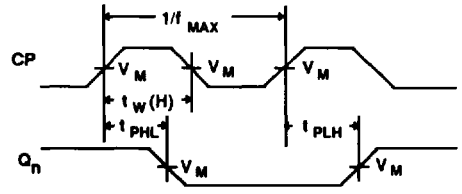
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	8.6	12.0	4.5	14.0	ns

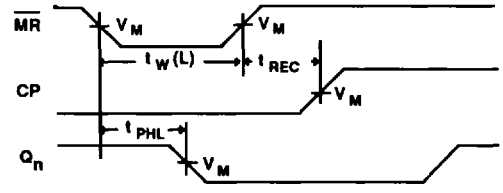
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n, D_{SL}, D_{SR} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_{SL}, D_{SR} to CP	Waveform 3	0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	5.0			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns

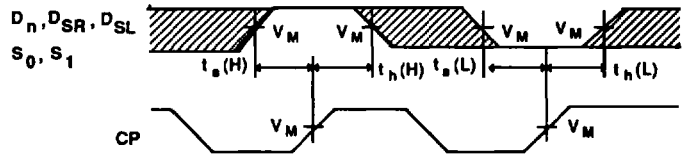
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



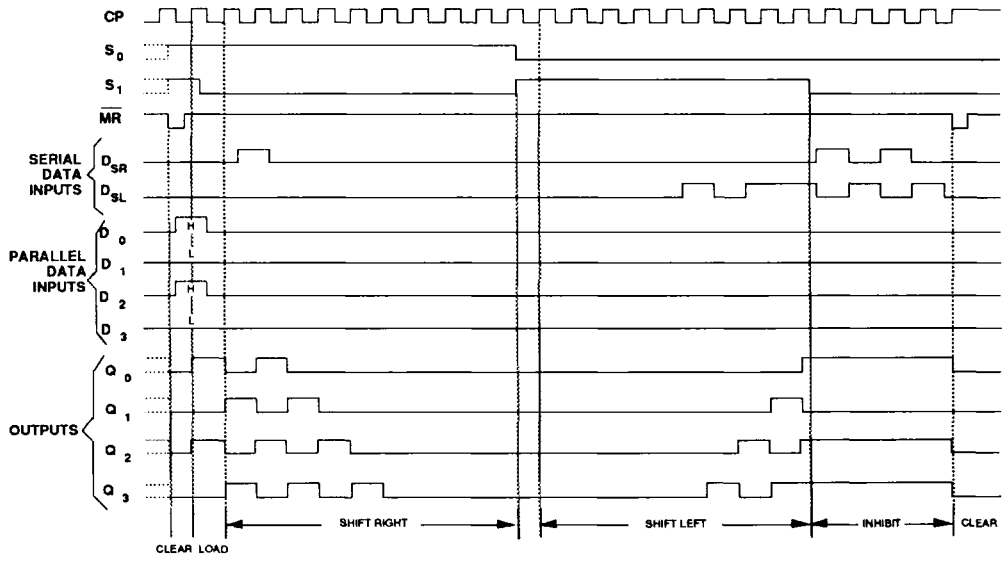
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



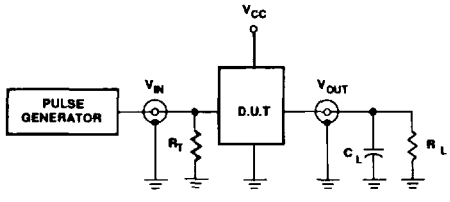
Waveform 3. Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TIMING DIAGRAM (Typical Clear, Load, Shift-Right, Shift-Left and Inhibit Sequence)



TEST CIRCUIT AND WAVEFORMS



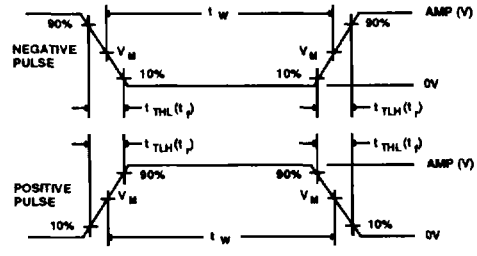
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns