

SANYO

No. ※ 4712

LC331664M, ML-70/80/10**1 MEG (65536 words × 16 bits) Pseudo-SRAM****Preliminary****Overview**

The LC331664 series is composed of pseudo static RAM that operate on a single 5 V power supply and are organized as 65536 words × 16 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. The LC331664 series can easily accomplish auto-refresh by means of $\overline{LOE}/\overline{RFSH}$ input. The available package is the 40-pin SOP with a width of 525 mil.

Features

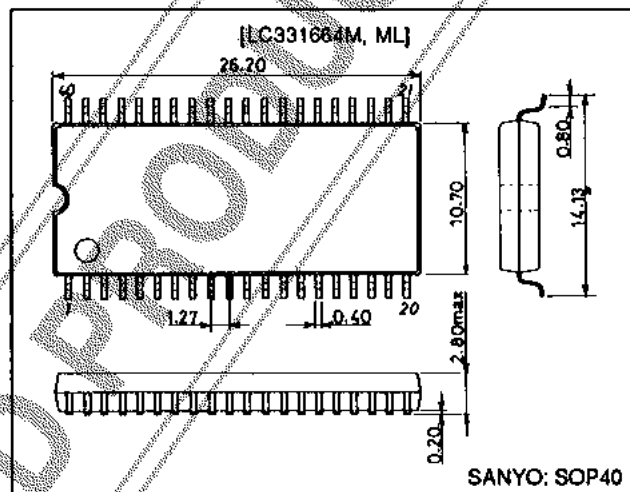
- 65536 words × 16 bits configuration
- $\overline{CE}$ access time, $\overline{OE}$ access time, cycle time, operating supply current and standby current 2

Parameter	LC331664M/ML		
	-70	-80	-10
$\overline{CE}$ access time	70 ns	80 ns	100 ns
$\overline{OE}$ access time	35 ns	40 ns	50 ns
Cycle time	115 ns	130 ns	160 ns
Operating supply current	100 mA	90 mA	75 mA
Standby current 2	2 mA/100 μ A (L version)		

- Single 5 V $\pm$ 10% power supply
- All input and output (I/O) TTL compatible
- Fast access time and low power dissipation
- 4 ms refresh using 256 refresh cycles
- Supports $\overline{CE}$ -only refresh and auto-refresh
- Supports byte-unit read and write operations using the $\overline{LOE}/\overline{RFSH}$ and $\overline{UOE}$ inputs or the $\overline{LWE}$ and $\overline{UWE}$ inputs.
- Low-power version: 100 μ A standby current 2 (I_{CCS2}).
- 40-pin SOP plastic package

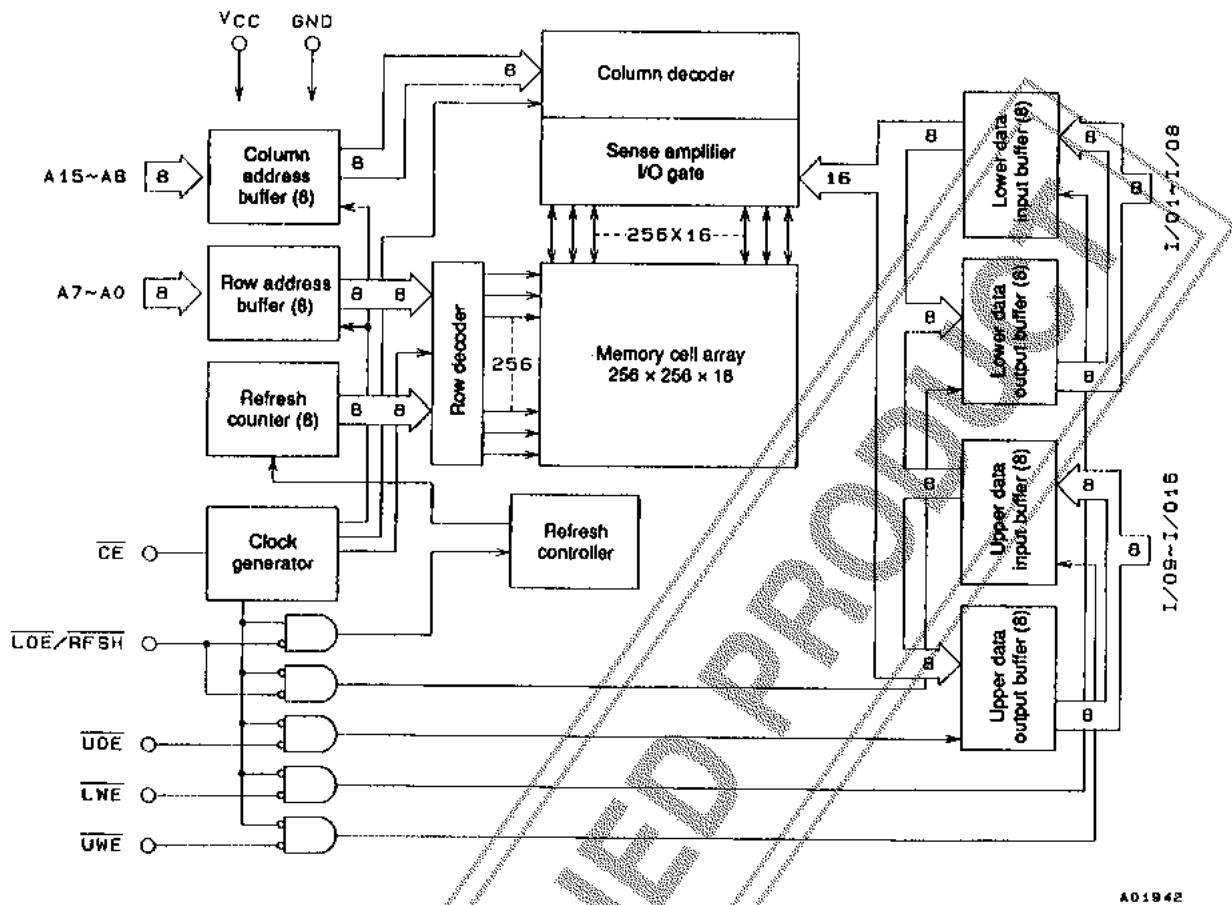
Package Dimensions

unit: mm

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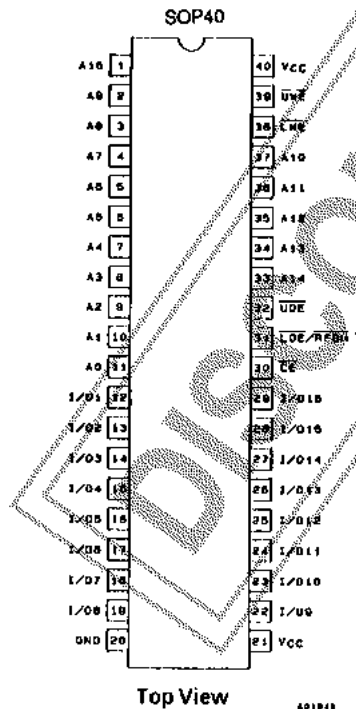
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Block Diagram



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Pin Assignment



Pin Functions

A0 to A15	Address input
LWE	Lower byte write enable Input
UWE	Upper byte write enable Input
LOE/RFSH	Lower byte output enable input/refresh input
UOE	Upper byte output enable Input
CE	Chip enable Input
I/O1 to I/O8	Lower byte data input/output
I/O9 to I/O16	Upper byte data input/output
Vcc	Power supply
GND	Ground

Function Logic

CE	LOE/RFSH	UOE	LWE	UWE	A0 to 7	A8 to 15	I/O1 to 8	I/O9 to 16	State
H	H	X	X	X	X	X	HZ	HZ	Standby
L	L	L	H	H	VX	VX	OUT	OUT	Read (word)
L	L	H	H	H	VX	VX	OUT	HZ	Read (lower byte)
L	H	L	H	H	VX	VX	HZ	OUT	Read (upper byte)
L	H	H	L	L	VX	VX	IN	IN	Write (word)
L	H	H	L	H	VX	VX	IN	HZ	Write (lower byte)
L	H	H	H	L	VX	VX	HZ	IN	Write (upper byte)
L	H	H	H	H	VX	X	HZ	HZ	CE-only refresh
H	NP	X	X	X	X	X	HZ	HZ	Auto-refresh

H: High-level input of $V_{IN} = 6.5 \text{ V}$ to V_{IH} (min)L: Low-level input of $V_{IN} = V_{IL}$ (max) to -1.0 V

X: High- or low-level input

VX: "IN" when CE = L is confirmed, then "X."

NP: Negative-polarity pulse input

HZ: High impedance

IN: Input state

OUT: Output state

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	$V_{CC \text{ max}}$	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Allowable power dissipation	$P_{D \text{ max}}$	600	mW	1
Output short current	I_{OUT}	50	mA	1
Operating temperature range	T_{opr}	0 to +70	°C	1
Storage temperature range	T_{stg}	-55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_A = 0$ to $+70^\circ\text{C}$

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	-1.0		+0.8	V	2

Note: 2. All voltages are referenced to GND.

DC Electrical Characteristics at $T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Conditions	min	max	Unit	Note
Operating current (average current during operation)	I_{CCA}	Cycle time 115 ns 130 ns 180 ns		100 90 75	mA	3, 4
Standby current 1	I_{CCS1}	$CE = LOE/RFSH = V_{IH}$ LC331664M LC331664ML		3 1	mA	
Standby current 2	I_{CCS2}	$CE = LOE/RFSH = V_{CC} - 0.2\text{ V}$ LC331664M LC331664ML		2 100	mA μA	
Input leakage current	I_{IL}	$0\text{ V} \leq V_{IN} \leq V_{CC}$, pins other than measuring pin = 0 V	-10	+10	μA	
Output leakage current	I_{OL}	Output disable, $0\text{ V} \leq V_{OUT} \leq V_{CC}$	-10	+10	μA	
Output high level voltage	V_{OH}	$I_{OUT} = -1\text{ mA}$	2.4		V	
Output low level voltage	V_{OL}	$I_{OUT} = 4.2\text{ mA}$		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller. A bypass capacitor of 0.01 μF or larger should be inserted between V_{CC} and GND for memory chip to suppress power supply noise (voltage drops) due to transient currents.

4. Dependent on output load. Maximum value is value during free state.

Capacitance Characteristics at $V_{CC} = 5\text{ V} \pm 10\%$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$

Parameter	Symbol	Measuring conditions	min	max	Unit
Input capacitance (A0 to 15)	C_{IN1}	$V_{IN1} = 0\text{ V}$		5	pF
Input capacitance (CE, LOE/RFSH, UOE, LWE, UWE)	C_{IN2}	$V_{IN2} = 0\text{ V}$		7	pF
I/O capacitance	C_{IO}	$V_{IO} = 0\text{ V}$		10	pF

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

AC Electrical Characteristics at $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$ (Notes 5, 6, 7, 8, 9, 14.)

Parameter	Symbol	70 ns		80 ns		100 ns		Unit	Note
		min	max	min	max	min	max		
Random read or write cycle time	t_{RC}	115		130		160		ns	
Read-modify-write cycle time	t_{RMW}	165		195		235		ns	
CE pulse width	t_{CE}	70	10000	80	10000	100	10000	ns	
CE precharge time	t_p	35		40		50		ns	
CE access time	t_{CEA}		70		80		100	ns	
LOE, UOE access time	t_{OEA}		35		40		50	ns	
CE output enable time	t_{CLZ}	10		10		10		ns	
LOE, UOE output enable time	t_{OLZ}	0		0		0		ns	
CE output disable time	t_{CHZ}	0	20	0	25	0	30	ns	10
LOE, UOE output disable time	t_{OHZ}	0	20	0	25	0	30	ns	10
LWE, UWE output disable time	t_{WHZ}	0	20	0	25	0	30	ns	10
LOE, UOE hold time for CE	t_{OHC}	0		0		0		ns	
LOE, UOE setup time for CE	t_{OSC}	10		10		10		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
Write pulse width	t_{WP}	25		30		35		ns	
Write command hold time	t_{WCH}	55		60		65		ns	
Write command lead time	t_{CWL}	40		45		50		ns	

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Parameter	Symbol	70 ns		80 ns		100 ns		Unit	Note
		min	max	min	max	min	max		
Input data setup time for $\overline{\text{LWE}}$, $\overline{\text{UWE}}$	t_{DSW}	25		30		35		ns	11
Input data setup time for $\overline{\text{CE}}$	t_{DSC}	25		30		35		ns	11
Input data hold time for $\overline{\text{LWE}}$, $\overline{\text{UWE}}$	t_{DHW}	0		0		0		ns	11
Input data hold time for $\overline{\text{CE}}$	t_{DHC}	0		0		0		ns	11
Address setup time for $\overline{\text{CE}}$	t_{ASC}	0		0		0		ns	12
Address hold time for $\overline{\text{CE}}$	t_{AHC}	15		20		25		ns	12
Auto-refresh cycle time	t_{FC}	115		130		160		ns	
RFSH delay time for $\overline{\text{CE}}$	t_{RFD}	35		40		50		ns	
RFSH pulse width (auto-refresh)	t_{FAP}	75	8000	80	8000	80	8000	ns	13
RFSH precharge time (auto-refresh)	t_{FP}	30		30		30		ns	13
RFSH active $\overline{\text{CE}}$ delay time (auto-refresh)	t_{FCE}	135		160		190		ns	13
Refresh time (256 cycles, A0 to A7)	t_{REF}		4		4		4	ms	
Rise or fall time	t_T	3	50	3	50	3	50	ns	

Note: 5. To accomplish internal initialization, $\overline{\text{CE}}$ is fixed at V_{IH} for an interval of 1 ms when V_{CC} reaches the specified voltage after power is switch on. At least eight cycles must be executed following the period.

6. Measured at $t_T = 5$ ns.

7. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are reference levels.

8. Measured using an equivalent of 100 pF and two standard TTL loads.

9. $\overline{\text{LOE}}$ /RFSH input functions as lower byte output enable input ($\overline{\text{LOE}}$) when $\overline{\text{CE}} = V_{IL}$ and as refresh input (RFSH) when $\overline{\text{CE}} = V_{IH}$.

10. t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.

11. As with ordinary static RAM, write data is incorporated at the rise of $\overline{\text{LWE}}$, $\overline{\text{UWE}}$ input or $\overline{\text{CE}}$ input, whichever is earlier, and write data is therefore held during t_{DSW} , t_{DSC} , t_{DHW} or t_{DHC} .

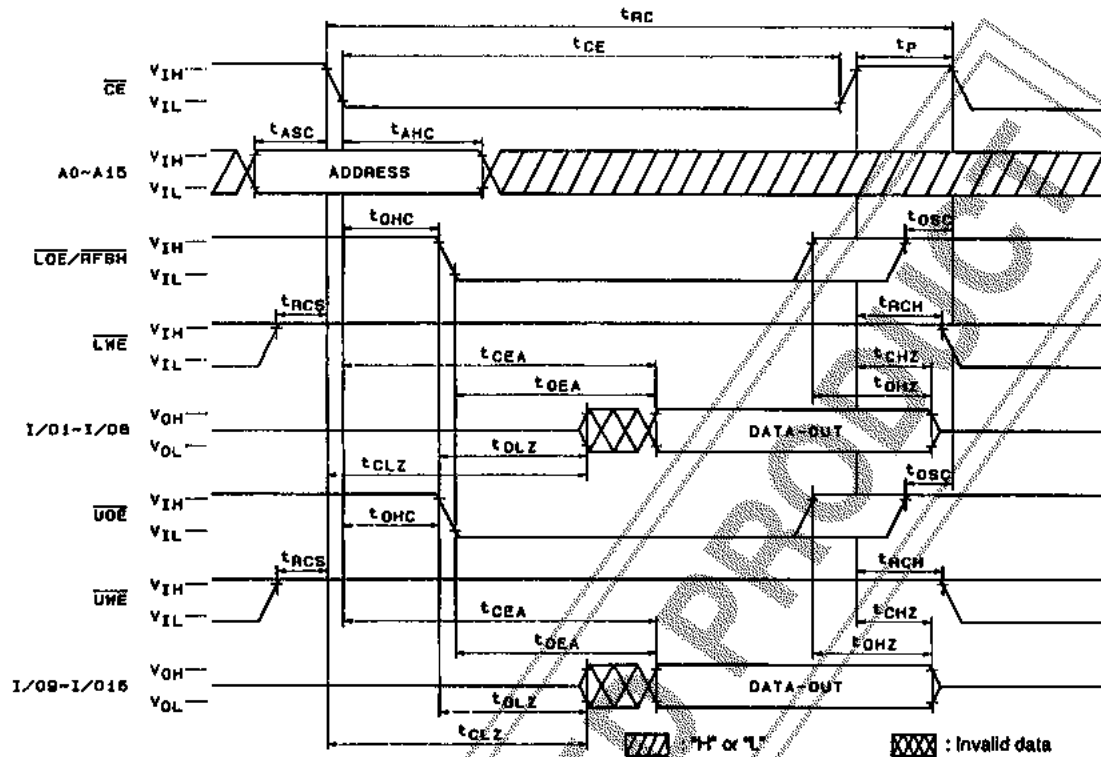
12. Because address input is incorporated at the fall of $\overline{\text{CE}}$, the address is maintained during t_{ASC} or t_{AHC} .

13. After auto-refresh has completed, $\overline{\text{CE}}$ must not be made active until the t_{FCE} period has elapsed.

14. The output timing measurement reference level is $V_{OH} = 2.0$ V or $V_{OL} = 0.8$ V.

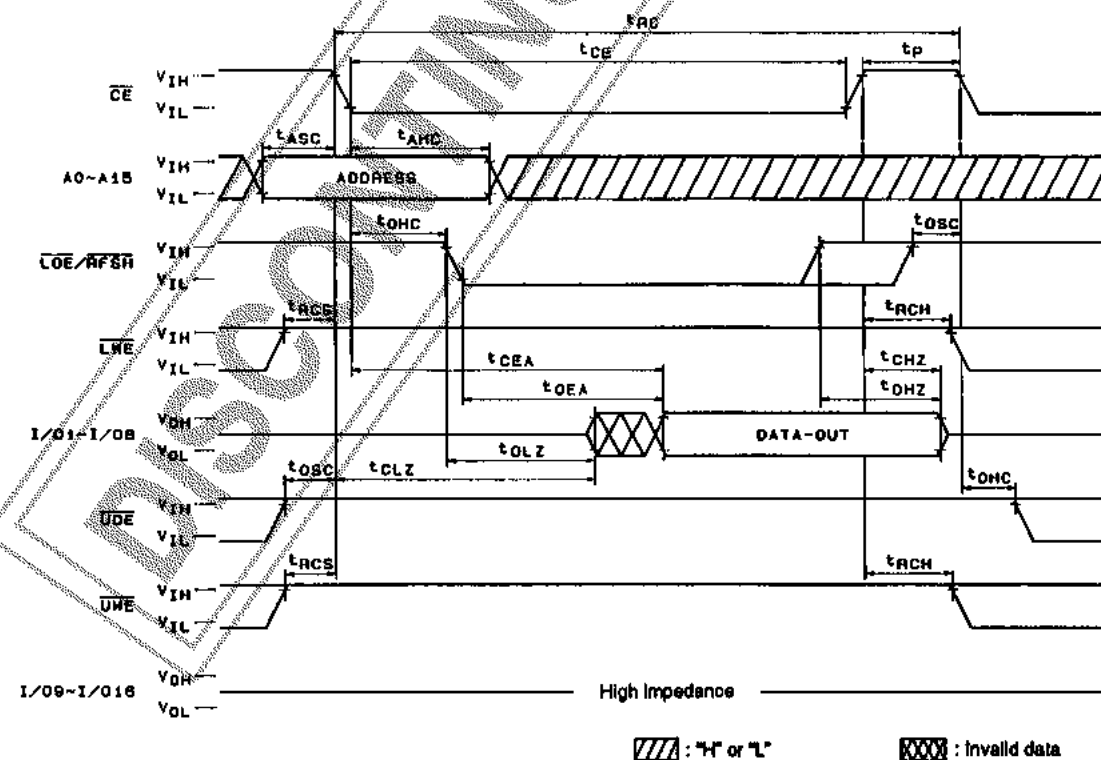
Timing Chart

Read Cycle (word)



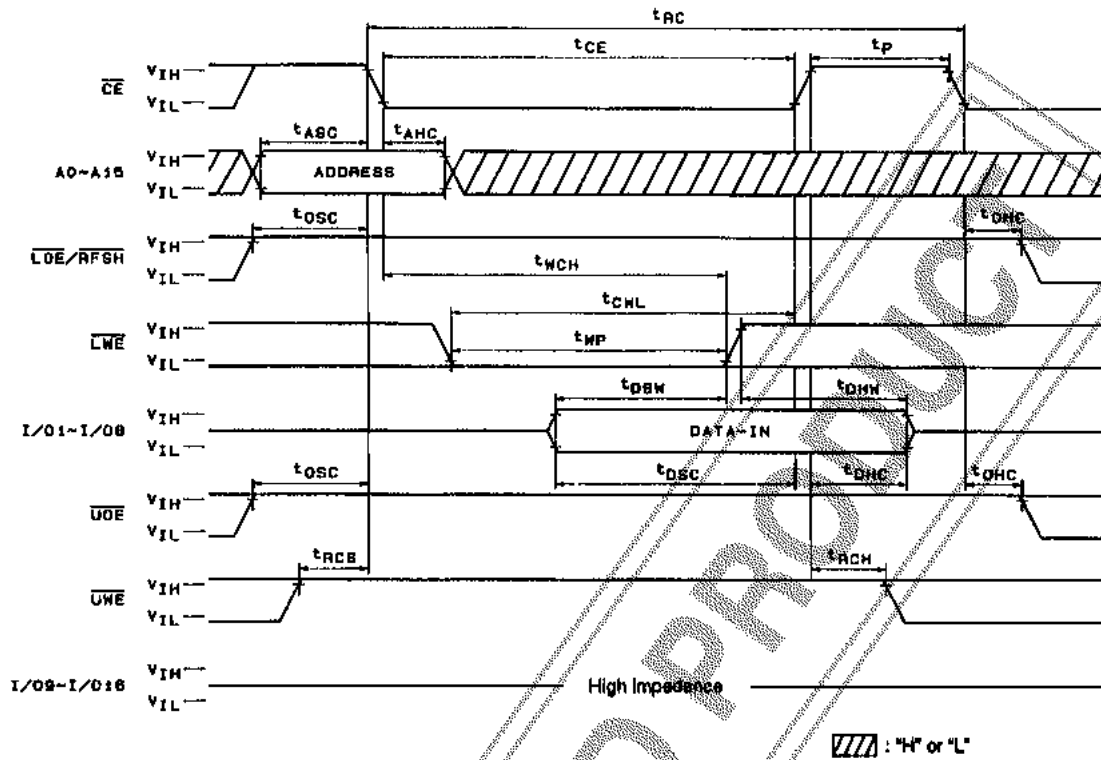
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Read Cycle (lower byte)



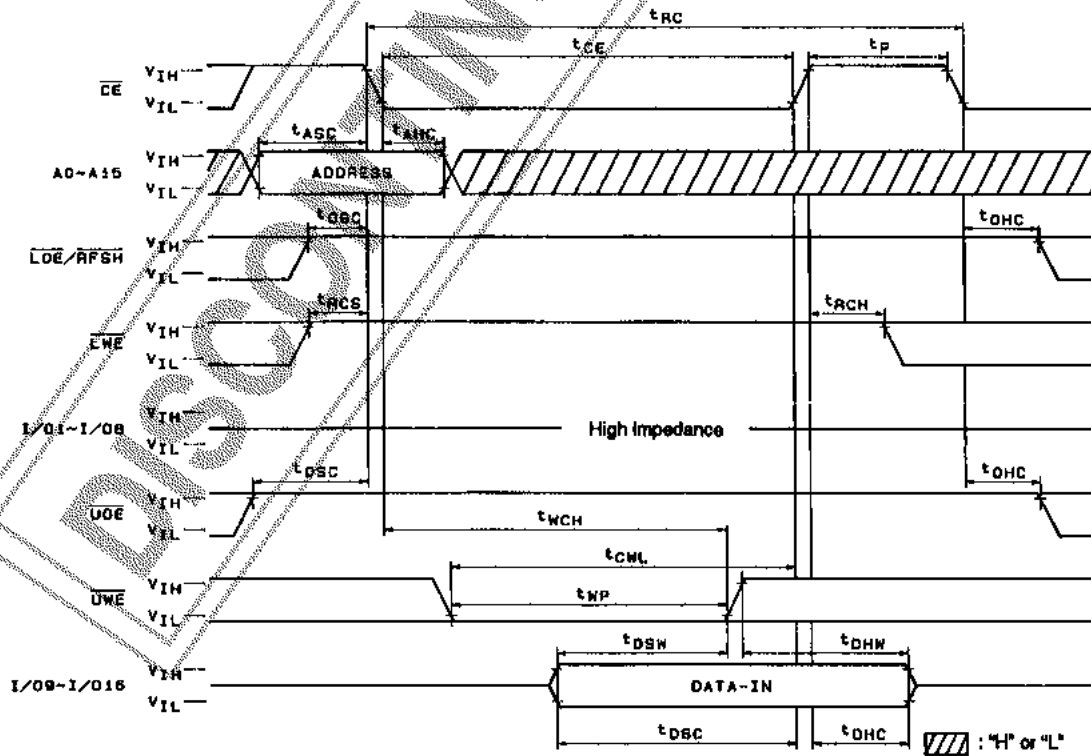
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Write Cycle (lower byte)



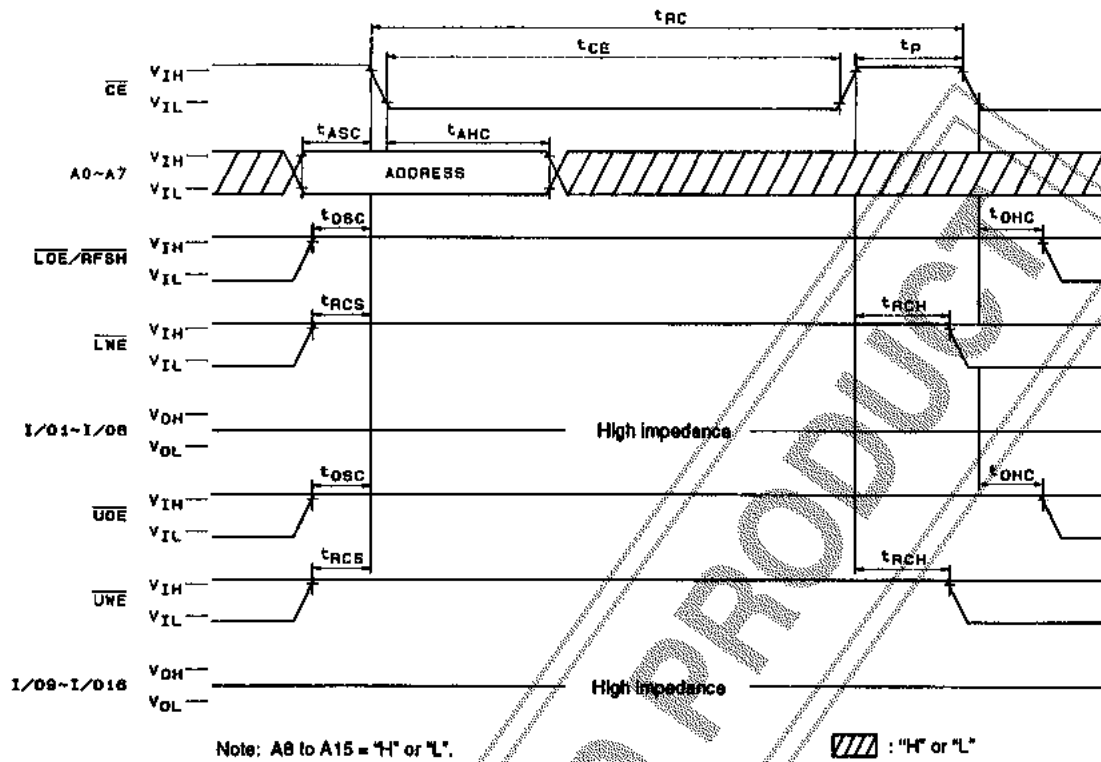
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Write Cycle (upper byte)



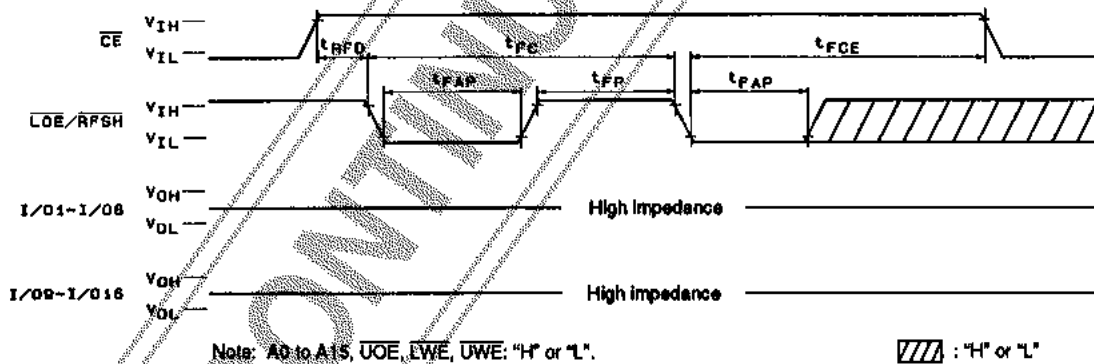
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CE-Only Refresh Cycle



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Auto-Refresh Cycle



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