S19FL128P MirrorBit® ROM

128-Megabit CMOS 3.0 Volt MirrorBit ROM with 104-MHz SPI (Serial Peripheral Interface) Bus

Data Sheet

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Publication Number S19FL128P_00 **Revision** 03 **Issue Date** June 13, 2008

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S19FL128P MirrorBit® ROM

128 Megabit CMOS 3.0 Volt MirrorBit ROM with 104 MHz SPI (Serial Peripheral Interface) Bus

Data Sheet

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6 V read operations
- **Device ID**
  - RDID (9Fh), READ_ID (90h) and RES (ABh) commands to read manufacturer and device ID information
  - RES command one-byte electronic signature for backward compatibility
- **Process Technology**
  - Manufactured on 0.09 µm MirrorBit® process technology
- **Package Option**
  - Industry Standard Pinouts
  - 16-pin SO package (300 mils)
  - 8-Contact WSON Package (6 x 8 mm)

Performance Characteristics

- **Speed**
  - 104 MHz clock rate (maximum)
- **Power Saving Standby Mode**
  - Standby Mode 200 µA (max)
  - Deep Power Down Mode 3 µA (typical)

Software Features

- SPI Bus Compatible Serial Interface

Hardware Features

- **x8 Parallel Mode (for 16-pin SO package only)**

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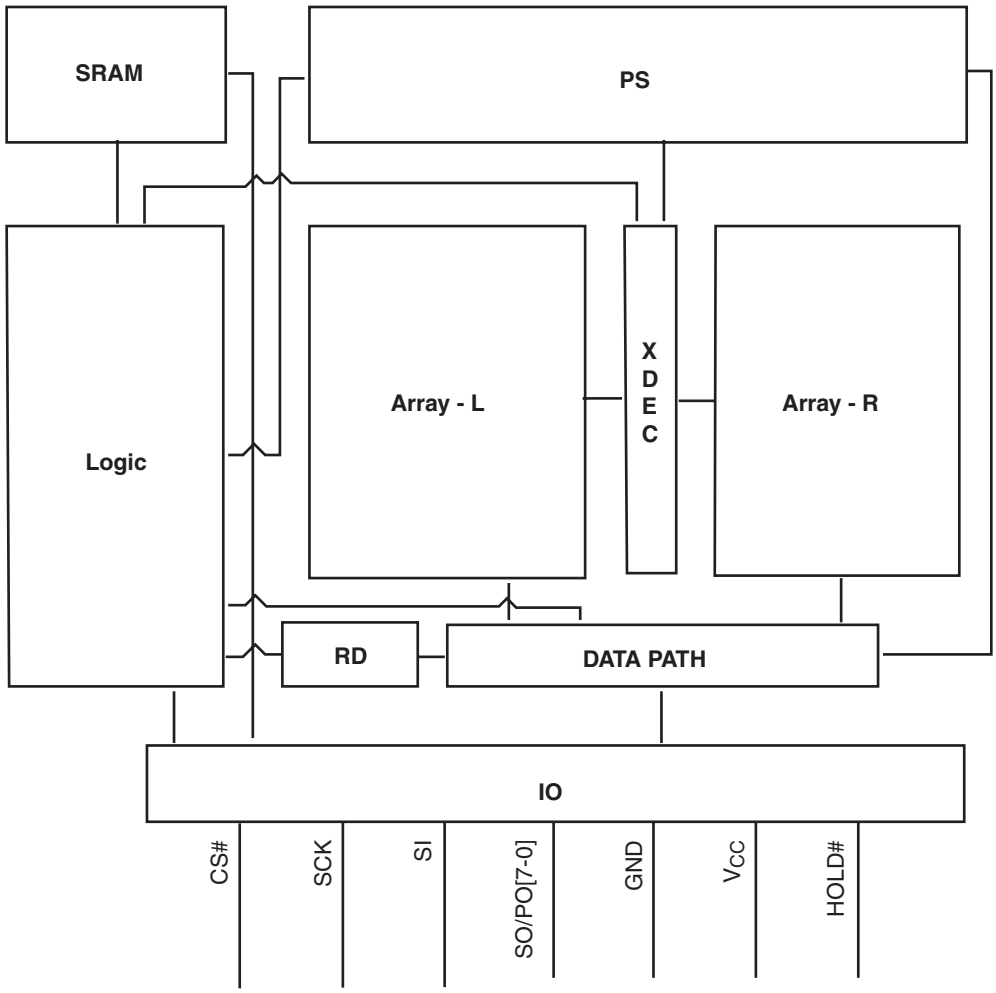


2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)

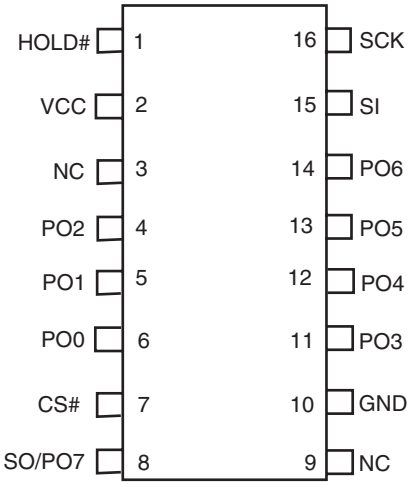
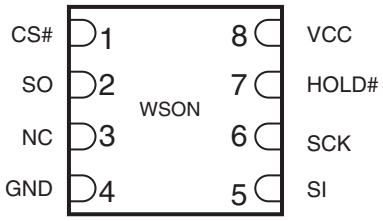


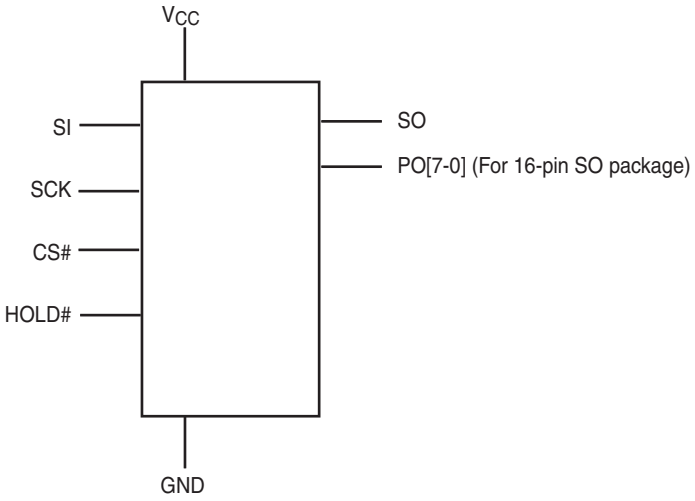
Figure 2.2 8-Pin WSON Package (6 x 8 mm)



3. Input/Output Descriptions

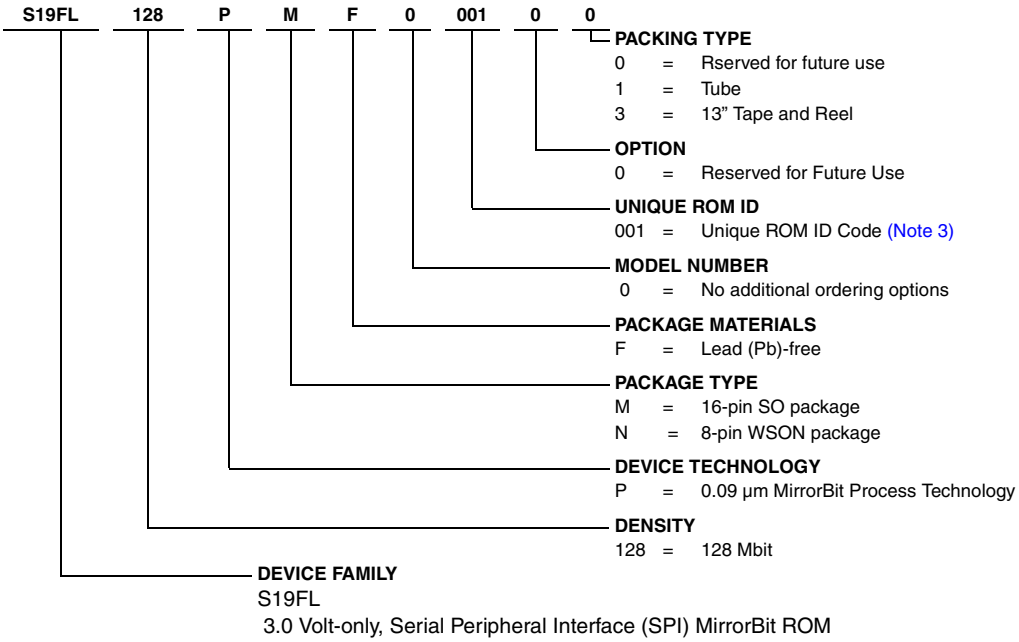
Signal Name	I/O	Description
SO (Signal Data Output)	Output	Transfers data serially out of the device on the falling edge of SCK.
PO[7–0] (Parallel Data Input/Output)	Input/Output	Transfers parallel data into the device on the rising edge of SCK or out of the device on the falling edge of SCK.
SI (Serial Data Input)	Input	Transfers data serially into the device. Device latches commands, and addresses, data on SI on the rising edge of SCK.
SCK (Serial Clock)	Input	Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS# (Chip Select)	Input	Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written.
HOLD# (Hold)	Input	Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low.
V_{CC}	Input	Supply Voltage
GND	Input	Ground

4. Logic Symbol



5. Ordering Information

The ordering part number is formed by a valid combination of the following:



Valid Combinations

Table 5.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 5.1 S19FL128P Valid Combinations Table

S19FL128P Valid Combinations						
Base Ordering Part Number	**Package & Material**	**Model Number**	**Unique ROM ID**	**Option**	**Packing Type**	**Marking Spec**
S19FL128P	MF, NF (Note 2)	0	XXX	0	1, 3	(FL128P) + (Unique ROM ID)

Notes

1. *All S19FL-A devices are offered over the industrial temperature (-40°C to 85°C) range .*
2. *Contact your local sales office for availability.*
3. *Unique ROM ID is assigned by the factory.*

6. Spansion SPI Modes

A microcontroller can use either of its two SPI modes to control Spansion SPI Flash memory devices:

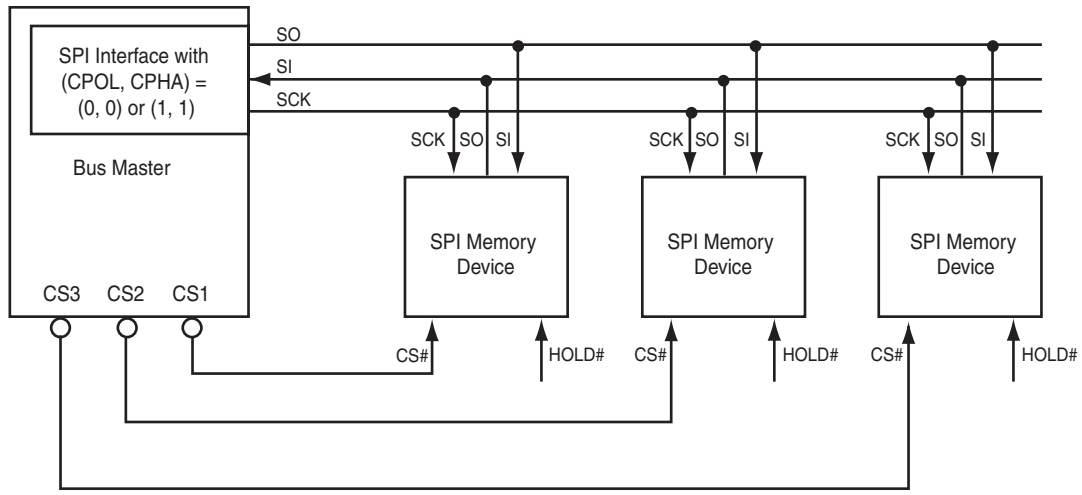
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in Figure 6.2 for each of the two modes:

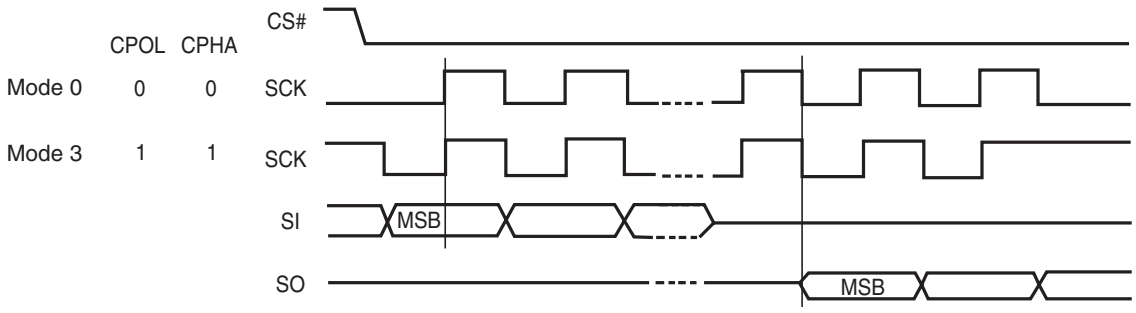
- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note
The Hold (HOLD#) signal should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Spansion SPI devices (S19FL-P) accept and output data in bytes (8 bits at a time).

7.1 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device.

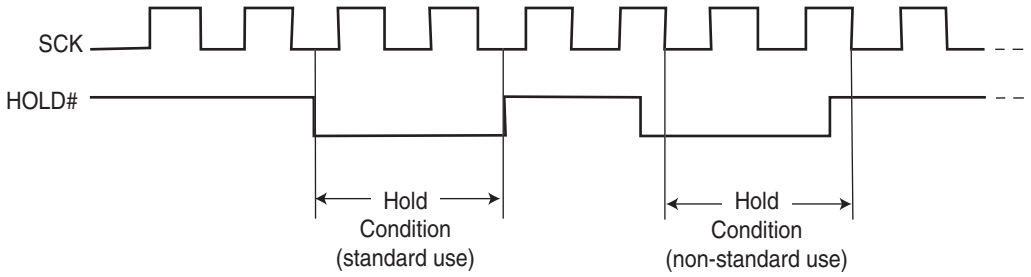
The Hold mode starts on the falling edge of HOLD# if SCK is also low (see Figure 7.1, standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See Figure 7.1.

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

Figure 7.1 Hold Mode Operation



8. Parallel Mode (for 16-pin SO package only)

The parallel mode provides 8 bits of input/output. Entering Parallel mode requires issuing the Enter Parallel Mode command (55h). After writing the Parallel Mode Entry command and pulling CS# high, the available commands are Read, Release from Deep Power Down/Release from Deep Power Down and Read Electronic Signature (RES), Deep Power Down (DP), Read Identification (RDID) and Read ID (READ_ID).

The flash memory will remain in Parallel mode until either the Parallel Mode Exit command (45h) is issued, or until a power-down / power-up sequence has been completed, after which the flash memory will exit parallel mode automatically and switch back to serial mode (no power-down will be necessary to switch back to serial mode if the Parallel Mode Exit command is issued).

In parallel mode, the maximum SCK clock frequency is limited to 6 MHz for Read Data Bytes and 10 MHz for other operations. PO[6-0] can be left unconnected if the Parallel Mode functions are not needed.

Fast Read command (0Bh) is not applicable in Parallel Mode.

9. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. Table 9.3 on page 23 lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST_READ) and Read Identification (RDID) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

9.1 Read Data Bytes (READ: 03h)

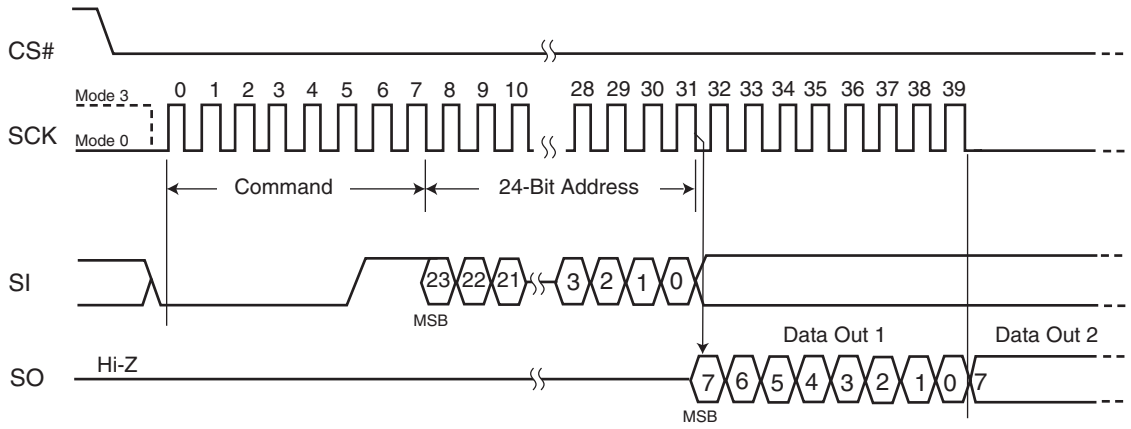
9.1.1 Serial Mode

The Read Data Bytes (READ-Serial Mode) command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 40 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3-byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

Figure 9.1 and Table 9.3 on page 23 detail the READ command sequence. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output.

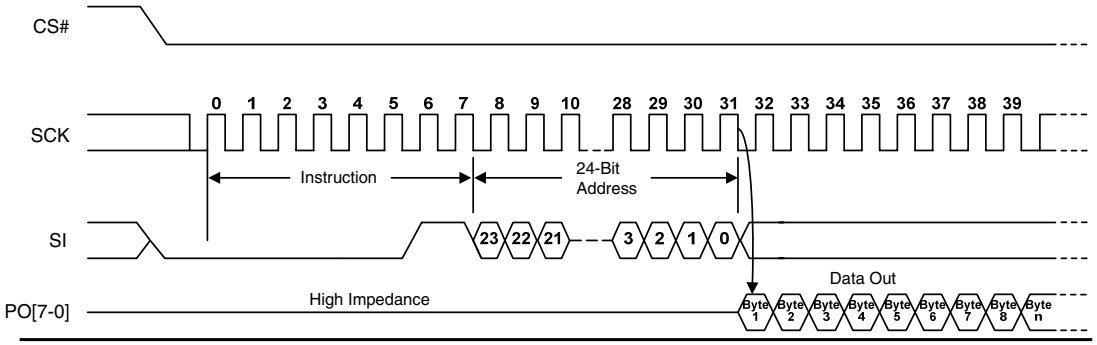
Figure 9.1 Read Data Bytes (READ) Command Sequence



9.1.2 Parallel Mode

In parallel mode, the maximum SCK clock frequency is 6 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The memory array output will be the same as in the serial mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. This means that 256 bytes of data can be copied into the 256 byte wide page write buffer in 256 clock cycles instead of in 2,048 clock cycles.

Figure 9.2 Parallel Read Instruction Sequence



Notes

1. *1st Byte = "03h".*
2. *2nd Byte = Address 1, MSB first (bits 23 through 16).*
3. *3rd Byte = Address 2, MSB first (bits 15 through 8).*
4. *4th Byte = Address 3, MSB first (bits 7 through 0).*
5. *From the 5th Byte, SO will output the array data.*
6. *In parallel mode, the maximum clock frequency (Fsck) is 6 MHz.*
7. *For parallel mode operation, the device requires an Enter Parallel Mode command (55h) before the READ command. An Exit Parallel Mode (45h) command or a power-down / power-up sequence is required to exit the parallel mode.*

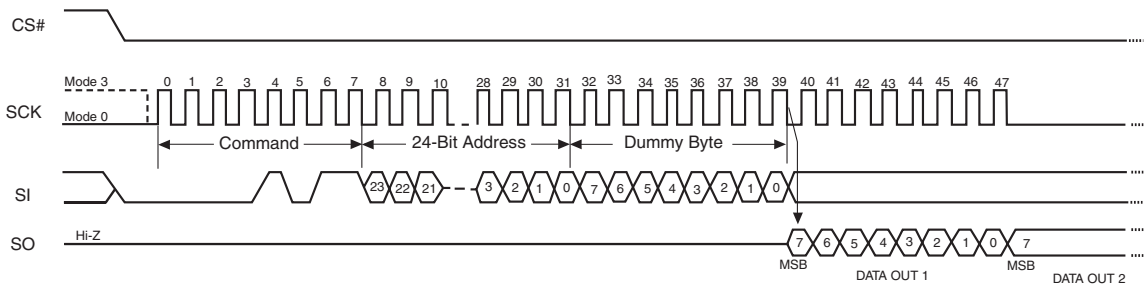
9.2 Read Data Bytes at Higher Speed (FAST_READ: 0Bh)

The FAST_READ command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 104 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 9.3 and Table 9.3. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output.

Figure 9.3 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



9.3 Read Identification (RDID: 9Fh)

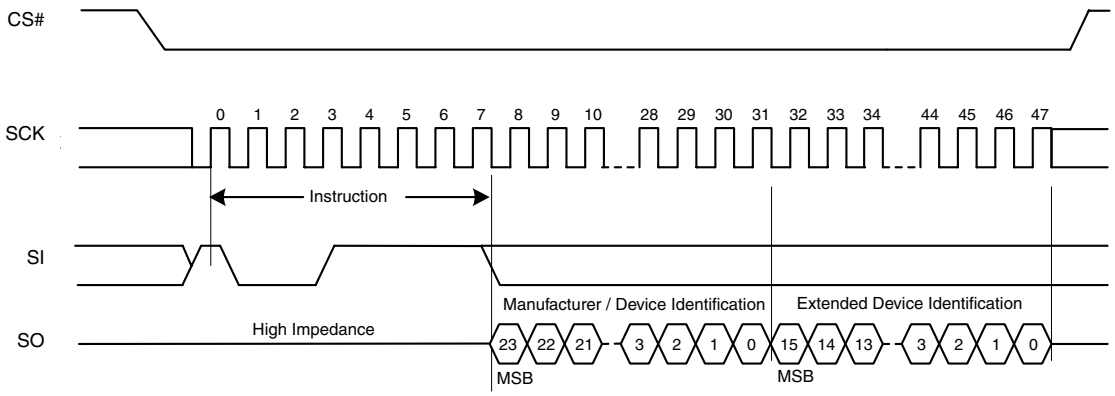
9.3.1 Serial Mode

The Read Identification (RDID) instruction opcode allows the 8-bit manufacturer identification to be read, follow by two bytes of device identification. The manufacturer identification is assigned by JEDEC. The device identification is assigned by the device manufacturer.

The device is first selected by driving the CS# chip select input pin to the logic low state. After this, the RDID 8-bit instruction opcode is shifted in onto the SI serial input pin. After the last bit of the RDID instruction opcode is shifted into the device, a byte of manufacturer identification, two bytes of device identification and two bytes of extended device identification will be shifted sequentially out of the SO serial output pin. Each bit is shifted out during the falling edge of the SCK serial clock signal. The maximum clock frequency for the RDID (9Fh) command is at 40 MHz (Normal Read).

The Read Identification (RDID) instruction sequence is terminated by driving the CS# chip select input pin to the logic high state anytime during data output. After issuing any Read ID instruction opcodes (90h, 9Fh, ABh), driving the CS# chip select input pin to the logic high state will automatically send the device into the standby mode. Driving the CS# chip select input pin to the logic low state again will automatically send the device out of the standby mode and into the active mode.

Figure 9.4 Read Identification Command Sequence and Data Out Sequence



9.3.2 Parallel Mode

In parallel mode, the maximum SCK clock frequency is 10 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The method of memory content output will be the same compared to the serial mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. In this case, the manufacturer identification will be output during the first byte cycle and the device identification during the second and third byte cycles out of the PO7-PO0 serial output pins. To read ID in parallel mode requires a Parallel Mode Entry command (55h) to be issued before the RDID command. Once in the parallel mode, the flash memory will not exit parallel mode until a Parallel Mode Exit (45h) command is given to the flash device, or upon power down/power up sequence.

Figure 9.5 Parallel Read_ID Command Sequence and Data Out Sequence

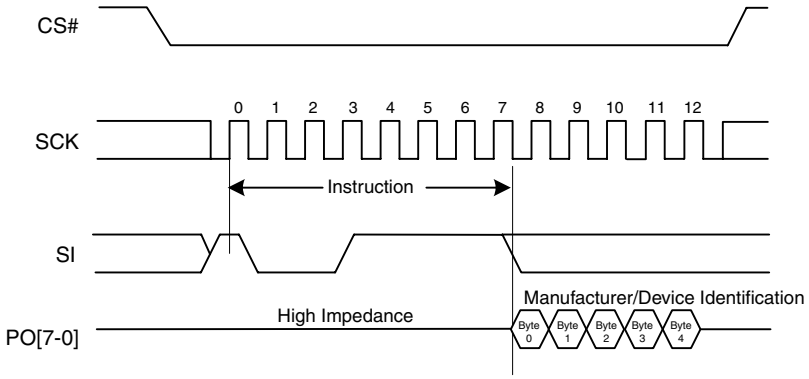


Table 9.1 Manufacturer & Device Identification, RDID (9Fh)

Manufacturer Identification	Device Identification		Extended Device Identification	
Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
01h	20h	18h	03h	03h

9.4 Read Manufacturer and Device ID (READ_ID: 90h)

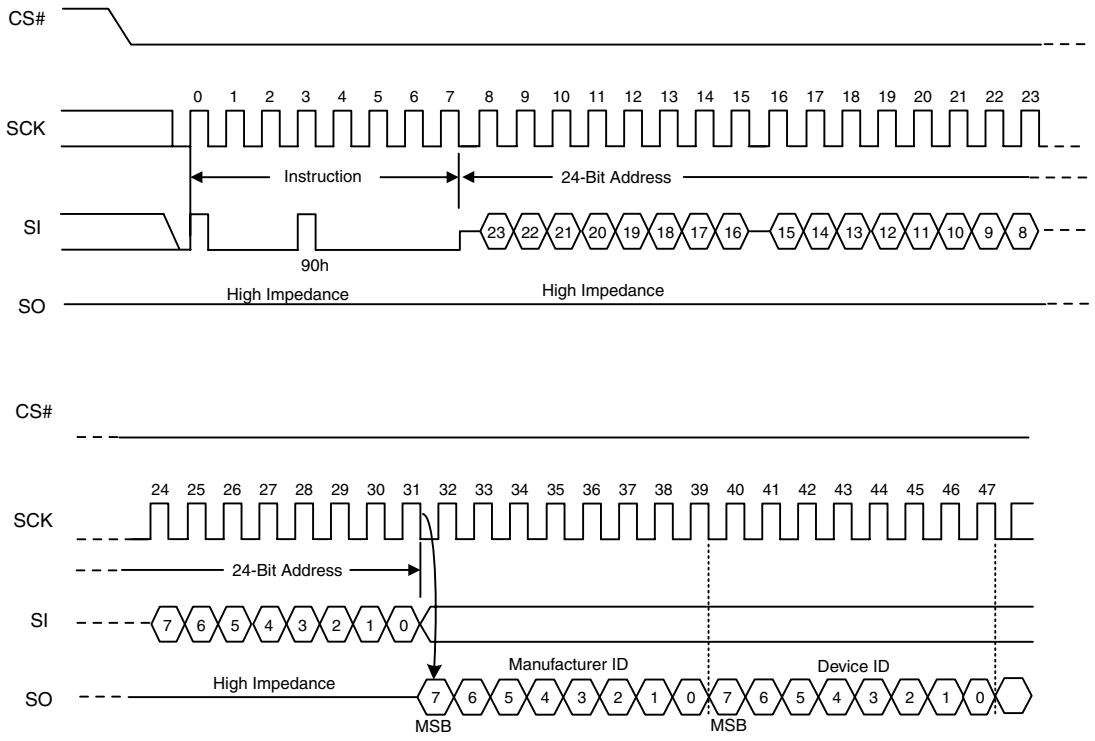
9.4.1 Serial Mode

The READ_ID (90h) instruction identifies the Device Manufacturer ID and the Device ID. The instruction is initiated by driving the CS# pin low and shifting in (via the SI input pin) the instruction code “90h” followed by a 24-bit address of XXXXX0h. (X: High or Low) Following this, the Manufacturer ID and the Device ID are shifted out on SO output pin starting after the falling edge of the SCK serial clock input signal. The Manufacturer ID and the Device ID are always shifted out on the SO output pin with the MSB first, as shown in Figure 9.6. If the 24-bit address is set to XXXXX1h, then the Device ID is read out first followed by the Manufacturer ID. Note that the upper 23 bits of the address do not have to be 0’s and can be don’t cares. Once the device is in READ_ID mode, the Manufacturer ID and Device ID output data toggles between address 000000H and 000001H until terminated by a low to high transition on the CS# input pin. After the first 24-bit address is provided, the user must wait 16 clock cycles for both the Manufacturer ID and Device ID to be output on the SO output pin. The maximum clock frequency for the READ_ID (90h) command is at 104 MHz (Fast Read). Parallel Mode the maximum clock frequency is 10 Mhz.

The Manufacturer ID & Device ID is output continuously until terminated by a low to high transition on CS# chip select input pin.

After issuing READ_ID instruction, driving the CS# chip select input pin to the logic high state will automatically send the device into the standby mode. Driving the CS# chip select input pin to the logic low state again will automatically sent the device out of the standby mode and into the active mode.

Figure 9.6 Serial READ_ID Instruction Sequence



9.4.2 Parallel Mode

The maximum clock frequency allowed on the SCK input pin in parallel mode is 10 MHz. The Parallel Mode Entry command (55h) must be issued before writing the READ_ID command. Once in the parallel mode, the flash memory will not exit parallel mode until a Parallel Mode Exit (45h) command is given to the flash device, or upon power-down/power-up sequence.

Figure 9.7 Parallel Read_ID Instruction Sequence

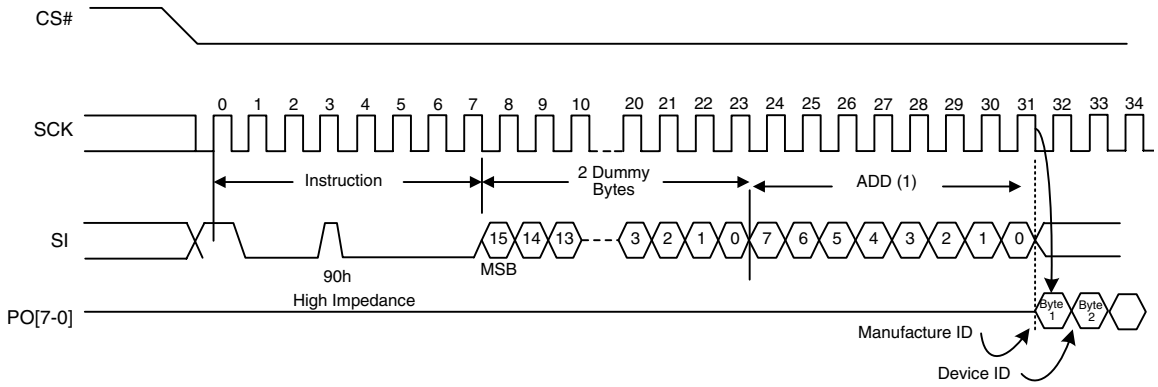


Table 9.2 READ_ID Command and Data

Description	Address	Data
Manufacturer Identification	00000h	01h
Device Identification (Memory Capacity)	00001h	17h

9.5 Deep Power Down (DP: B9h)

The Deep Power Down (DP) command provides the lowest power consumption mode of the device. It is intended for periods when the device is not in active use, and ignores all commands except for the Release from Deep Power Down (RES) command. The standard standby mode, which the device goes into automatically when CS# is high (and all operations in progress are complete), should generally be used for the lowest power consumption when the quickest return to device activity is required.

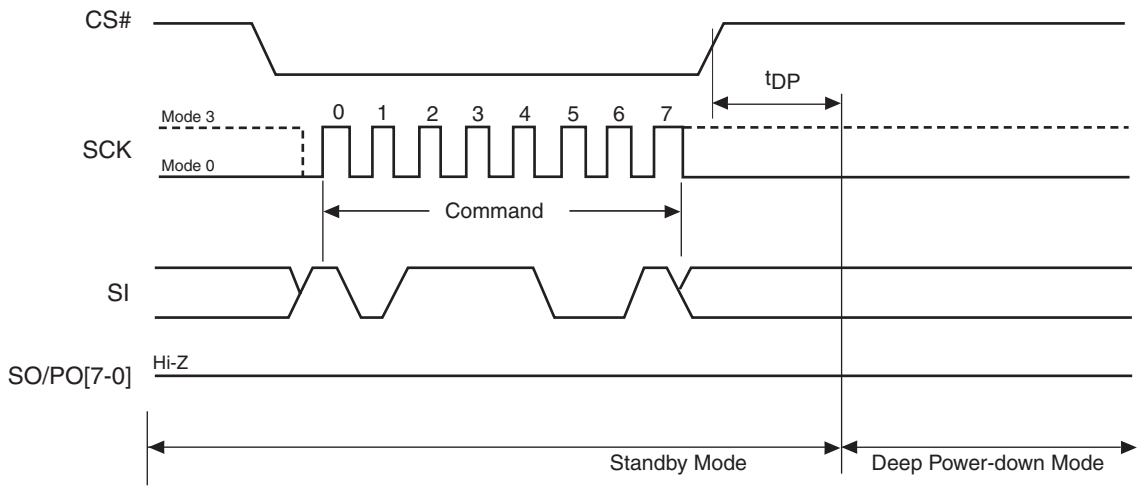
The host system must drive CS# low, and then write the DP command on SI. CS# must be driven low for the entire duration of the DP sequence. The command sequence is shown in Figure 9.8 and Table 9.3.

The host system must drive CS# high after the device has latched the 8th bit of the DP command, otherwise the device does not execute the command. After a delay of t_{DP}, the device enters the DP mode and current reduces from I_{SB} to I_{DP} (see Table 13.1 on page 26).

Once the device has entered the DP mode, all commands are ignored except the RES command (which releases the device from the DP mode). The RES command also provides the Electronic Signature of the device to be output on SO, if desired (see sections 9.6 and 9.7).

DP mode automatically terminates when power is removed, and the device always powers up in the standard standby mode.

Figure 9.8 Deep Power Down (DP) Command Sequence



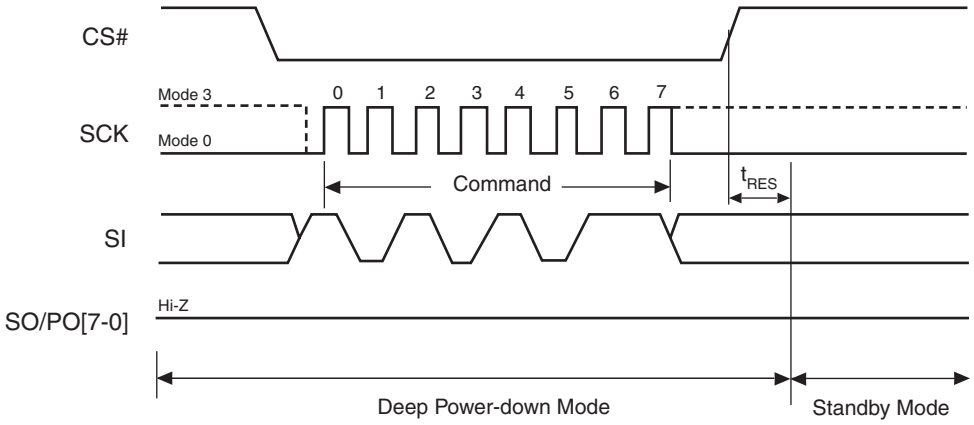
9.6 Release from Deep Power Down (RES: ABh)

The device requires the Release from Deep Power Down (RES) command to exit the Deep Power Down mode. When the device is in the Deep Power Down mode, all commands except RES are ignored.

The host system must drive CS# low and write the RES command to SI. CS# must be driven low for the entire duration of the sequence. The command sequence is shown in Figure 9.9 and Table 9.3 on page 23.

The host system must drive CS# high $t_{RES(max)}$ after the 8-bit RES command byte. The device transitions from DP mode to the standby mode after a delay of t_{RES} (see Table 15.1 on page 27). In the standby mode, the device can execute any read command.

Figure 9.9 Release from Deep Power Down (RES) Command Sequence



9.7 Release from Deep Power Down and Read Electronic Signature (RES: ABh)

9.7.1 Serial Mode

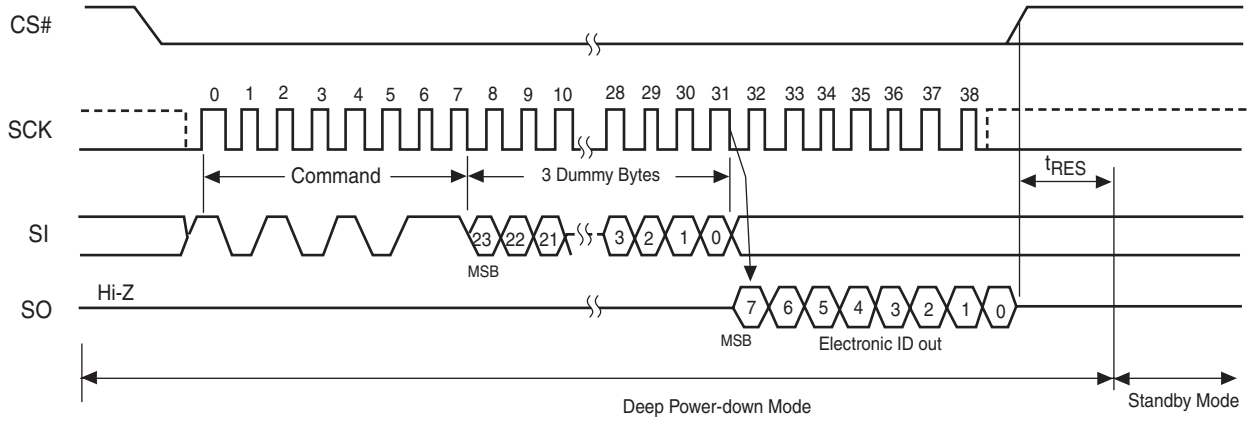
This command reads the old-style Electronic Signature from the SO serial output pin. See Figure 9.10 and Table 9.3 for the command sequence and signature value. Please note that the Electronic Signature only consists of the Device ID portion of the 16-bit JEDEC ID that is read by the Read Identifier (RDID) instruction. The old style Electronic Signature is supported for backward compatibility, and should not be used for new software designs, which should instead use the JEDEC 16-bit Electronic Signature by issuing the Read Identifier (RDID) command.

The device is first selected by driving the CS# chip select input pin to the logic low state. The RES command is shifted in followed by three dummy bytes onto the SI serial input pin. After the last bit of the three dummy bytes is shifted into the device, a byte of Electronic Signature will be shifted out of the SO serial output pin. Each bit is shifted out during the falling edge of the SCK serial clock signal. The maximum clock frequency for the RES (ABh) command is at 104 MHz.

The Electronic Signature can be read repeatedly by applying multiples of eight clock cycles.

The RES instruction sequence is terminated by driving the CS# chip select input pin to the logic high state anytime during data output. After issuing any Read ID commands (90h, 9Fh, ABh), driving the CS# chip select input pin to the logic high state will automatically send the device into the standby mode. Driving the CS# chip select input pin to the logic low state again will automatically sent the device out of the standby mode and into the active mode.

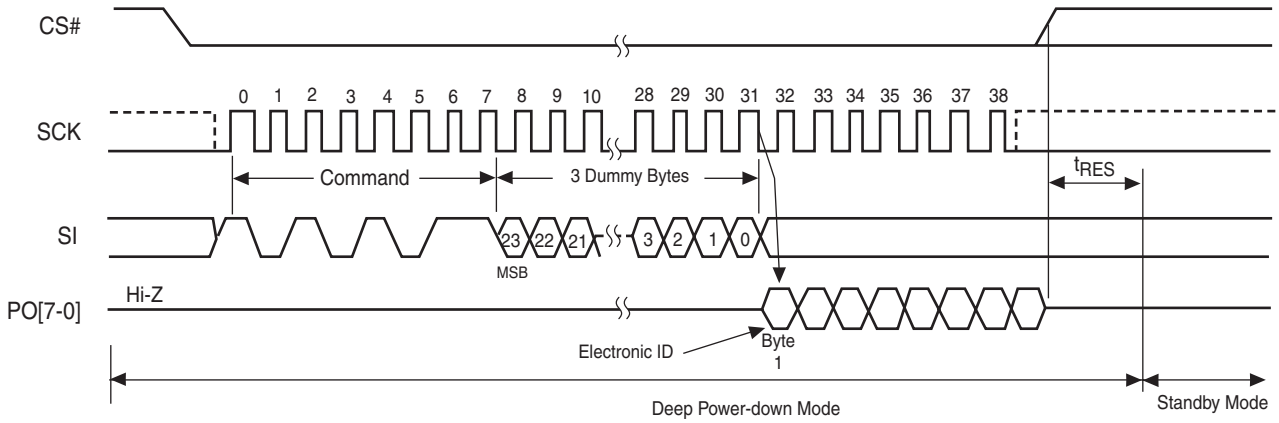
Figure 9.10 Serial Release from Deep Power Down and Read Electronic Signature (RES) Command Sequence



9.7.2 Parallel Mode

When the device is in parallel mode, the maximum SCK clock frequency is 10 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The method of memory content output will be the same compared to outside of parallel mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. In this case, the Electronic Signature will be output onto the P0[7–0] serial output pins.

Figure 9.11 Parallel Release from Deep Power Down and Read Electronic Signature (RES) Command Sequence



Notes

1. *In parallel mode, the maximum access clock frequency (Fsck) is 10 MHz (SCK pin clock frequency).*
2. *To release the device from Deep Power Down and read Electronic ID in parallel mode, a Parallel Mode Enter command (55h) must be issued before the RES command. The device will not exit parallel mode until a Parallel Mode Exit command (45h) is written, or upon power-down or power-up sequence.*
3. *Byte 1 will output the Electronic Signature.*

9.8 Command Definitions

Table 9.3 Command Definitions

Operation	Command	Description	One-Byte Command Code	Address Bytes	Dummy Byte	Data Bytes
Read	READ	Read Data Bytes	03h (0000 0011)	3	0	1 to ∞
	FAST_READ	Read Data Bytes at Higher Speed	0Bh (0000 1011)	3	1	1 to ∞
	RDID	Read Identification	9Fh (1001 1111)	0	0	1 to 3
	READ_ID	Read Manufacturer ID and Device ID	90h (1001 0000)	3	0	1 to ∞
Parallel Mode	Entry	Enter x8 Parallel Mode	55h (0101 0101)	0	0	0
	Exit	Exit x8 Parallel Mode	45h (0100 0101)	0	0	0
Power Saving	DP	Deep Power Down	B9h (1011 1001)	0	0	0
	RES	Release from Deep Power Down	ABh (1010 1011)	0	0	0
		Release from Deep Power Down and Read Electronic Signature	ABh (1010 1011)	0	3	1 to ∞

10. Power-up and Power-down

During power-up and power-down, certain conditions must be observed. CS# must follow the voltage applied on V_{CC}, and must not be driven low to select the device until V_{CC} reaches the allowable values as follows (see Figure 10.1 and Table 10.1):

- At power-up, V_{CC} (min.) plus a period of t_{PU}
- At power-down, V_{SS}

A pull-up resistor on Chip Select (CS#) typically meets proper power-up and power-down requirements.

At power-up, the device is in standby mode (not Deep Power Down mode) and the WEL bit is reset (0).

Each device in the host system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 µF), as a precaution to stabilizing the V_{CC} feed.

When V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold at power-down, all operations are disabled and the device does not respond to any commands.

Figure 10.1 Power-Up Timing Diagram

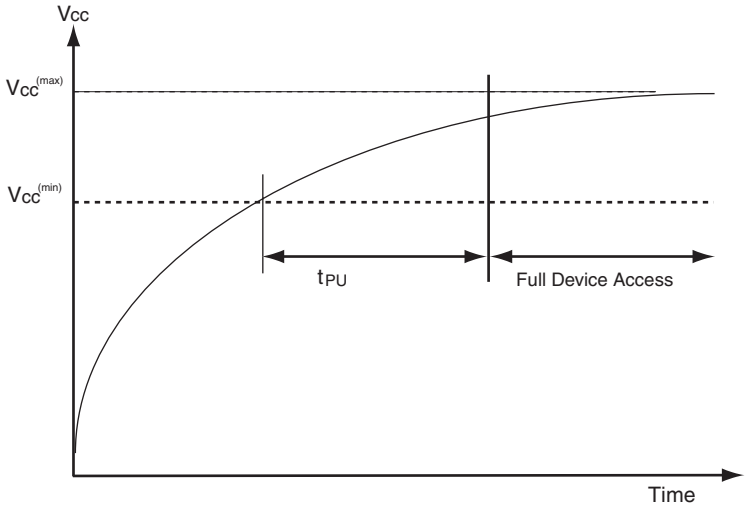


Table 10.1 Power-Up Timing Characteristics

Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC} (minimum)	2.7		V
t_{PU}	V_{CC} (min) to device operation	15		ms

11. Absolute Maximum Ratings

Do not stress the device beyond the ratings listed in this section, or serious, permanent damage to the device may result. These are stress ratings only and device operation at these or any other conditions beyond those indicated in this section and in the *Operating Ranges* on page 25 section of this document is not implied. Device operation for extended periods at the limits listed in this section may affect device reliability.

Table 11.1 Absolute Maximum Ratings

Description	Rating
Ambient Storage Temperature	–65°C to +150°C
Voltage with Respect to Ground: All Inputs and I/Os	–0.5 V to V_{CC}+0.5 V

Notes

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input at I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 11.2. Maximum DC voltage on output and I/O pins is 3.6 V. During voltage transitions output pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 11.2.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 11.1 Maximum Negative Overshoot Waveform

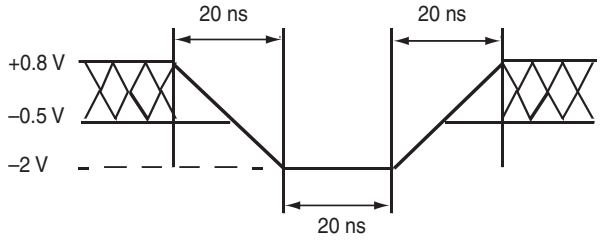
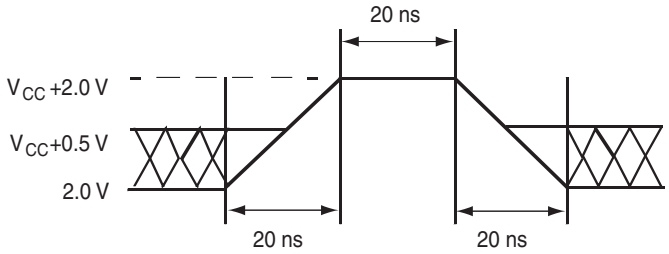


Figure 11.2 Maximum Positive Overshoot Waveform



12. Operating Ranges

Table 12.1 Operating Ranges

Description		Rating
Ambient Operating Temperature (T_A)	Industrial	–40°C to +85°C
Positive Power Supply	Voltage Range	2.7 V to 3.6 V

Note

Operating ranges define those limits between which functionality of the device is guaranteed.

13. DC Characteristics

This section summarizes the DC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 14.1 on page 26, when relying on the quoted parameters.

Table 13.1 DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions (See Note)		Min	Typ.	Max	Unit
V_{CC}	Supply Voltage			2.7		3.6	V
I_{CC1}	Active Read Current	SCK = 0.1 V_{CC}/ 0.9V_{CC}	104 MHz (Serial)			22	mA
		SCK = 0.1 V_{CC}/ 0.9V_{CC}	40 MHz (Serial: Fast Read Mode)			10	mA
			3 MHz (Parallel Mode)			10	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}, CS# = V_{CC}				200	µA
I_{DP}	Deep Power Down Current	V_{IN} = GND or V_{CC}, CS# = V_{CC}			3	20	µA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}, V_{CC} = V_{CC}max				2	µA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC}max				2	µA
V_{IL}	Input Low Voltage			–0.3		0.3 V_{CC}	V
V_{IH}	Input High Voltage			0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = $V_{CC\ min}$				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA		V_{CC} – 0.6			V

Note
Typical values are at T_A = 25° C and 3.0 V.

14. Test Conditions

Figure 14.1 AC Measurements I/O Waveform

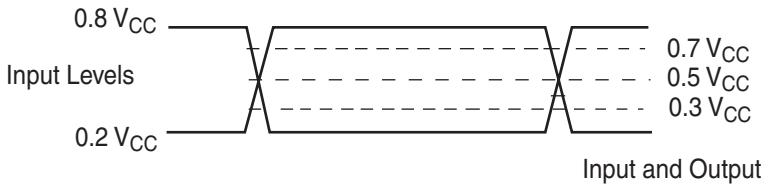


Table 14.1 Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

15. AC Characteristics

Table 15.1 AC Characteristics

Symbol	Parameter	Min	Typ (Notes)	Max (Notes)	Unit
F_{SCK}	SCK Clock Frequency READ command	D.C.		40 (Serial) 6 (Parallel)	MHz
F_{SCK}	SCK Clock Frequency for: FAST_READ, RDID, READ_ID, DP, RES (Note 2)	D.C.		104 (Serial) 10 (Parallel)	MHz
t_{CRT}	Clock Rise Time (Slew Rate)	0.1 (Serial) 0.25 (Parallel)			V/ns
t_{CFT}	Clock Fall Time (Slew Rate)	0.1 (Serial) 0.25 (Parallel)			V/ns
t_{WH}	SCK High Time	4.5 (Serial) 50 (Parallel)			ns
t_{WL}	SCK Low Time	4.5 (Serial) 50 (Parallel)			ns
t_{CS}	CS# High Time	100 (Serial) 20 (Parallel)			ns
t_{CSS}	CS# Setup Time (Note 1)	3			ns
t_{CSH}	CS# HOLD Time (Note 1)	3			ns
t_{HD}	HOLD# Setup Time (relative to SCK) (Note 1)	3			ns
t_{CD}	HOLD# Non-Active Hold Time (relative to SCK) (Note 1)	3			ns
t_{HC}	HOLD# Non-Active Setup Time (relative to SCK)	3			ns
t_{CH}	HOLD# Hold Time (relative to SCK)	3			ns
t_V	Output Valid	0		8 (Serial) 20 (Parallel)	ns
t_{HO}	Output Hold Time	0			ns
$t_{HD:DAT}$	Data in Hold Time	2 (Serial) 10 (Parallel)			ns
$t_{SU:DAT}$	Data in Setup Time	3 (Serial) 10 (Parallel)			ns
t_R	Input Rise Time			5	ns
t_F	Input Fall Time			5	ns
t_{LZ}	HOLD# to Output Low Z (Note 1)			8 (Serial) 20 (Parallel)	ns
t_{HZ}	HOLD# to Output High Z (Note 1)			8 (Serial) 20 (Parallel)	ns
t_{DIS}	Output Disable Time (Note 1)			8 (Serial) 20 (Parallel)	ns
t_{DP}	CS# High to Deep Power Down Mode			3	µs
t_{RES}	Release DP Mode			30	µs

Notes

1. *Not 100% tested.*
2. *FAST_READ is not valid in parallel mode.*

Figure 15.1 SPI Mode 0 (0,0) Input Timing

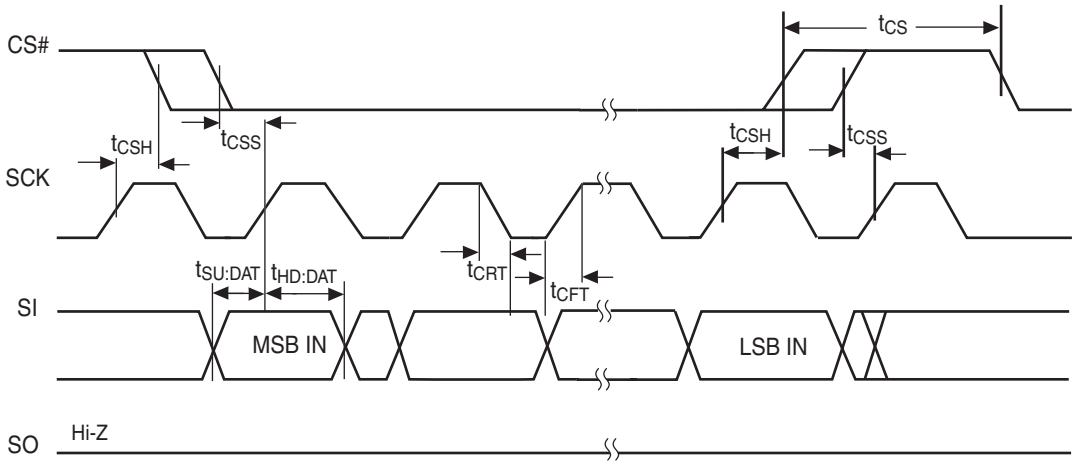


Figure 15.2 SPI Mode 0 (0,0) Output Timing

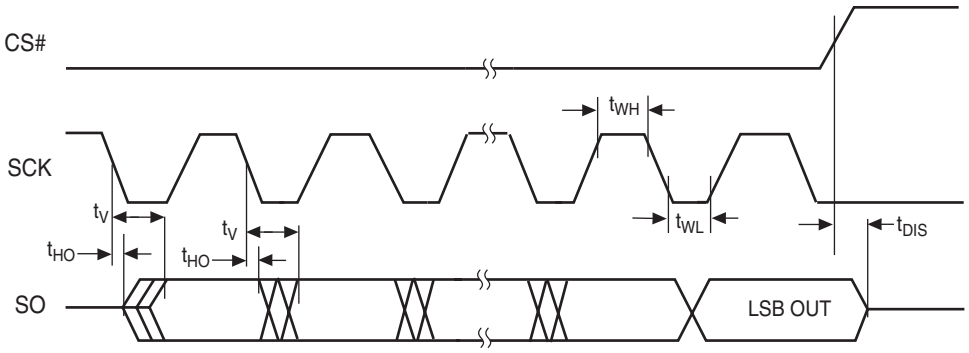
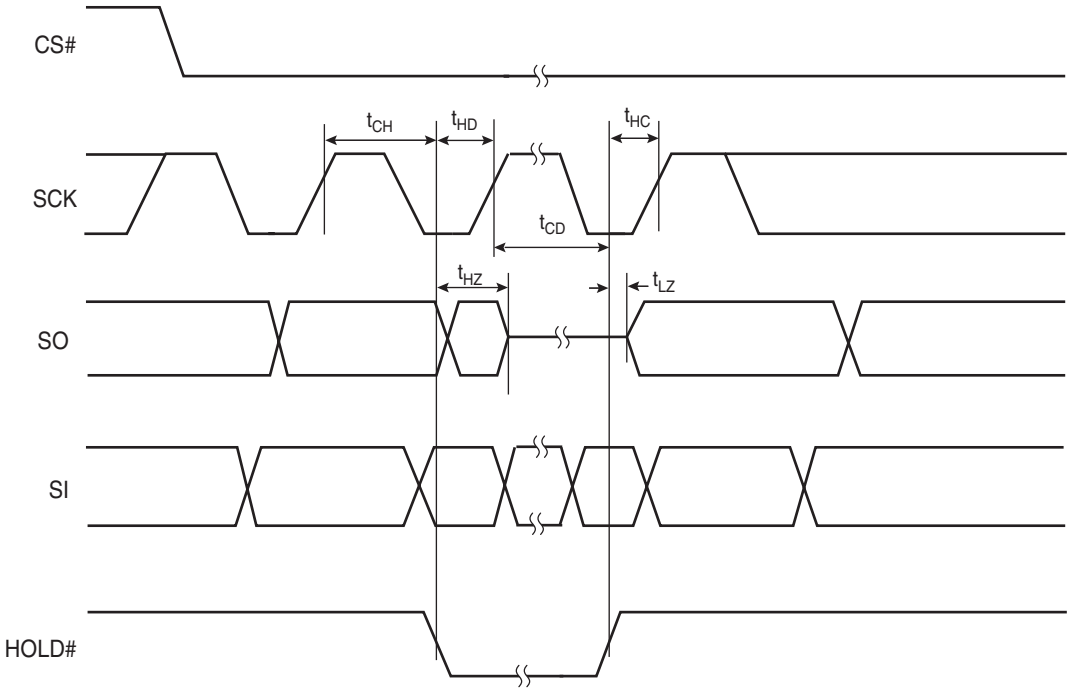
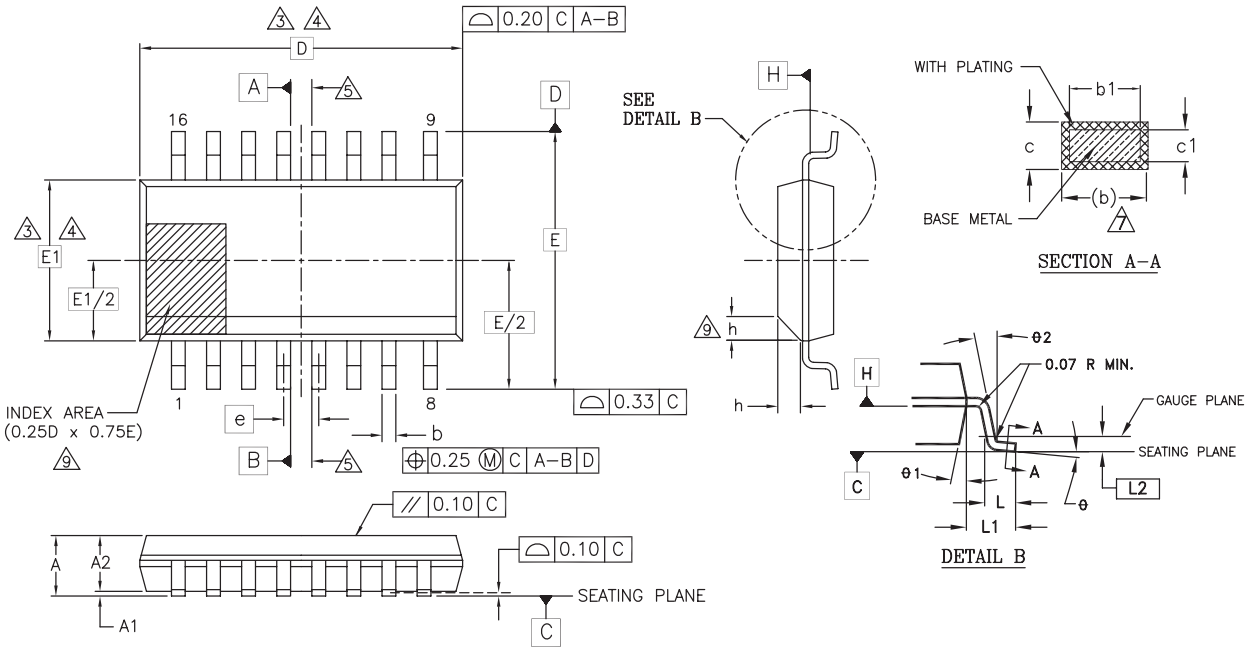


Figure 15.3 HOLD# Timing



16. Physical Dimensions

16.1 SO3 016 wide—16-pin Plastic Small Outline Package (300-mil Body Width)



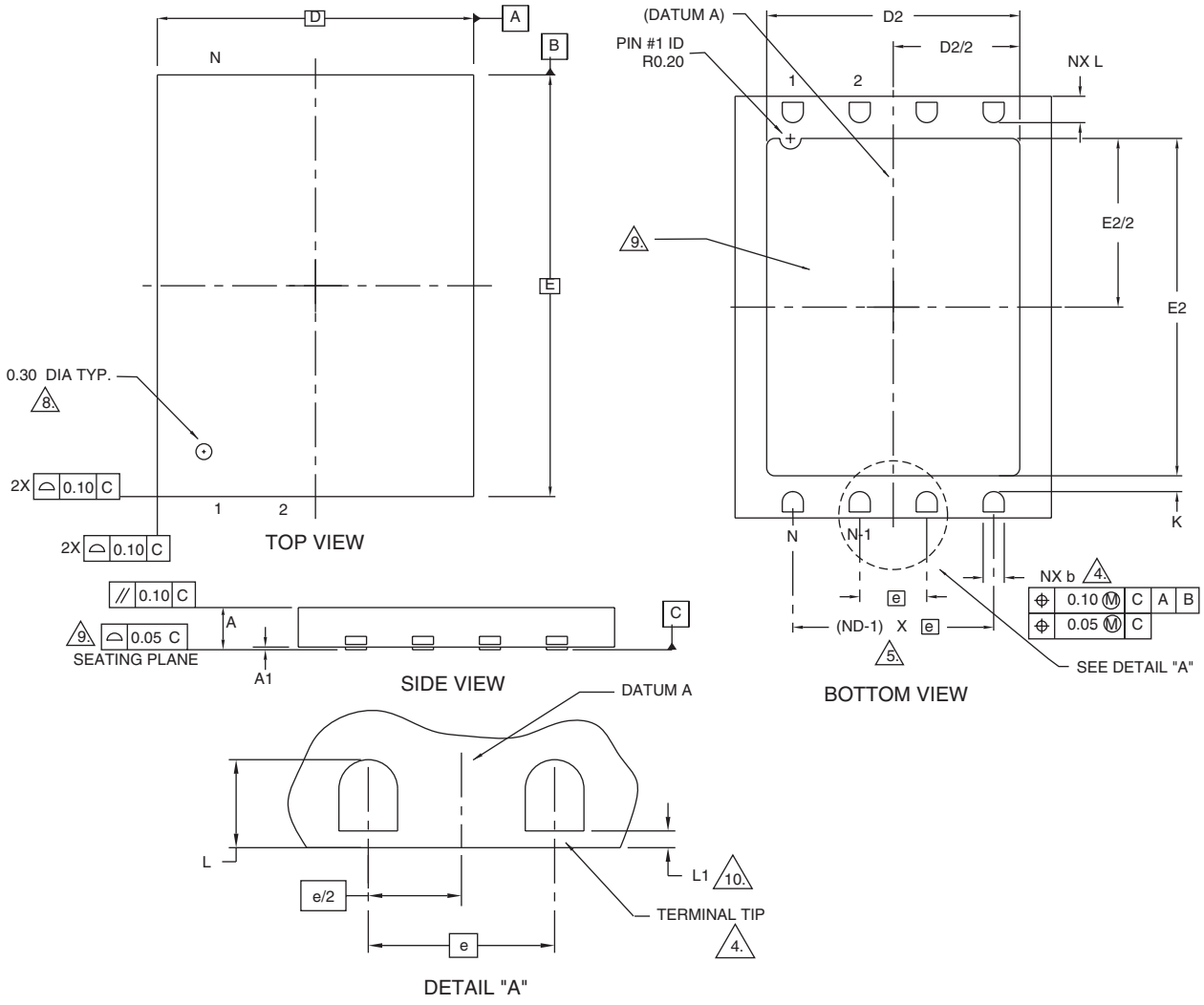
PACKAGE	SO3 016 (inches)		SO3 016 (mm)	
JEDEC	MS-013(D)AA		MS-013(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.081	0.104	2.05	2.55
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.008	0.013	0.20	0.33
c1	0.008	0.012	0.20	0.30
D	0.406 BSC		10.30 BSC	
E	0.406 BSC		10.30 BSC	
E1	0.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3601 \ 16-038.03 \ 8.31.6

16.2 WSON 8-contact (6 x 8 mm) No-Lead Package



QUAD FLAT NO LEAD PACKAGES (WSNB) - PLASTIC				
	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
e		1.27 BSC		
N		8		3
ND		4		5
L	0.45	0.50	0.55	
b	0.35	0.40	0.45	4
D2	4.70	4.80	4.90	
E2	6.30	6.40	6.50	
D		6.00 BSC		
E		8.00 BSC		
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
L1		0.15 MAX.		10
θ	0	---	12	2
K		0.20 MIN.		

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, SYM θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TOT HE NUMBER OF TERMINALS ON D SIDE.
6. MAXIMUM PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15 mm PULL BACK (L1) MAY BE PRESENT.

3408\ 16-038.28a

17. Revision History

Section	Description
Revision 01 (June 28, 2007)	
	Initial release.
Revision 02 (July 2, 2007)	
Global	Changed document status from *Advance Information* to *Preliminary*
Revision 03 (June 13, 2008)	
Global	Changed document status from *Preliminary* to *Full Production*

Colophon

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