Ordering number : ENA0868

SANYO Semiconductors
DATA SHEET

Monolithic Digital IC

LB1813MS — FDD Spindle Motor Driver

Overview

The LB1813MS is 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

Functions

- Three phase total wave linear driver.
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply).
- On-chip digital speed control : fosc=(1024×f_{FG})/D
  When SL1=high D=5/8
  SL1=low D=6/8
- Start/Stop circuit.
- Rotation speed switching.
- Current limiter circuit.
- On-chip index comparator (single hysteresis).
- On-chip index delay circuit.
- AGC circuit.
- Thermal protection circuit.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Maximum output current	I_O max1	t ≤ 0.5s	1.0	A
Steady maximum output current	I_O max2		0.7	A
Allowable power dissipation	Pd max	Independent IC	1	W
Operating temperature	Topr		-30 to +95	°C
Storage temperature	Tstg		-40 to 150	°C

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Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Suppiy voltage	V_{CC}		4.2 to 6.5	V

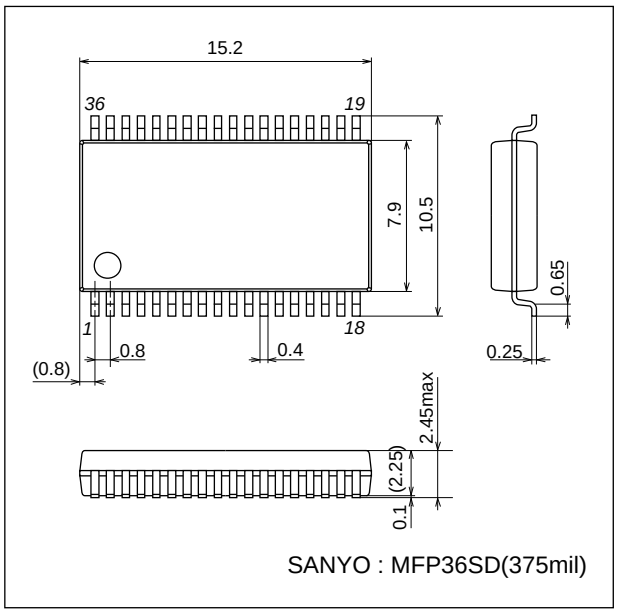
Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

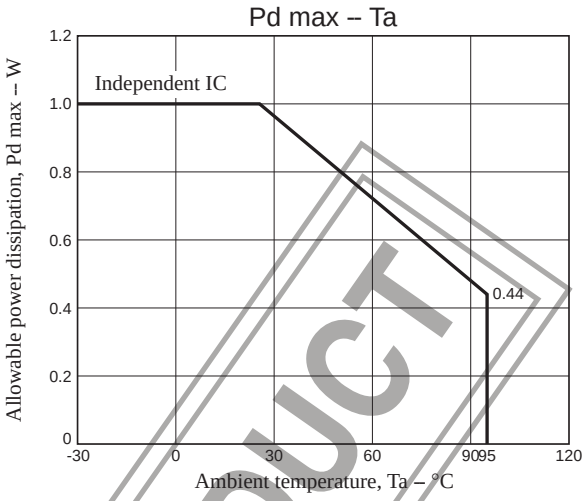
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	$I_{CCO}1$	V_{CC} = 5.0V (Stop)			0.4	mA
	$I_{CC}1$	V_{CC} = 5.0V (Steady)		20	30	mA
Time changeover bias current	I_{SL}				0.4	mA
Time changeover input voltage1	V_{SLL}		0		0.8	V
Time changeover input voltage2	V_{SLH}		2.0		V_{CC}	V
S/S bias current	$I_{S/S}$				0.1	mA
S/S start voltage	$V_{S/S}$		0		0.8	V
S/S stop voltage	$V_{S/S}$		2.0		V_{CC}	V
Hall-effect bias amplifier input current	I_{HB}				20	µA
In-phase input voltage range	Vh		2.2		V_{CC}-0.7	V
Differential input voltage range	Vdif		70		200	mVp-p
Input offset voltage	Vho	*			±10	mV
Hall-effect output voltage	V_H	I_H = 5mA		1.5	1.8	V
Leak current	I_{HL}	Stop			±10	µA
Output saturation voltage (sink plus source)	Vsat1	I_O = 0.35A, V_{CC} = 4.2V		1.2	1.4	V
	Vsat2	I_O = 0.70A, V_{CC} = 4.2V		1.5	2.0	V
Output leak current	I_{OL}				±10	mA
current limiter	Vref1		0.27	0.30	0.33	V
Control amplifier voltage gain	G_C			-6		dB
Voltage gain phase differential	ΔG_C				±1	dB
Integrated amplifier internal reference voltage	Vref2			V_{CC}/2		V
Integrated amplifier bias current	Iib				±1	µA
Integrated output voltage amplitude	Vi^+	Ii = -0.5mA with reference of Vref2		0.75		V
	Vi^-	Ii = 0.5mA with reference of Vref2		-1.4		V
Gain band width		*		1000		kHz
FG amplifier input voltage range	V_{FG}		5		100	mVp-p
FG amplifier voltage gain	G_{FG}			60		dB
FG amplifier input offset	$V_{FG}0$				±10	mV
FG amplifier internal reference voltage	$V_{FG}B$		2.20	2.50	2.80	V
Schmitt hysteresis width	ΔVsh1	High → Low *		25		mV
	ΔVsh2	Low → High *		25		mV
Schmitt input operation level	Vsh		1		V_{CC}-1	V
Speed disk recount number	N			1042		
Disk recount out low level voltage	V_{DL}	I_D = -0.5mA			0.3	V
Disk recount out high level voltage	V_{DH}	I_D = 0.5mA	V_{CC}-0.4			V
Disk recount out leak current	I_D1				±1.0	µA
Disk recount operation frequency	F_D	*			1.1	MHz
Oscillation range	F_{OSC}	*			1.1	MHz
Index bias current	I_{IDB}				±10	µA
In-phase input voltage range	V_{ID}		1.5		V_{CC}-0.5	V
Hysteresis setting current range	I_{IDO}		5	10	15	µA
Index output low level voltage	V_{IDL}	V_{ID} = 5V			0.4	V
Index output high level voltage	V_{IDH}	V_{ID} = 5V	4.5			V
Brake-down voltage	V_{DLDC}	V_{ID} = 5V		2.50		V
Delay output low level voltage	V_{DLL}	V_{ID} = 5V			0.4	V
Delay output high level voltage	V_{DLH}	V_{ID} = 5V	4.5			V
Thermal shutdown operating temperature	TSD	*	150	180		°C
Hysteresis temperature	ΔTSD	*		40		°C

Note : *) Marked values are guaranteed by the design itself and therefore do not require measurement.

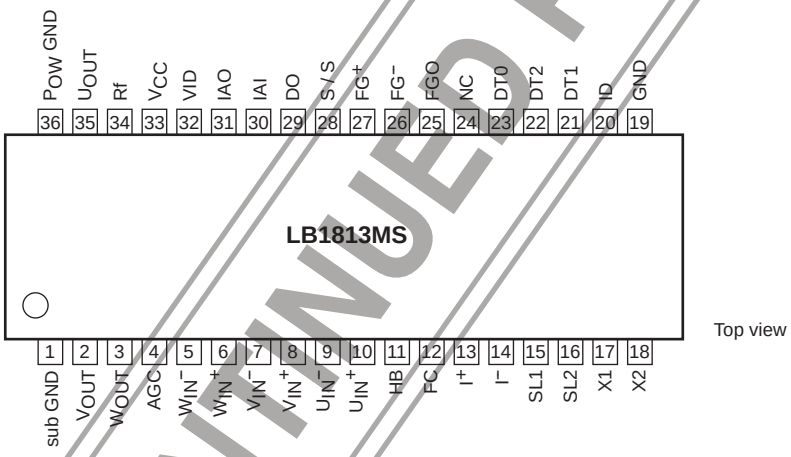
Package Dimensions

unit : mm (typ)
3129B

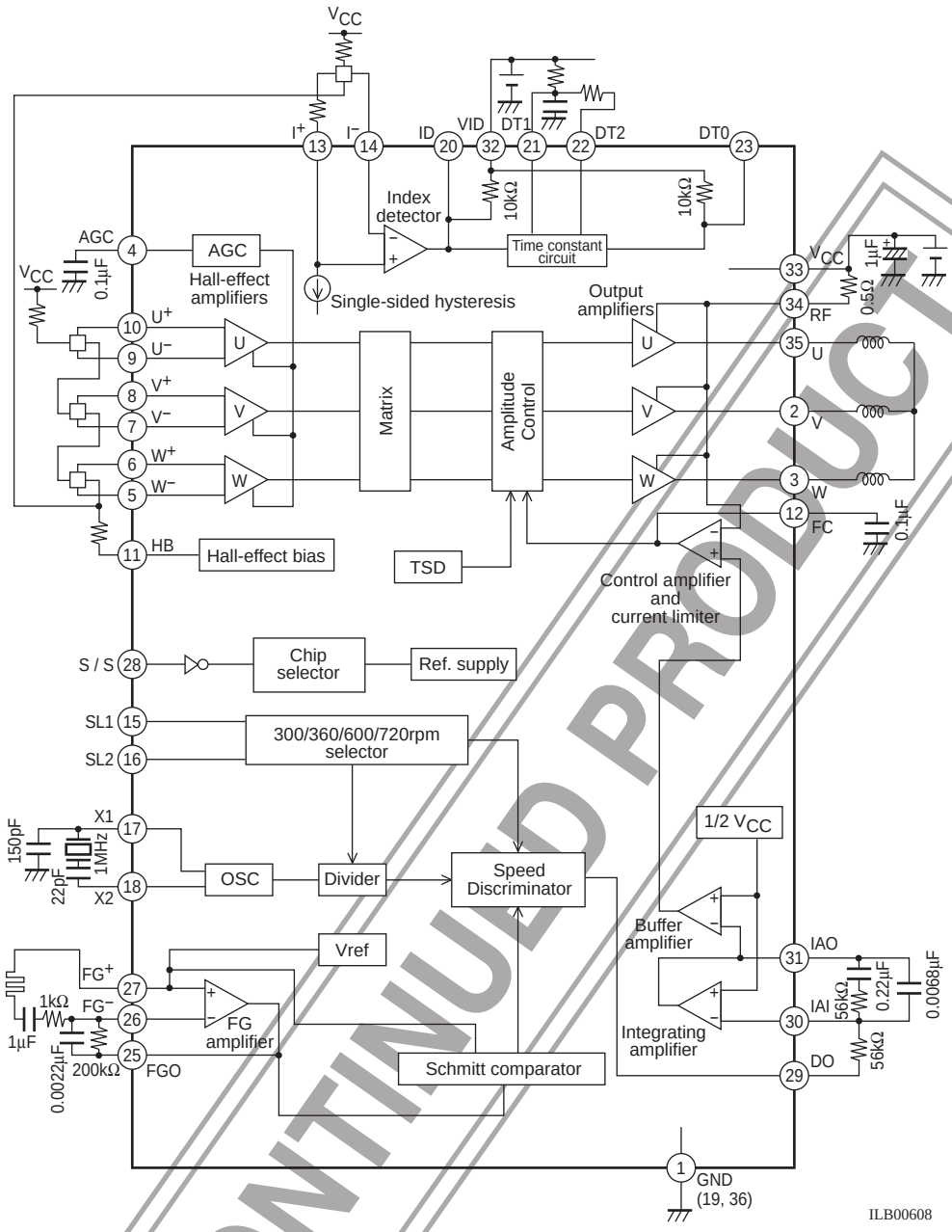




Pin Assignment



Block Diagram



Each parameter is a reference value.
However, depending on the motor, this may not apply.

Truth Table

	Source → sink	Hall-effect input		
		U	V	W
1	V-phase → W-phase	H	H	L
2	V-phase → U-phase	L	H	L
3	W-phase → U-phase	L	H	H
4	W-phase → V-phase	L	L	H
5	U-phase → V-phase	H	L	H
6	U-phase → W-phase	H	L	L

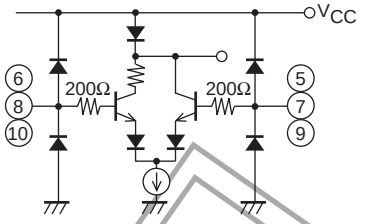
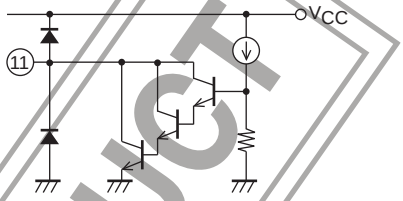
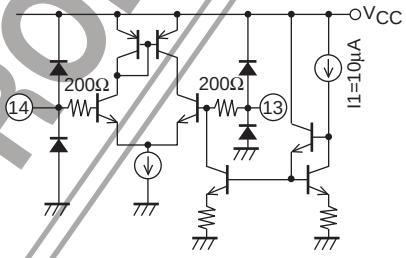
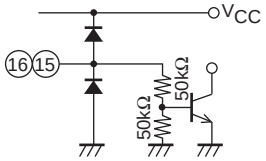
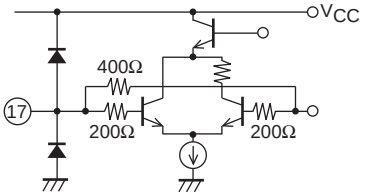
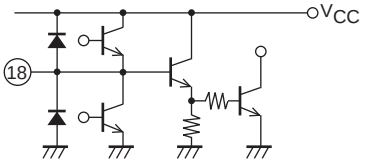
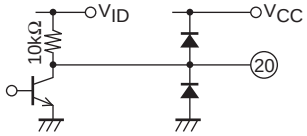
When an high level exists for Hall-effect input.

$U^+ > U^-$

$V^+ > V^-$

$W^+ > W^-$

Pin Function

Pin No.	Symbol	Pin voltage	Pin function	Equivalent circuit
5 6 7 8 9 10	W^- W^+ V^- V^+ U^- U^+	2.2V min V_{CC}-0.7V max	· W-phase Hall-effect input pin. $W^+ > W^-$ is established when logic is at an high level. · V-phase Hall-effect input pin. $V^+ > V^-$ is established when logic is at an high level. · U-phase Hall-effect input pin. $U^+ > U^-$ is established when logic is at an high level.	
11	HB	1.5V typ I_H=5mA	· Minus pin for Hall-effect bias. When stopped, switches open and Hall-effect bias severs.	
12	FC		· Frequency characteristics revision pin. By installing a capacitor between this pin and GND, close-loop oscillation for the current control system halts.	
13 14	I+ I-	1.5V typ V_{CC}-0.5 max	· Index input pin. When the I^+ pin is at an low level, I1 operates with the fixed current of I1=10μA and when at an high level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I^+ pin.	
15 16	SL1 SL2	High: 2.0V min Low: 0.8V max High: 2.0V min Low: 0.8V max	· Time changeover pin. fosc=1MHz FG: 60pulse/round	
17	X1		· Reference clock generating pin.	
18	X2			
19	GND		· Ground pin. Grounded as with pins 1 and 36.	
20	ID	High: 4.5V min Low: 0.4V max (When V_{ID}=5V)	· Index pulse output pin.	

SL2 \ SL1	H	L
H	600rpm	300rpm
L	720rpm	360rpm

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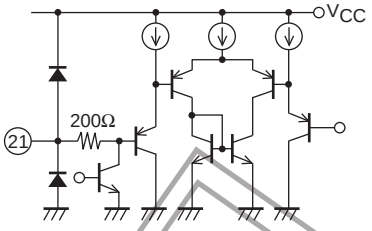
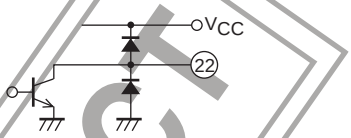
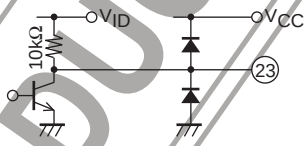
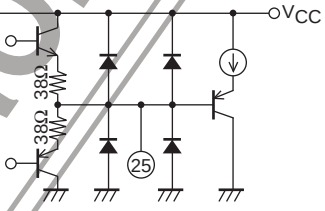
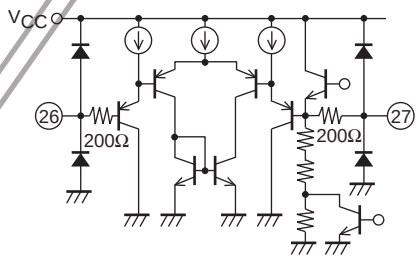
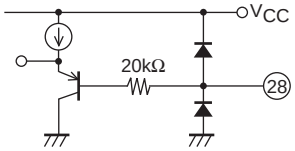
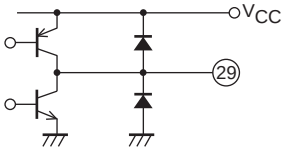
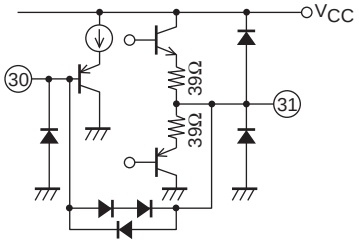
Pin No.	Symbol	Pin voltage	Pin function	Equivalent circuit
21	DT1		· Pin Connecting the external CR for the delay time constant circuit.	
22	DT2		· Break-down current setting pin for the delay time constant circuit.	
23	DTO	High: 4.5V min Low: 0.4V max (When V_{ID}=5V)	· Index delay pulse output pin.	
25	FG0		· FG amplifier output pin.	
26	FG^-		· FG amplifier negative input pin.	
27	FG^+	2.48V (When V_{ID}=5V)	· FG amplifier positive input pin. Generates reference voltage within IC.	
28	S/S	High: 2.0V min Low: 0.8V max	· Start/Stop changeover pin. Low level active.	
29	DO		· Speed discriminator output pin.	
30	IAI		· Integrated amplifier input pin.	
31	IAO		· Integrated amplifier output pin.	

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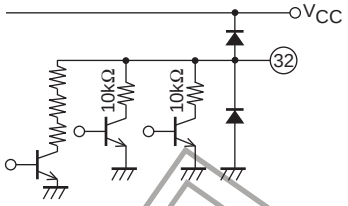
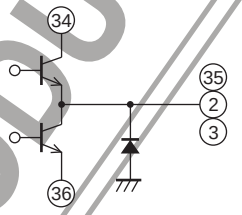
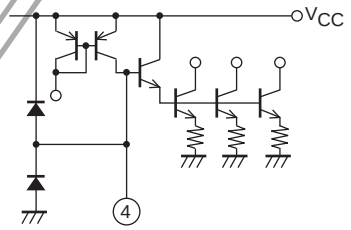
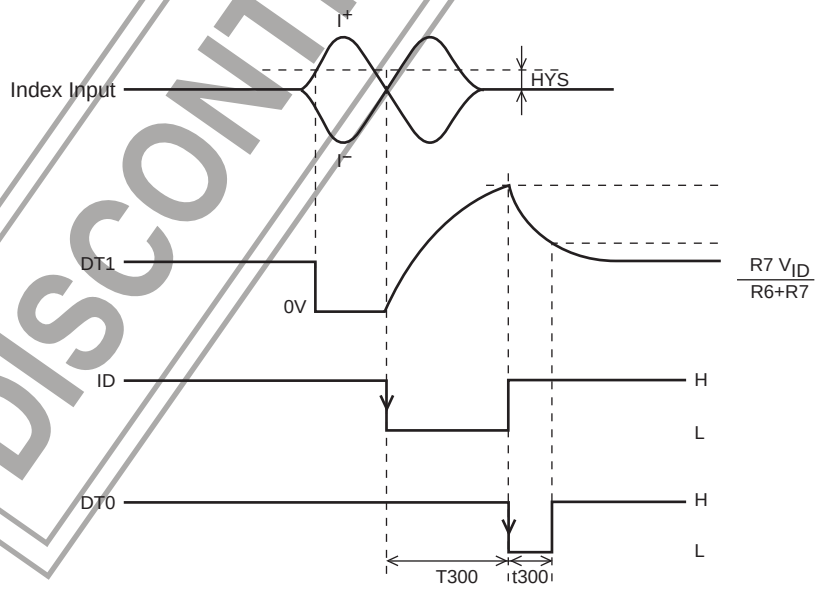
Pin No.	Symbol	Pin voltage	Pin function	Equivalent circuit
32	V_{ID}		· Index pulse output and index delay pulse output power supply pin. For applications when V_{CC} equals 5V, V_{CC}=V_{ID}=5V.	
33	V_{CC}		· Total power supply voltage pin except for V_{ID}. Voltage must be stable and free of ripple and noise interference.	
34	R_f		· Output current detection pin. By installing an Rf resistor between this pin and V_{CC}, output current is detected as voltage. Voltage detection at this pin activates the current limiter.	
35 2 3	U_{OUT} V_{OUT} W_{OUT}		· U-phase output pin. · V-phase output pin. · W-phase output pin.	
36	Power GND		· Output transistor ground pin.	
1	Sub GND		· Ground pin. Ground as with pins 19 and 36.	
4	AGC		· AGC (Automatic gain control) pin. Confides Hall-effect amplifier gain in response to Hall-effect input-frequency.	

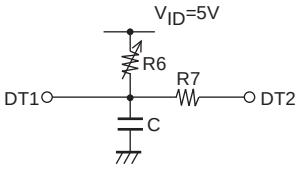
Index and Timing Chart



When SL1=high level

· T300 ≈ 0.693CR6

· $t300 \approx \frac{CR6\,R7}{R6+R7}\left\{0.405 + \ln\left(\frac{R6-R7}{R6-2R7}\right)\right\}$



When SL1=low level

· T360 ≈ 0.577CR6

· $t360 \approx \frac{CR6\,R7}{R6+R7}\left\{0.522 + \ln\left(\frac{0.781R6-R7}{R6-2R7}\right)\right\}$

Using only the ID pulse involves shorting DT1 and DT2.