



SANYO Semiconductors

DATA SHEET

LB1813MS — Monolithic Digital IC FDD Spindle Motor Driver

Overview

The LB1813MS is 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

Functions

- Three phase total wave linear driver.
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply).
- On-chip digital speed control : $f_{osc} = (1024 \times f_{FG}) / D$
When SL1=high D=5/8
SL1=low D=6/8
- Start/Stop circuit.
- Rotation speed switching.
- Current limiter circuit.
- On-chip index comparator (single hysteresis).
- On-chip index delay circuit.
- AGC circuit.
- Thermal protection circuit.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	V
Maximum output current	I _O max1	t ≤ 0.5s	1.0	A
Steady maximum output current	I _O max2		0.7	A
Allowable power dissipation	P _d max	Independent IC	1	W
Operating temperature	T _{opr}		-30 to +95	°C
Storage temperature	T _{stg}		-40 to 150	°C

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application" intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment, etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer, or who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LB1813MS

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		4.2 to 6.5	V

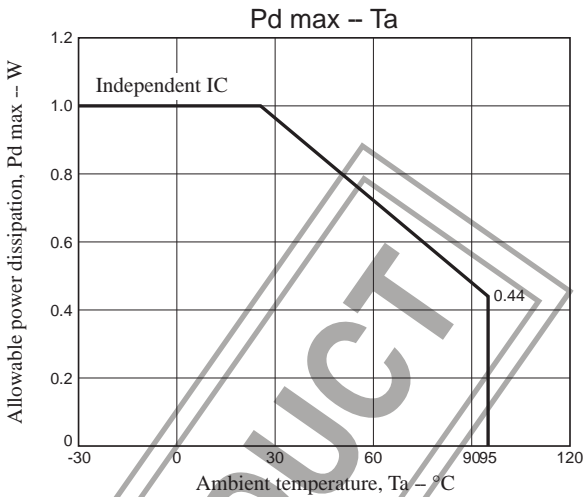
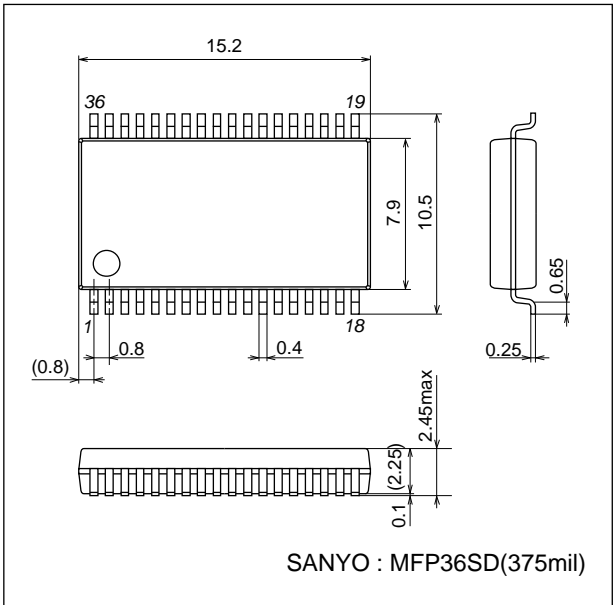
Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I _{CCO} 1	V _{CC} = 5.0V (Stop)			0.4	mA
	I _{CC} 1	V _{CC} = 5.0V (Steady)		20	30	mA
Time changeover bias current	I _{SL}				0.4	mA
Time changeover input voltage1	V _{SLL}		0		0.8	V
Time changeover input voltage2	V _{SLH}		2.0		V _{CC}	V
S/S bias current	I _{S/S}				0.1	mA
S/S start voltage	V _{S/S}		0		0.8	V
S/S stop voltage	V _{S/S}		2.0		V _{CC}	V
Hall-effect bias amplifier input current	I _{HB}				20	μA
In-phase input voltage range	V _h		2.2		V _{CC} -0.7	V
Differential input voltage range	V _{dif}		70		200	mVp-p
Input offset voltage	V _{ho}	*			±10	mV
Hall-effect output voltage	V _H	I _H = 5mA		1.5	1.8	V
Leak current	I _{HL}	Stop			±10	μA
Output saturation voltage (sink plus source)	V _{sat} 1	I _O = 0.35A, V _{CC} = 4.2V		1.2	1.4	V
	V _{sat} 2	I _O = 0.70A, V _{CC} = 4.2V		1.5	2.0	V
Output leak current	I _{OL}				±10	mA
current limiter	V _{ref} 1		0.27	0.30	0.33	V
Control amplifier voltage gain	G _C			-6		dB
Voltage gain phase differential	ΔG _C				±1	dB
Integrated amplifier internal reference voltage	V _{ref} 2			V _{CC} /2		V
Integrated amplifier bias current	I _{ib}				±1	μA
Integrated output voltage amplitude	V _i ⁺	I _i = -0.5mA with reference of V _{ref} 2		0.75		V
	V _i ⁻	I _i = 0.5mA with reference of V _{ref} 2		-1.4		V
Gain band width		*		1000		kHz
FG amplifier input voltage range	V _{FG}		5		100	mVp-p
FG amplifier voltage gain	G _{FG}			60		dB
FG amplifier input offset	V _{FG} 0				±10	mV
FG amplifier internal reference voltage	V _{FG} B		2.20	2.50	2.80	V
Schmitt hysteresis width	ΔV _{sh} 1	High → Low *		25		mV
	ΔV _{sh} 2	Low → High *		25		mV
Schmitt input operation level	V _{sh}		1		V _{CC} -1	V
Speed disk recount number	N			1042		
Disk recount out low level voltage	V _{DL}	I _D = -0.5mA			0.3	V
Disk recount out high level voltage	V _{DH}	I _D = 0.5mA	V _{CC} -0.4			V
Disk recount out leak current	I _D 1				±1.0	μA
Disk recount operation frequency	F _D	*			1.1	MHz
Oscillation range	F _{OSC}	*			1.1	MHz
Index bias current	I _{IDB}				±10	μA
In-phase input voltage range	V _{ID}		1.5		V _{CC} -0.5	V
Hysteresis setting current range	I _{IDO}		5	10	15	μA
Index output low level voltage	V _{IDL}	V _{ID} = 5V			0.4	V
Index output high level voltage	V _{IDH}	V _{ID} = 5V	4.5			V
Brake-down voltage	V _{DLDC}	V _{ID} = 5V		2.50		V
Delay output low level voltage	V _{DLL}	V _{ID} = 5V			0.4	V
Delay output high level voltage	V _{DLH}	V _{ID} = 5V	4.5			V
Thermal shutdown operating temperature	TSD	*	150	180		°C
Hysteresis temperature	ΔTSD	*		40		°C

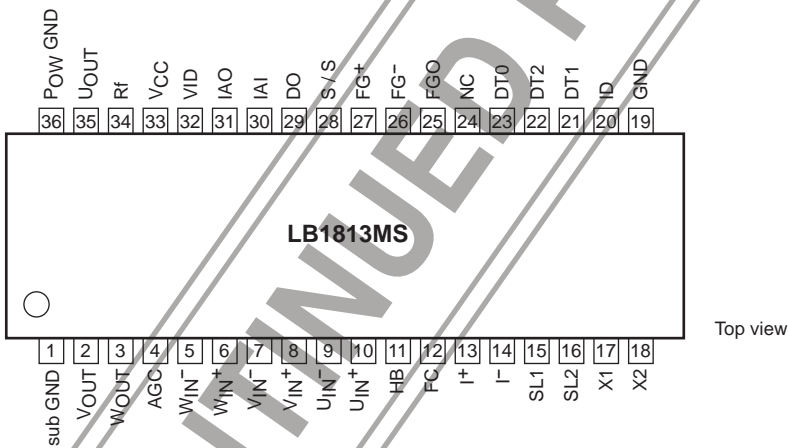
Note : *) Marked values are guaranteed by the design itself and therefore do not require measurement.

Package Dimensions

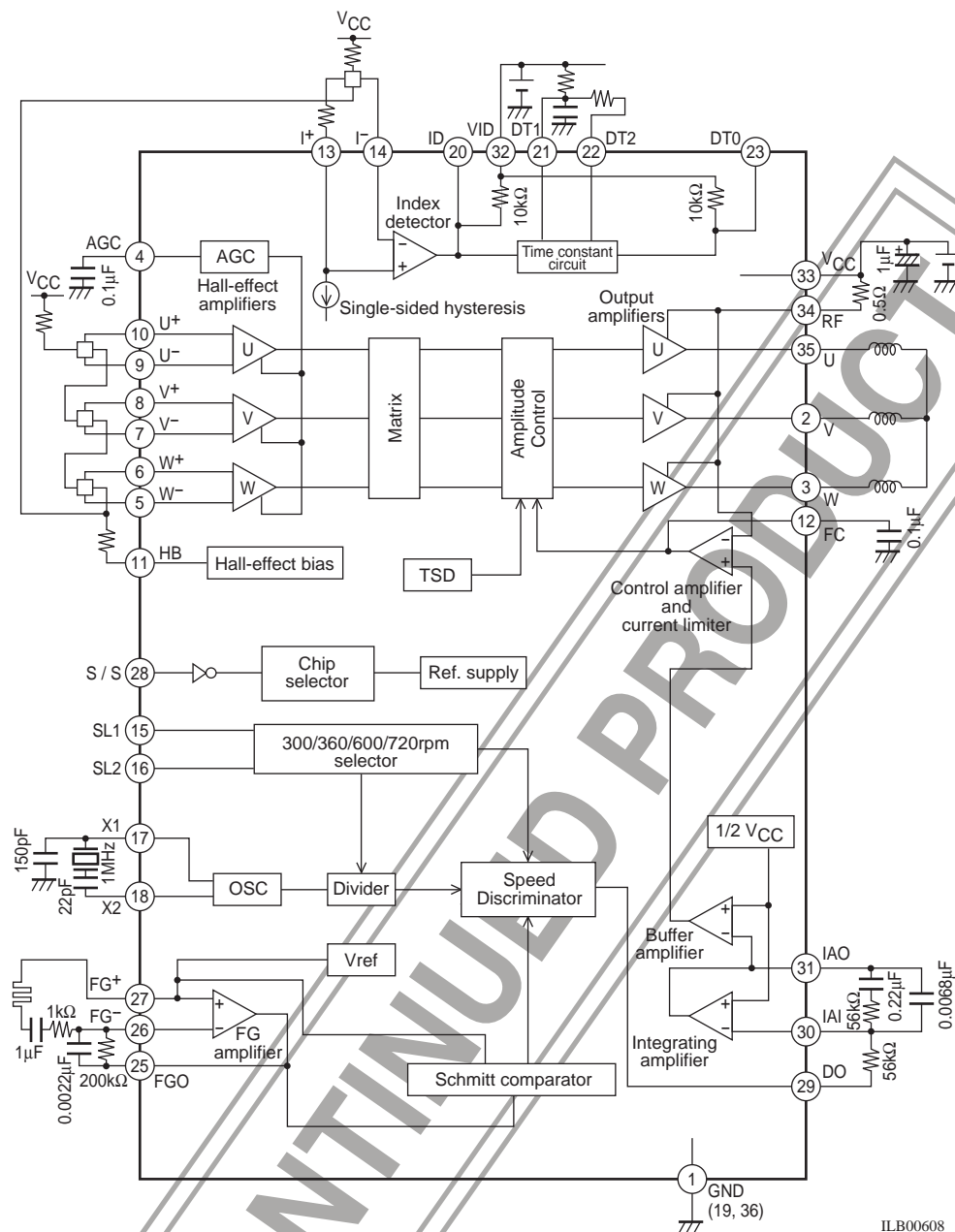
unit : mm (typ)
3129B



Pin Assignment



Block Diagram



Each parameter is a reference value.
However, depending on the motor, this may not apply.

Truth Table

	Source → sink	Hall-effect input		
		U	V	W
1	V-phase → W-phase	H	H	L
2	V-phase → U-phase	L	H	L
3	W-phase → U-phase	L	H	H
4	W-phase → V-phase	L	L	H
5	U-phase → V-phase	H	L	H
6	U-phase → W-phase	H	L	L

When an high level exists for Hall-effect input.

- U+ > U-
- V+ > V-
- W+ > W-

Pin Function

Pin No.	Symbol	Pin voltage	Pin function	Equivalent circuit								
5 6 7 8 9 10	W ⁻ W ⁺ V ⁻ V ⁺ U ⁻ U ⁺	2.2V min V _{CC} -0.7V max	<ul style="list-style-type: none">W-phase Hall-effect input pin. W⁺>W⁻ is established when logic is at an high level.V-phase Hall-effect input pin. V⁺>V⁻ is established when logic is at an high level.U-phase Hall-effect input pin. U⁺>U⁻ is established when logic is at an high level.									
11	HB	1.5V typ I _H =5mA	<ul style="list-style-type: none">Minus pin for Hall-effect bias. When stopped, switches open and Hall-effect bias severs.									
12	FC		<ul style="list-style-type: none">Frequency characteristics revision pin. By installing a capacitor between this pin and GND, close-loop oscillation for the current control system halts.									
13 14	I ⁺ I ⁻	1.5V typ V _{CC} -0.5 max	<ul style="list-style-type: none">Index input pin. When the I⁺ pin is at an low level, I1 operates with the fixed current of I1=10μA and when at an high level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I⁺ pin.									
15	SL1	High: 2.0V min Low: 0.8V max	<ul style="list-style-type: none">Time changeover pin. fosc=1MHz									
16	SL2	High: 2.0V min Low: 0.8V max	<table border="1"><tr><td>SL2 \ SL1</td><td>H</td><td>L</td></tr><tr><td>H</td><td>600rpm</td><td>300rpm</td></tr><tr><td>L</td><td>720rpm</td><td>360rpm</td></tr></table> <p>FG: 60pulse/round</p>		SL2 \ SL1	H	L	H	600rpm	300rpm	L	720rpm
SL2 \ SL1	H	L										
H	600rpm	300rpm										
L	720rpm	360rpm										
17	X1		<ul style="list-style-type: none">Reference clock generating pin.									
18	X2											
19	GND		<ul style="list-style-type: none">Ground pin. Grounded as with pins 1 and 36.									
20	ID	High: 4.5V min Low: 0.4V max (When V _{ID} =5V)	<ul style="list-style-type: none">Index pulse output pin.									

Continued to next page.

LB1813MS

Continued from preceding page.

Pin No.	Symbol	Pin voltage	Pin function	Equivalent circuit
21	DT1		· Pin Connecting the external CR for the delay time constant circuit.	
22	DT2		· Break-down current setting pin for the delay time constant circuit.	
23	DTO	High: 4.5V min Low: 0.4V max (When $V_{ID}=5V$)	· Index delay pulse output pin.	
25	FG0		· FG amplifier output pin.	
26	FG ⁻		· FG amplifier negative input pin.	
27	FG ⁺	2.48V (When $V_{ID}=5V$)	· FG amplifier positive input pin. Generates reference voltage within IC.	
28	S/S	High: 2.0V min Low: 0.8V max	· Start/Stop changeover pin. Low level active.	
29	DO		· Speed discriminator output pin.	
30	IAI		· Integrated amplifier input pin.	
31	IAO		· Integrated amplifier output pin.	

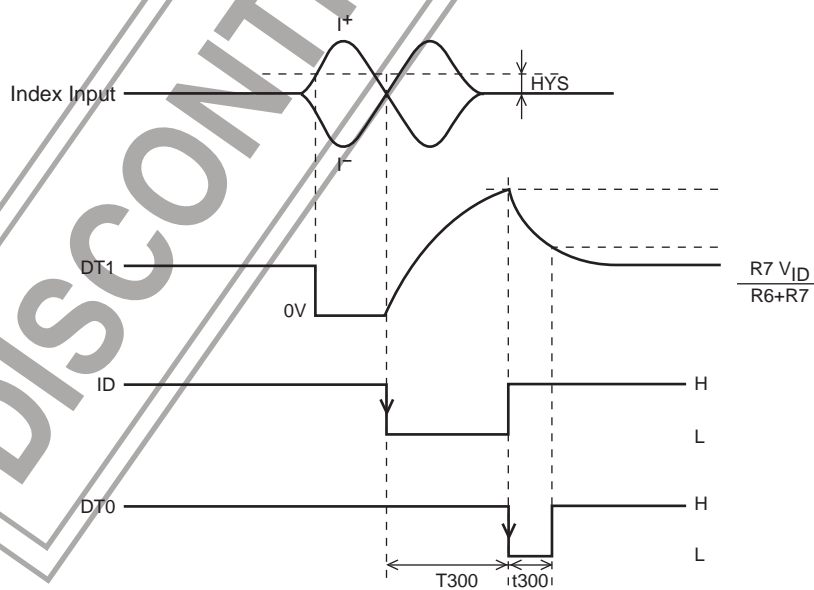
Continued to next page.

LB1813MS

Continued from preceding page.

Pin No.	Symbol	Pin voltage	Pin function	Equivalent circuit
32	V_{ID}		<ul style="list-style-type: none"> Index pulse output and index delay pulse output power supply pin. For applications when V_{CC} equals 5V, $V_{CC}=V_{ID}=5V$. 	
33	V_{CC}		<ul style="list-style-type: none"> Total power supply voltage pin except for V_{ID}. Voltage must be stable and free of ripple and noise interference. 	
34	R_f		<ul style="list-style-type: none"> Output current detection pin. By installing an R_f resistor between this pin and V_{CC}, output current is detected as voltage. Voltage detection at this pin activates the current limiter. 	
35 2 3	U_{OUT} V_{OUT} W_{OUT}		<ul style="list-style-type: none"> U-phase output pin. V-phase output pin. W-phase output pin. 	
36	Power GND		<ul style="list-style-type: none"> Output transistor ground pin. 	
1	Sub GND		<ul style="list-style-type: none"> Ground pin. Ground as with pins 19 and 36. 	
4	AGC		<ul style="list-style-type: none"> AGC (Automatic gain control) pin. Confides Hall-effect amplifier gain in response to Hall-effect input-frequency. 	

Index and Timing Chart



When SL1=high level

$$\cdot T300 \approx 0.693CR6$$

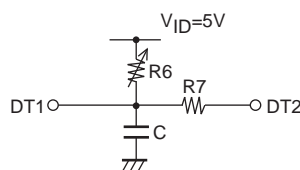
$$\cdot t300 \approx \frac{CR6R7}{R6+R7} \left\{ 0.405 + \ln \left(\frac{R6-R7}{R6-2R7} \right) \right\}$$

When SL1=low level

$$\cdot T360 \approx 0.577CR6$$

$$\cdot t360 \approx \frac{CR6R7}{R6+R7} \left\{ 0.522 + \ln \left(\frac{0.781R6-R7}{R6-2R7} \right) \right\}$$

Using only the ID pulse involves shorting DT1 and DT2.



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of June, 2007. Specifications and information herein are subject to change without notice.