

# CLC920

## APPLICATIONS:

- radar receivers
- professional video
- waveform analyzers
- instrumentation
- medical imaging

## DESCRIPTION:

The CLC920 is a 10-bit, flash, Analog-to-Digital converter, capable of encoding video bandwidth input signals at rates above 20 mega-samples per second (MSPS). Fabricated in a high-speed 1 micron bipolar process, the CLC920 provides high-quality performance over a wide operational range. An efficient design with tightly controlled processing provides untrimmed integral linearity to 0.1% (typ), and even tighter integral linearity to 0.05% (typ) is achievable through adjustments in the reference ladder inter-tap points.

The CLC920 has been designed to provide accurate and predictable performance, on the 10-bit level, with a minimum of external circuitry. Simple reference voltage circuitry and a conversion signal are all that are needed for operation. The 5MHz analog input bandwidth coupled with 1024 latching input comparators, eliminate the need for external track-and-hold circuits, even at data rates of 25MSPS. Additionally, dynamic performance can be dramatically improved with the use of an external track-and-hold like the CLC940. Both input bandwidth performance and effective conversion rate (through "ping-pong" techniques) can be enhanced with this technique in a very cost-effective manner.

The on-board output latches incorporate logic inversion circuitry, providing stable data in either binary or 2's complement format. The high-speed TTL compatible outputs are designed to function with both TTL and CMOS logic families. In addition to the digital output format flexibility, two overflow outputs are provided to signal analog input overrange conditions.

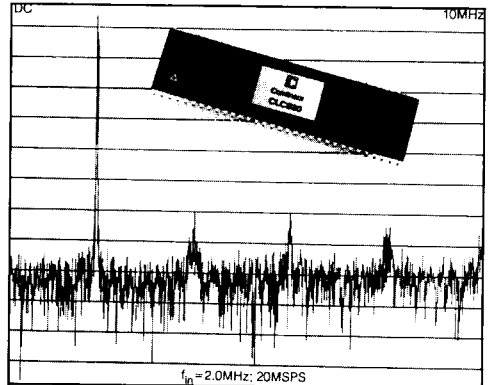
The CLC920 is available specified over the commercial temperature range (0°C to +70°C) and the military temperature range (-55°C to +125°C). Both versions of the CLC920 are packaged in a 64-pin ceramic DIP with an integrated heatsink. The CLC920A8D is fully compliant to MIL-STD-883.

## ORDERING INFORMATION

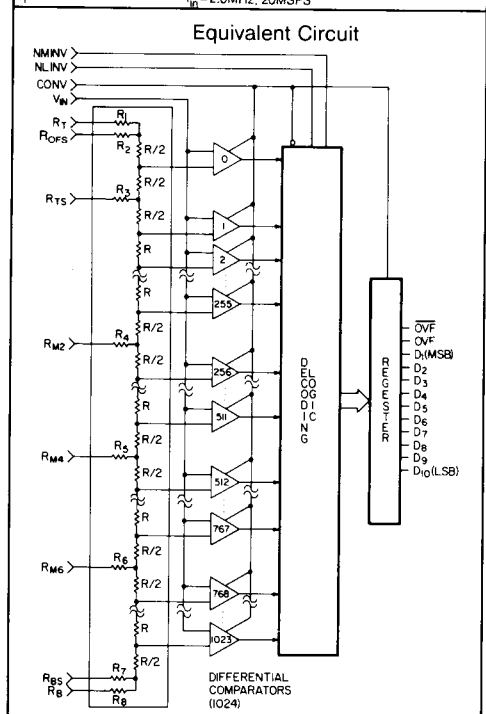
PART NUMBER	TEMPERATURE RANGE	DESCRIPTION
CLC920ACD	0°C to +70°C	64-Pin DIP, Commercial Temperature
CLC920A8D	-55°C to +125°C	64-Pin DIP, Military Temperature

## FEATURES (typical):

- 25MSPS encode rate
- 10-bit resolution
- full flash design
- reference ladder sense lines
- TTL compatible
- overflow outputs



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# Electrical Characteristics (+V<sub>CC</sub> = +5.0V; -V<sub>EE</sub> = -5.2V; V<sub>RT</sub> = +2.000V; V<sub>RB</sub> = -2.000V unless specified)

Parameters <sup>1</sup>	Conditions	typ	min and max ratings		units	symbol
Ambient Temperature CLC920A8D		+25°C	-55°C	+25°C	+125°C	
Ambient Temperature CLC920ACD		+25°C	0°C	+25°C	+70°C	
<b>LINEARITY<sup>2,5</sup></b>						
* differential non-linearity error		0.05	<0.1	<0.1	<0.1	%FS DNL
* integral non-linearity error		0.1	<0.2	<0.2	<0.2	%FS INL
* integral non-linearity error <sup>6</sup>		0.05	<0.1	<0.1	<0.1	%FS AINL
* code size			+10 to +250% guaranteed			CS
no missing codes						MC
<b>TIME DOMAIN PERFORMANCE</b>						
* conversion rate <sup>4,5</sup>		25	>20	>20	>20	MSPS CR
* aperture delay <sup>2,3</sup>			<15	<15	<15	ns TA
aperture uncertainty (jitter)		50				ps-rms TAU
* output propagation delay <sup>2,3</sup>			<37	<37	<37	ns TPD
* output hold time <sup>2,3</sup>			>5	>5	>5	ns TOH
output rise/fall time		20				ns TR/TF
output bit skew		15				ns BS
transient response time		20				ns TTR
overvoltage recovery time		20				ns TOV
<b>FREQUENCY DOMAIN PERFORMANCE<sup>7</sup></b>						
effective bits	f <sub>IN</sub> = 1.0 MHz	9.3				bits EB
SNR – rms signal/rms noise	f <sub>IN</sub> = 1.0 MHz	59	>56	>56	>56	dB SNR
(without harmonics)	f <sub>IN</sub> = 2.0 MHz	56	>53	>53	>53	dB
	f <sub>IN</sub> = 5.0 MHz	52	>49	>49	>49	dB
	f <sub>IN</sub> = 8.0 MHz	47	>44	>44	>44	dB
	f <sub>IN</sub> = 10.0 MHz	43	>40	>40	>40	dB
SNR – rms signal/rms harmonics	f <sub>IN</sub> = 1.0 MHz	61	>58	>58	>58	dB THD
(total harmonic distortion)	f <sub>IN</sub> = 2.0 MHz	59	>56	>56	>56	dB
	f <sub>IN</sub> = 5.0 MHz	55	>52	>52	>52	dB
	f <sub>IN</sub> = 8.0 MHz	46	>43	>43	>43	dB
	f <sub>IN</sub> = 10.0 MHz	44	>41	>41	>41	dB
SINAD – signal-to-noise-and-distortion	f <sub>IN</sub> = 1.0 MHz	58	>55	>55	>55	dB SINAD
(with harmonics)	f <sub>IN</sub> = 2.0 MHz	55	>52	>52	>52	dB
	f <sub>IN</sub> = 5.0 MHz	51	>48	>48	>48	dB
	f <sub>IN</sub> = 8.0 MHz	44	>41	>41	>41	dB
	f <sub>IN</sub> = 10.0 MHz	42	>39	>39	>39	dB
differential phase				<0.5		deg DP
differential gain				<1.0		% DG
full-power bandwidth	(no missing codes)	7.0		>5.0		MHz FPBW
<b>ANALOG INPUT PERFORMANCE</b>						
* top of ladder offset			<25	<25	<25	mV TLO
* bottom of ladder offset			<30	<30	<30	mV BLO
ladder offset temperature coefficient			<10	<10	<10	μV/°C DLO
reference ladder resistance		140	>72	>72	>72	Ω RREF
* reference ladder current <sup>4,5</sup>			<55	<55	<55	mA IREF
reference ladder bandwidth		5				MHz RBW
* analog input resistance <sup>2,3</sup>			>2000	>2000	>2000	Ω RIN
analog input capacitance		105	<130	<130	<130	pF CIN
* analog input bias current <sup>4,5</sup>			<2.0	<2.0	<2.0	mA IBC
<b>DIGITAL INPUTS</b>						
* input voltage, logic LOW <sup>4</sup>			<0.8	<0.8	<0.8	V VIL
* input voltage, logic HIGH <sup>2</sup>			>2.4	>2.4	>2.4	V VIH
* input current, logic LOW (+0.4V) <sup>2,3</sup>			<50	<50	<50	μA IIL
* input current, logic HIGH (+2.4V) <sup>4,5</sup>			<100	<100	<100	μA IIH
* input current, logic Max HIGH (+5.5V) <sup>2,5</sup>			<100	<100	<100	μA IIM
digital input capacitance		6	<15			pF CI
* convert pulse width, LOW <sup>2,5</sup>			>18	>18	>18	ns TPWL
* convert pulse width, HIGH <sup>4,5</sup>			>22	>22	>22	ns TPWH
<b>DIGITAL OUTPUTS</b>						
* output voltage, logic LOW (4.0mA) <sup>3,4</sup>			<0.5	<0.5	<0.5	V VOL
* output voltage, logic HIGH (-400μA) <sup>4,5</sup>			>2.4	>2.4	>2.4	V VOH
* output short circuit current <sup>2,5,8</sup>			<35	<35	<35	mA IOS
<b>POWER REQUIREMENTS</b>						
* positive supply current <sup>2,3</sup>		3.65	<900	<900	<900	mA ICC
* negative supply current <sup>2,3</sup>			<550	<550	<550	mA IEE
nominal power dissipation						W PD

# Recommended Operating Conditions Absolute Maximum Ratings

positive supply voltage (+V <sub>CC</sub> )	+5.0V ±0.25V
negative supply voltage (-V <sub>EE</sub> )	-5.2V ±0.30V
ANALOG to DIGITAL ground differential	0.1V
CONV pulse width HIGH	> 18ns
CONV pulse width LOW	> 22ns
CONV signal rise/fall time	< 40ns
reference ladder top	+2.0V ±0.2V
reference ladder tap (R <sub>M2</sub> )	+1.0V ±0.2V
reference ladder tap (R <sub>M4</sub> )	0.0V ±0.2V
reference ladder tap (R <sub>M6</sub> )	-1.0V ±0.2V
reference ladder bottom	-2.0V ±0.2V
reference ladder differential voltage	4.0V ±0.4V
analog input range	4.0V ±0.4V

positive supply voltage (+V <sub>CC</sub> )	-0.5V to +6.0V
negative supply voltage (-V <sub>EE</sub> )	-6.0 to +0.5V
analog to digital ground differential	1.0V
CONV, NMINV, NLINV voltage range	-0.5V to +5.5V
analog input (V <sub>IN</sub> ) voltage range	-V <sub>EE</sub> to +V <sub>CC</sub>
any reference ladder point to A <sub>GND</sub>	-V <sub>EE</sub> to +V <sub>CC</sub>
sense lead current	1mA
differential ladder voltage (R <sub>T</sub> to R <sub>B</sub> )	-1.0V to +4.4V
forced digital output voltage	-0.5V to +5.5V
forced digital output current	-1.0mA to +6.0mA
output short-circuit current duration	1 sec
power dissipation	see thermal model
junction temperature	+175°C
operating temperature range	
CLC920ACD	0°C to +70°C
CLC920A8D	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10sec

## NOTES:

1. Parameters preceded by an \* are the final electrical test parameters and are 100% tested. A8D units are tested at -55°C, +25°C, and +125°C. AC units are tested only at +25°C, although their performance is guaranteed at 0°C and +70°C as indicated above.

2. +V<sub>CC</sub> = +5.25V.

3. -V<sub>EE</sub> = -5.5V.

4. +V<sub>CC</sub> = +4.75V.

5. -V<sub>EE</sub> = -4.9V.

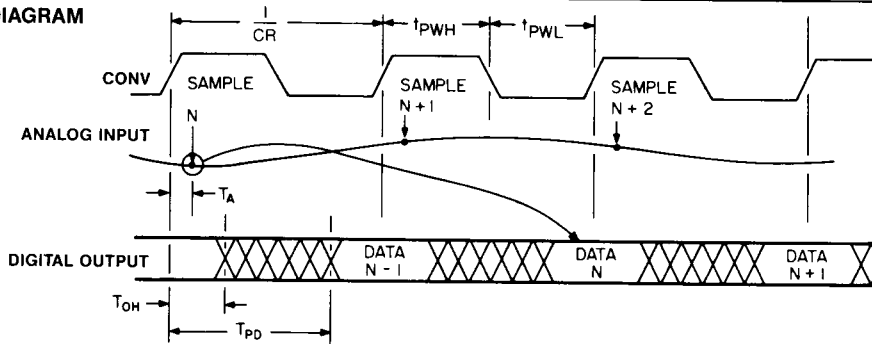
6. R<sub>M2</sub>, R<sub>M4</sub> and R<sub>M6</sub> adjusted.

7. 20MSPS.

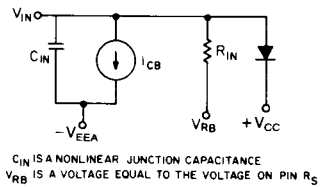
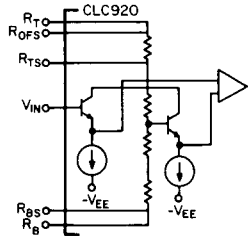
8. One output HIGH to ground 1 sec max.

Comlinear reserves the right to change specifications without notice. Please contact Comlinear for current specifications.

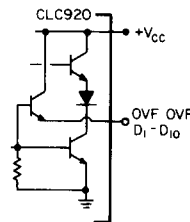
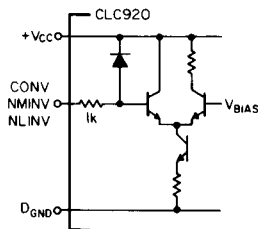
## TIMING DIAGRAM



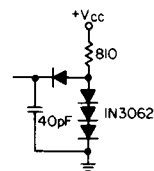
## EQUIVALENT INPUT/OUTPUT CIRCUITS



## INPUT AND REFERENCE LADDER CIRCUITS



## EQUIVALENT INPUT CIRCUIT



CONV, NMINV, AND NLINV INPUT CIRCUIT

OUTPUT STAGE  
9-5

TEST LOAD

## PIN DESCRIPTIONS

$V_{IN}$	The four analog inputs to the CLC920. All four $V_{IN}$ pins should be connected together for proper operation. The normal analog input voltage range is $\pm 2.0V$ .
$R_T, R_B$	$R_T$ is the top (most positive) of the internal reference ladder, and $R_B$ is the bottom (most negative) of the internal reference ladder. $R_T$ is normally adjusted to $+2.0V$ , and $R_B$ is adjusted to $-2.0V$ . Both $R_T$ and $R_B$ should be driven from a low impedance source to insure optimum performance.
$R_{TS}, R_{BS}$	$R_{TS}$ and $R_{BS}$ are the respective sense lines for $R_T$ and $R_B$ . $R_{TS}$ and $R_{BS}$ are not designed to carry greater than 1.0mA, and should be used only in reference driver feedback circuits.
$R_{OFS}$	$R_{OFS}$ is the overflow sense line, which is 1LSB more positive than the $R_{TS}$ sense line. $R_{OFS}$ is not designed to carry greater than 1.0mA, and should be used only in reference driver feedback circuits.
$R_{M1}-R_{M7}$	$R_{M1}-R_{M7}$ are seven equally spaced ladder tap points between $R_T$ , the top of the reference ladder, and $R_B$ , the bottom of the reference ladder. Adjustment of the tap voltages can minimize integral linearity errors. Adjustment of $R_{M2}$ , $R_{M4}$ and $R_{M6}$ is required to maintain the specified 0.1% Integral linearity.

Pin	Function	Normal Value	Correction To 0.1% Linearity
$R_T$	Top of Reference Ladder	+2.000V	+2.000V
$R_{OFS}$	Overflow Sense	+2.000V	+2.000V*
$R_{TS}$	Top of Ladder Sense	+1.996V	+1.996V*
$R_{M1}$	1/8 Scale Tap Line	+1.500V	OPEN**
$R_{M2}$	2/8 Scale Tap Line	+1.000V	+1.000V
$R_{M3}$	3/8 Scale Tap Line	+0.500V	OPEN**
$R_{M4}$	4/8 Scale Tap Line	+0.000V	+0.000V
$R_{M5}$	5/8 Scale Tap Line	-0.500V	OPEN**
$R_{M6}$	6/8 Scale Tap Line	-1.000V	-1.000V
$R_{M7}$	7/8 Scale Tap Line	-1.500V	OPEN**
$R_{BS}$	Bottom of Ladder Sense	-2.000V	-2.000V
$R_B$	Bottom of Reference Ladder	-2.000V	-2.000V

\*Either  $R_{OFS}$  or  $R_{TS}$  should be used, but not both

\*\*Unused ladder tap lines should be *individually* decoupled to ground through 0.1 $\mu$ F capacitors.

CONV	The TTL compatible convert input signal. CONV is rising edge triggered. Dynamic performance can generally be improved by extending the CONV signal LOW period, but the minimum convert HIGH period, listed in the specification table, should not be violated.
$D_1-D_{10}$	$D_1-D_{10}$ are the digital outputs, with $D_1$ being the MSB (Most Significant Bit) and $D_{10}$ being the LSB (Least Significant Bit). The output data is delayed by one clock cycle (this is also termed a "pipeline delay of one cycle"), and is latched by the output register on the rising edge of the CONV pulse. All digital outputs are TTL compatible, and are capable of driving four "LS" type loads.
$\overline{OVF}, \overline{OVF}$	$\overline{OVF}$ and $\overline{OVF}$ are the complementary, overflow output bits. $\overline{OVF}$ will be at logic HIGH for $V_{IN} \geq +2.000V$ . $\overline{OVF}$ and $\overline{OVF}$ are TTL compatible outputs capable of driving four "LS" type loads.
$\overline{NMINV}, \overline{NLINV}$	These two digital inputs determine the specific digital data output format. This is accomplished by presenting the digital output data in either "true" or "inverted" format. $\overline{NMINV}$ controls the logic sense of $D_1$ (MSB), while $\overline{NLINV}$ controls the logic sense of the remaining LSB's, $D_2-D_{10}$ . Both $\overline{NMINV}$ and $\overline{NLINV}$ are TTL compatible inputs.

Input	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	$\overline{NMINV} - 1$ $\overline{NLINV} - 1$	$\overline{NMINV} - 0$ $\overline{NLINV} - 0$	$\overline{NMINV} - 0$ $\overline{NLINV} - 1$	$\overline{NMINV} - 1$ $\overline{NLINV} - 0$
$>2.000V$	msb - lsb (ovf) 000000000(1)	111111111(1)	100000000(1)	011111111(1)
2.000V	000000000(0)	111111111(0)	100000000(0)	011111111(0)
1.996V	000000001(0)	111111110(0)	100000001(0)	011111110(0)
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
0.004V	011111111(0)	100000000(0)	111111111(0)	000000000(0)
0.000V	100000000(0)	011111111(0)	000000000(0)	111111111(0)
-0.004V	100000001(0)	011111110(0)	000000001(0)	111111110(0)
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
-1.996V	111111110(0)	000000001(0)	011111110(0)	100000001(0)
-2.000V	111111111(0)	000000000(0)	011111111(0)	100000000(0)

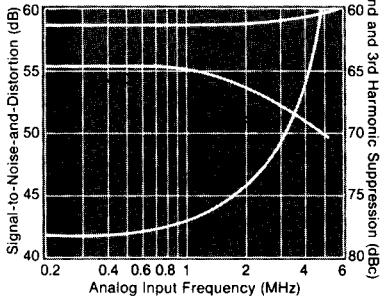
Note: Input voltages are at code centers.

$+V_{CC}$	Positive supply voltage, nominally +5.0V. All $+V_{CC}$ Pins must be used for proper operation. $+V_{CC}$ is primarily a digital supply, and should be referenced to $D_{GND}$ . Each $+V_{CC}$ pin should be decoupled to $D_{GND}$ through 0.1 $\mu$ F capacitors at a minimum.
$-V_{EE}$	Negative supply voltage, normally -5.2V. All $-V_{EE}$ pins must be used for proper operating. $-V_{EE}$ is primarily an analog supply, and should be referenced to $A_{GND}$ . Each $-V_{EE}$ pin should be decoupled to $A_{GND}$ through 0.1 $\mu$ F capacitors at a minimum.
$A_{GND}, D_{GND}$	$A_{GND}$ and $D_{GND}$ are the respective analog and digital ground returns. Optimum noise immunity is maintained by referencing the positive supply voltage ( $+V_{CC}$ ) to the digital ground ( $D_{GND}$ ), and by referencing the negative supply voltage ( $-V_{EE}$ ) to the analog ground ( $A_{GND}$ ). Dynamic performance may benefit from separate ground plane areas for the digital and analog circuits, with a single point connection at the CLC920.
NC	These pins are not internally connected, and should be grounded under normal circumstances for optimum noise performance.

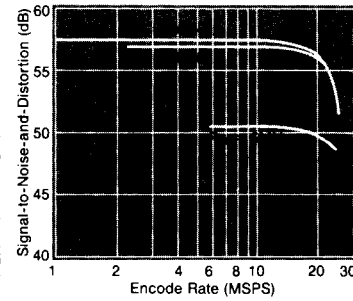


# Typical Performance Characteristics $T_A = +25^\circ\text{C}$ , $V_{\text{REF}} = \pm 2.000\text{V}$ unless otherwise stated

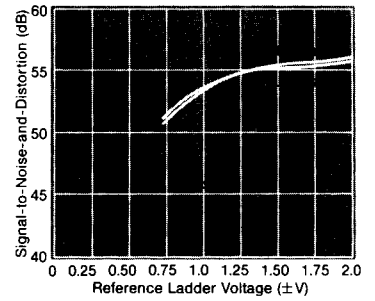
**SINAD and Harmonics vs Analog Input Frequency**



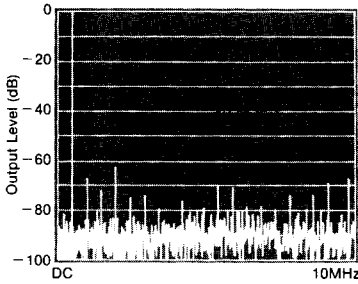
**SINAD vs Encode Rate**



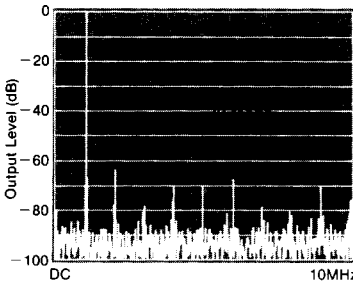
**Signal-to-Noise-and-Distortion vs Reference Voltage**



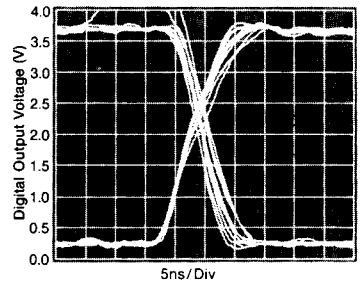
**500kHz Output Spectrum**



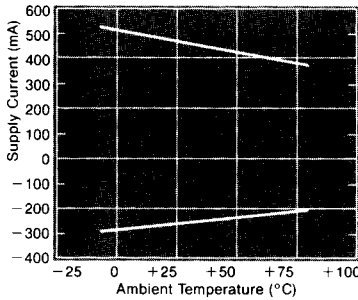
**1.0MHz Output Spectrum**



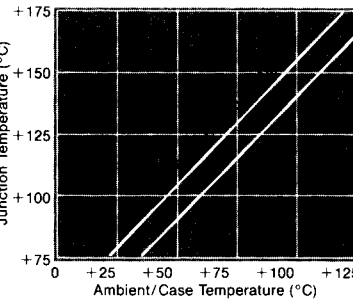
**Output Bit Skew**



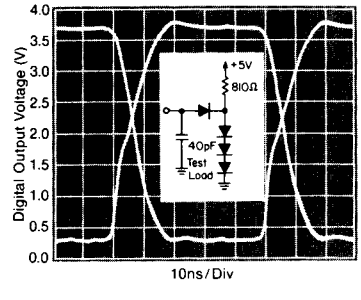
**Supply Current vs Ambient Temperature**



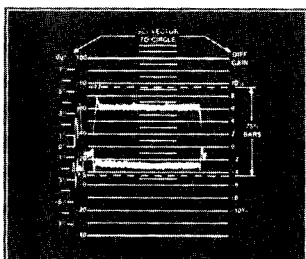
**Junction Temperature vs Ambient & Case Temperatures**



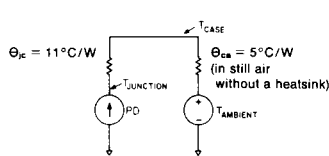
**Digital Output Transitions**



**15MSPS NTSC Modulated Ramp Input**



**Thermal Model**



$$PD = |I_{CC}| V_{CC} + |I_{EE}| V_{EE}$$

$$\Theta_{ca} = \Theta_{cs} + \Theta_{sa} \text{ (with heatsink)}$$

Where  $\Theta_{sa}$  = Heatsink-to-ambient ( $^\circ\text{C}/\text{W}$ );  
 $\Theta_{cs}$  = Case-to-Heatsink ( $^\circ\text{C}/\text{W}$ )  
 and usually  $\Theta_{sa} \gg \Theta_{cs}$ , therefore  $\Theta_{ca}$  (with heatsink)  $\approx \Theta_{sa}$   
 (Thermalloy 2286 or 6088B)

$$T_{\text{JUNCTION}} = T_{\text{AMBIENT}} + (\Theta_{JC} + \Theta_{CA}) PD = T_{\text{AMBIENT}} + (\Theta_{JA}) PD$$

where  $\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$

or

$$T_{\text{JUNCTION}} = T_{\text{CASE}} + (\Theta_{JC}) PD,$$

where in either case  $T_{\text{JUNCTION}} \leq T_{\text{JUNCTION}} (\text{MAX})$

## INSIDE THE CLC920

The CLC920 is a 10-bit parallel flash converter. The 1024 internal comparators determine the exact level of the analog input signal relative to 1024 separate tap points on a resistor ladder/divider. The subsequent digital decoding section converts the comparator outputs into a more useful binary format. The 25 Mega-sample per second encode rate and wide analog input bandwidth necessitate careful design choices and a clear understanding of flash converter operation.

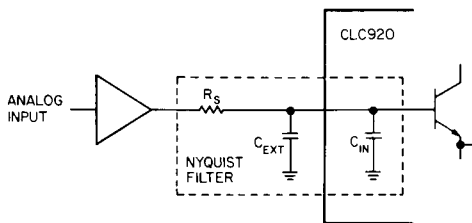
The 1024 input comparators of the CLC920 are latched on the rising edge of the CONV signal. The latched output of the comparators is then decoded and will be latched into the output registers on the rising edge of the *next* CONV signal. In other words, the output data is delayed by one clock cycle, plus the output propagation delay ( $t_{pd}$ ), from the actual conversion event. Overall performance will generally be improved if the CONV signal duty cycle is adjusted to provide as much time in the LOW state as is possible without violating the convert pulse width requirements (see "Recommended Operating Conditions").

The actual digital data outputs are capable of driving four "LS" type TTL loads each. The specific digital data output format can be set to straight binary or 2's complement, in either "true" or "inverted" form (for a total of four options). The output format is determined by the settings of the NMINV and NLINV controls (see Pin Descriptions).

## INPUT BUFFERS AND FILTERING

The most important aspect of analog-to-digital conversion is supplying the converter a high-quality analog input signal with a minimum of distortion. Often this requires an input buffer/amplifier to provide sufficient drive current, voltage gain, and impedance matching. The CLC231 is one amplifier choice which will provide sufficient output current to drive the 105pF input capacitance of the CLC920. Additionally, the CLC231 can be used to amplify low-level input signals, to match the  $\pm 2V$  analog input range of the CLC920.

Analog input frequency components greater than one-half the encode rate (the Nyquist frequency) will show up as low frequency terms in the digital output data; this is known as "aliasing." These false terms can be eliminated through low pass filtering of the converter input signal. A simple RC low pass should work well (note that the CLC920 input capacitance parallels the filter capacitance, and should be considered). Multi-Pole filters will provide more effective cutoff performance, and should be strongly considered in cases where the signal energy above "Nyquist" is high.



## INTERNAL REFERENCE LADDER

Both the top and bottom reference inputs ( $R_T$  and  $R_B$ ) should be driven from a low impedance source. Three ladder sense

lines are provided to allow the reference ladder voltages to be very precisely adjusted. The sense lines are intended to be used only as part of a feedback circuit and should not carry more than 1.0mA.

Seven reference tap points are provided at 1/8 scale intervals. Voltage adjustments of the "mid-point" reference ladder taps can be used to improve integral linearity. This is accomplished by minimizing the difference between the actual and ideal internal reference ladder tap voltages. The specified 0.1% linearity requires the adjustment of  $R_{M2}$ ,  $R_{M4}$ , and  $R_{M6}$ . Additional linearity improvements are possible with the adjustment of  $R_{M1}$ ,  $R_{M3}$ ,  $R_{M5}$  and  $R_{M7}$ . A crude alignment technique involves adjusting a specific reference tap voltage such that the CLC920 output data accurately reflects the analog input level (see Typical Interface Circuit for alignment procedure).

Under normal circumstances the reference ladder top and bottom,  $R_T$  and  $R_B$ , as well as the ladder tap points  $R_{M1}$ – $R_{M7}$ , should be decoupled to analog ground ( $A_{GND}$ ) through 0.1 $\mu$ F capacitors. Certain applications may require a variable reference ladder potential. The reference ladder voltage can be varied at up to 5MHz with less than 3dB of degradation, but it should be noted that dynamic performance may suffer if the differential ladder potential is other than 4.0V ( $V_{RT}$ – $V_{RB}$ ).

## VOLTAGE SUPPLIES

The CLC920 requires two voltage supplies, a +5.0V supply which is primarily digital, and a –5.2V supply which is primarily analog. In operation, the maximum supply current level occurs at the colder temperatures. The guaranteed performance listed in the specifications table assumes  $T_{AMBIENT} = T_{CASE} = T_{JUNCTION}$ , which is a worst case condition for 0°C or –55°C supply currents as appropriate. After a short stabilization and warm-up period, the supply currents will drop approximately 14%. At the high temperature extreme, the CLC920 is designed to operate at +70°C ambient temperature in still air without a heatsink. See "thermal model" for operation above +70°C.

## LAYOUT CONSIDERATIONS

High performance data conversion components require an extra measure of care to insure optimum performance. One of the most important aspects of CLC920 performance is the use of a substantial ground plane around and under the converter. Separate ground plane areas for the digital and analog circuit elements can help to keep digital switching noise off of the sensitive analog signal and reference lines. If separate ground planes are used, they should be connected together near the CLC920.

The next major area of interest are the voltage supplies. Effective decoupling of the supply lines near the device pins is essential to the CLC920's performance. DC supply variations of  $\pm 15\%$  should have a minimal effect on converter operation; supply ripple, however, can seriously undermine dynamic performance. Generally, 0.1 $\mu$ F capacitors from each supply pin to ground (+ $V_{CC}$  to  $D_{GND}$ , and – $V_{EE}$  to  $A_{GND}$ ) should provide satisfactory results. Chip capacitors are preferred because of their inherently lower lead inductance.

Sockets increase lead inductance and capacitance; consequently, the use of sockets, for the CLC920 or its analog input buffer, is not advised. If sockets must be used, low profile teflon types or "pin" sockets are the preferred types.

## TYPICAL INTERFACE CIRCUIT

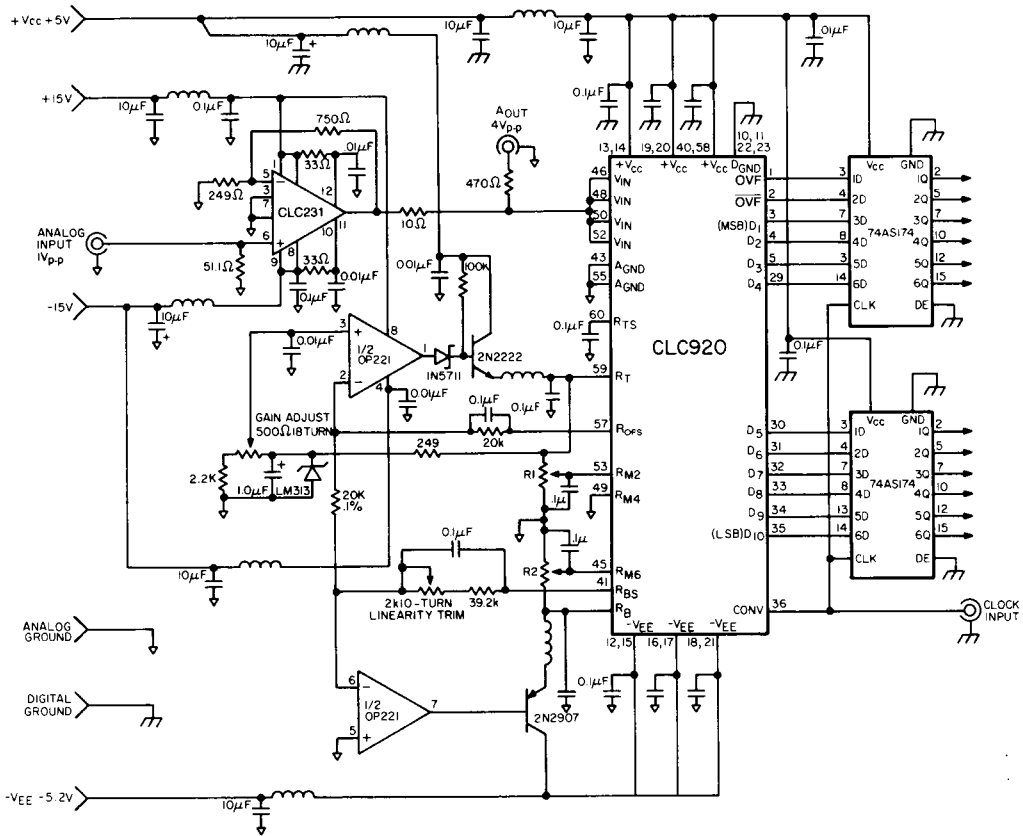
The CLC920 evaluation circuit incorporates both reference driver circuitry and an analog signal input buffer. Special care has been exercised to separate analog and digital supplies through the extensive use of decoupling capacitors and series inductors in the supply lines. The self-tracking reference driver insures high-quality performance with a minimum of initial adjustment.

The calibration procedure involves first setting the  $R_{ofs}$  voltage to  $+2.000V$  by adjusting the "Gain" potentiometer.

The second adjustment is to the  $R_{BS}$  voltage, which should be at  $-2.000V$ , with the "Linearity" trim.

A crude Integral Linearity Adjustment can be made by first setting the  $V_{IN}$  voltage to  $+1.000V$ .  $R_1$  is then adjusted until the digital output is equal to  $MSB01\ 0000\ 0000_{LSB}$ .  $V_{IN}$  is then changed to  $-1.000V$  and  $R_2$  is adjusted until the digital output is equal to  $MSB11\ 0000\ 0000_{LSB}$ . Since these adjustments can be interactive, it may prove useful to repeat the entire calibration procedure (including top and bottom of ladder adjustments) as a self check.

INDUCTORS = FERROXCUBE #VK20019/4B



## PACKAGE OUTLINE DIMENSIONS

INCHES, (MM)

