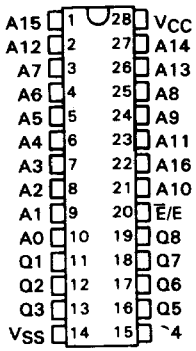
TMS47C1024
131,072-WORD BY 8-BIT READ-ONLY MEMORY

NOVEMBER 1985

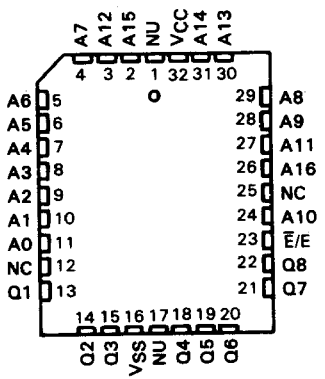
- **131,072 X 8 Organization**
- **Fully Static (No Clocks, No Refresh)**
- **All Inputs and Outputs TTL and CMOS Compatible**
- **Single 5-V Power Supply**
- **Standby Mode for Minimum Power Usage**
- **Maximum Access Time from Address or Power Down**

TMS47C1024-20	**200 ns**
TMS47C1024-25	**250 ns**
TMS47C1024-30	**300 ns**

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C1024 is a 1,048,576-bit read-only memory organized as 131,072 words of 8-bit length. This makes the TMS47C1024 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C1024 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chip-enable/power-down pin is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-enable/power-down pin.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$/E	Chip Enable/Power Down
NC	No Connection
NU	Make No Internal Connection
Q1-Q8	Data Out
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A16)

The address-valid interval determines the device cycle time. The 17-bit positive-logic address is decoded on-chip to select one of 131,072 words of 8-bit length in the memory array. A0 is the least-significant bit and A16 is the most-significant bit of the word address.

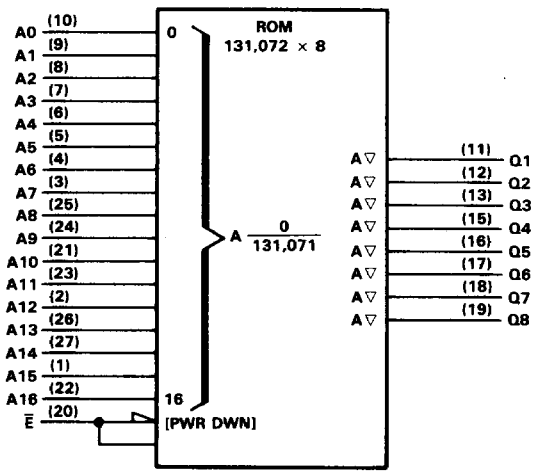
chip-enable/power down ($\overline{E}$ or E)

The chip-enable/power-down pin can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on the chip-enable/power-down pin is active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state and the device goes into a standby current mode.

data out (Q1-Q8)

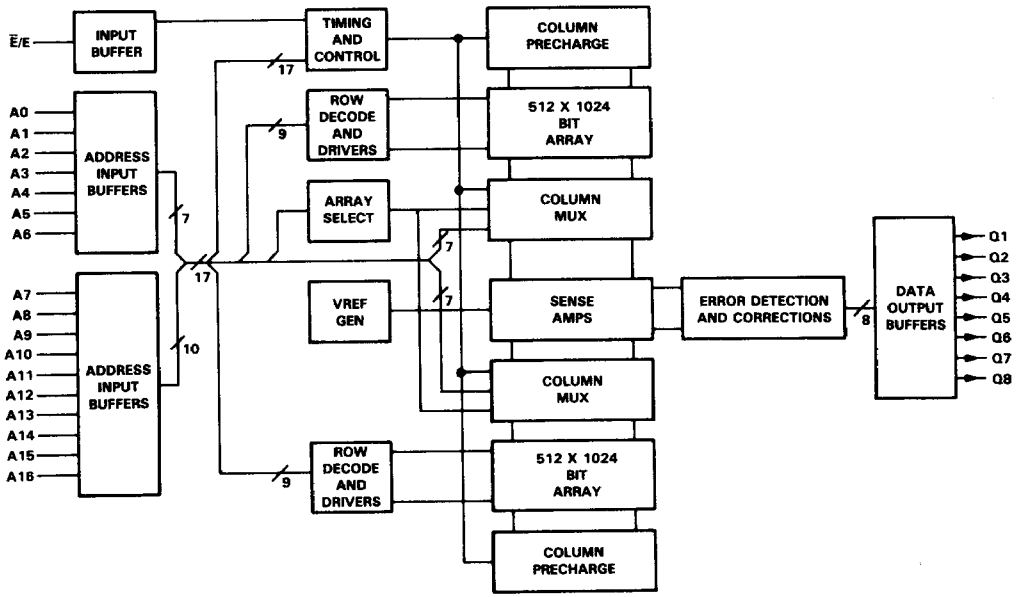
The eight outputs must be enabled by the chip-enable/power-down pin before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package. Pin 20 can be active low as shown in the symbol above or active high.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . T.B.D.
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input leakage current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		±10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		T.B.D.	
I_{CC2}	Supply current from V_{CC} (standby)	V_{CC} = 5.5 V			T.B.D.	
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		15	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS47C1024-20		TMS47C1024-25		TMS47C1024-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		300	ns
$t_{a(E)}$	Access time from chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

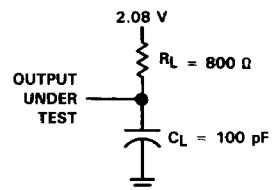
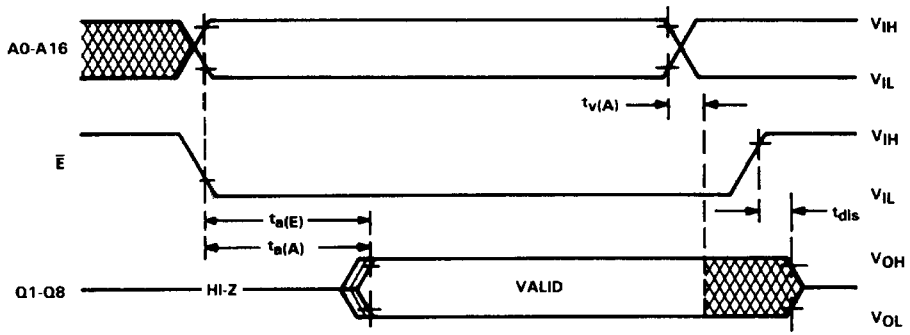


FIGURE 1. LOAD CIRCUIT

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C1024 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 131,072 8-bit words with address locations numbered 0 to 131,071. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A16 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, 512K, or 1024K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____ SURFACE MOUNT (FM)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW

N PACKAGE: PIN 20: _____
PLCC: PIN 23 _____