

# 93427

## ISOPLANAR SCHOTTKY TTL MEMORY

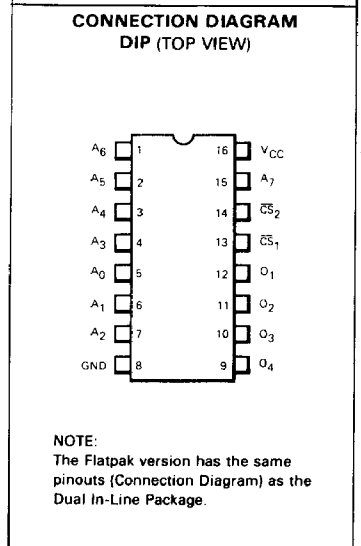
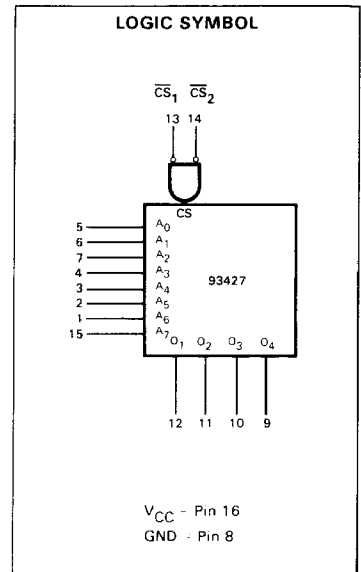
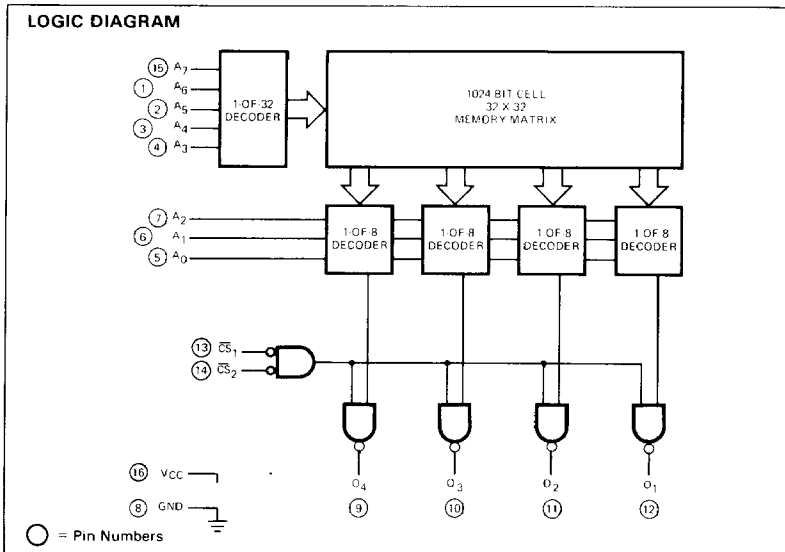
### 256×4-BIT PROGRAMMABLE READ ONLY MEMORY

**DESCRIPTION** - The 93427 is a fully decoded high-speed 1024-bit field Programmable ROM organized 256 words by four bits per word. The 93427 has 3-state outputs. The outputs are disabled when either  $\overline{CS}_1$  or  $\overline{CS}_2$  are in the HIGH state. The 93427 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZED 256 X 4 BITS PER WORD
- 3-STATE OUTPUTS
- FULLY DECODED - ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 16-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS - FOR HIGH RELIABILITY

**PIN NAMES**

- $A_0 - A_7$       Address Inputs
- $\overline{CS}_1, \overline{CS}_2$     Chip Select Inputs
- $O_1 - O_4$       Data Outputs



# FAIRCHILD ISOPLANAR SCHOTTKY TTL MEMORY • 93427

**FUNCTIONAL DESCRIPTION** – The 93427 is a bipolar field Programmable Read Only Memory (PROM) organized 256 words by four bits per word. The 93427 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects are active LOW; conversely, a HIGH (logic "1") on the  $\overline{CS}_1$  or  $\overline{CS}_2$  will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the  $A_0$  through  $A_7$  inputs, the chip is selected, and data is valid at the outputs after  $t_{AA}$  nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

**PROGRAMMING** – The 93427 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 6, page 6-14.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
$V_{CC}$	–0.5 V to +7.0 V
Input Voltages	–0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	–0.5 V to +5.5 V

## GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE ( $V_{CC}$ )			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93427XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93427XM	4.50 V	5.0 V	5.50 V	–55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

**DC CHARACTERISTICS:** Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
$V_{OL}$	Output LOW Voltage		0.30	0.45	V	$V_{CC} = \text{MIN}$ , $I_{OL} = 16 \text{ mA}$ , $A_0 = +10.8 \text{ V}$ $A_1$ through $A_7 = \text{HIGH}$
$V_{OH}$	Output HIGH Voltage	2.4			V	$V_{CC} = \text{MIN}$ , $I_{OH} = -2.0 \text{ mA}$
$I_{off}$	Output Leakage Current for HIGH Impedance State			50 –50	$\mu\text{A}$ $\mu\text{A}$	$V_{OH} = 2.4 \text{ V}$ $V_{OL} = 0.4 \text{ V}$ 0°C to +75°C
$I_{off}$	Output Leakage Current for HIGH Impedance State			100 –50	$\mu\text{A}$ $\mu\text{A}$	$V_{OH} = 2.4 \text{ V}$ $V_{OL} = 0.4 \text{ V}$ –55°C to +125°C
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$I_F$	Input LOW Current					
	$I_{FA}$ (Address Inputs) $I_{FCS}$ (Chip Select Inputs)		–160 –160	–250 –250	$\mu\text{A}$ $\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_F = 0.45 \text{ V}$
$I_R$	Input HIGH Current					
	$I_{RA}$ (Address Inputs) $I_{RCS}$ (Chip Select Input)			40 40	$\mu\text{A}$ $\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_R = 2.4 \text{ V}$
$I_{CC}$	Power Supply Current		85	110	mA	$V_{CC} = \text{MAX}$ , Outputs open Inputs Grounded and Chip Selected
$C_O$	Output Capacitance		7		pF	$V_{CC} = 5.0 \text{ V}$ , $V_O = 4.0 \text{ V}$ , $f = 1.0 \text{ MHz}$
$C_{IN}$	Input Capacitance		4		pF	$V_{CC} = 5.0 \text{ V}$ , $V_O = 4.0 \text{ V}$ , $f = 1.0 \text{ MHz}$
$V_C$	Input Clamp Diode Voltage			–1.2	V	$V_{CC} = \text{MIN}$ , $I_A = -18 \text{ mA}$

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**AC CHARACTERISTICS:**  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 5\%$ .

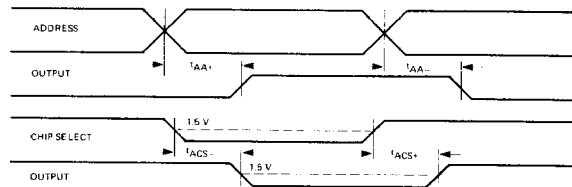
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
$t_{AA-}$	Address to Output Access Time		25	45	ns	See Figure 1
$t_{AA+}$			25	45		
$t_{ACS-}$	Chip Select Access Time		12	20	ns	
$t_{ACS+}$			12	20		

**AC CHARACTERISTICS:**  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ .

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
$t_{AA-}$	Address to Output Access Time		25	60	ns	See Figure 1
$t_{AA+}$			25	60		
$t_{ACS-}$	Chip Select Access Time		12	30	ns	
$t_{ACS+}$			12	30		

Note 1: Typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $+25^\circ\text{C}$  and max loading.

## AC WAVEFORMS



## AC TEST OUTPUT LOAD

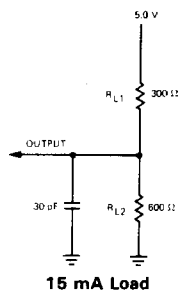


Fig. 1