CMOS OCTAL COUNTER/DIVIDER

FEATURES

- Eight Decoded Outputs
- Direct Reset
- Trigger from either Edge of Clock Input
- Carry Output for Cascading Stages
- Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The 4022 B consists of a 4-stage Johnson Divide-by-8 Counter and an Output Decoder. Inputs include Clock, Reset, and Clock Enable signals.

The counter has interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. A high Reset signal clears the counter to its zero count.

Use of the Johnson divide-by-eight counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A Carry-out (C_{OUT}) signal completes one cycle every 8 clock input cycles and is used to directly clock the succeeding counter in multi-stage applications.

This part can be used in frequency division circuits as well as octal counter or octal decode display applications.

FUNCTIONAL TRUTH TABLE

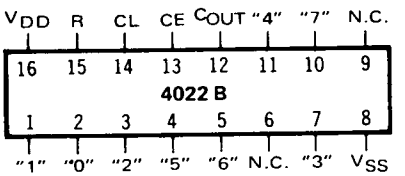
(Positive Logic)

Clock	Clock Enable	Reset	Output = n
0	X	0	n
X	1	0	n
⌐	0	0	n + 1
¬	X	0	n
1	⌐	0	n + 1
X	¬	0	n
X	X	1	"0"

X Don't Care If n < 4 Carry = 1, otherwise = 0

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

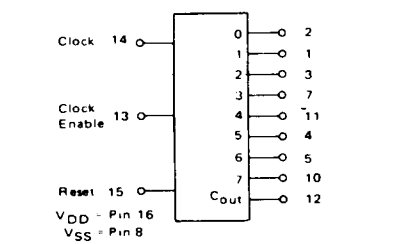
C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

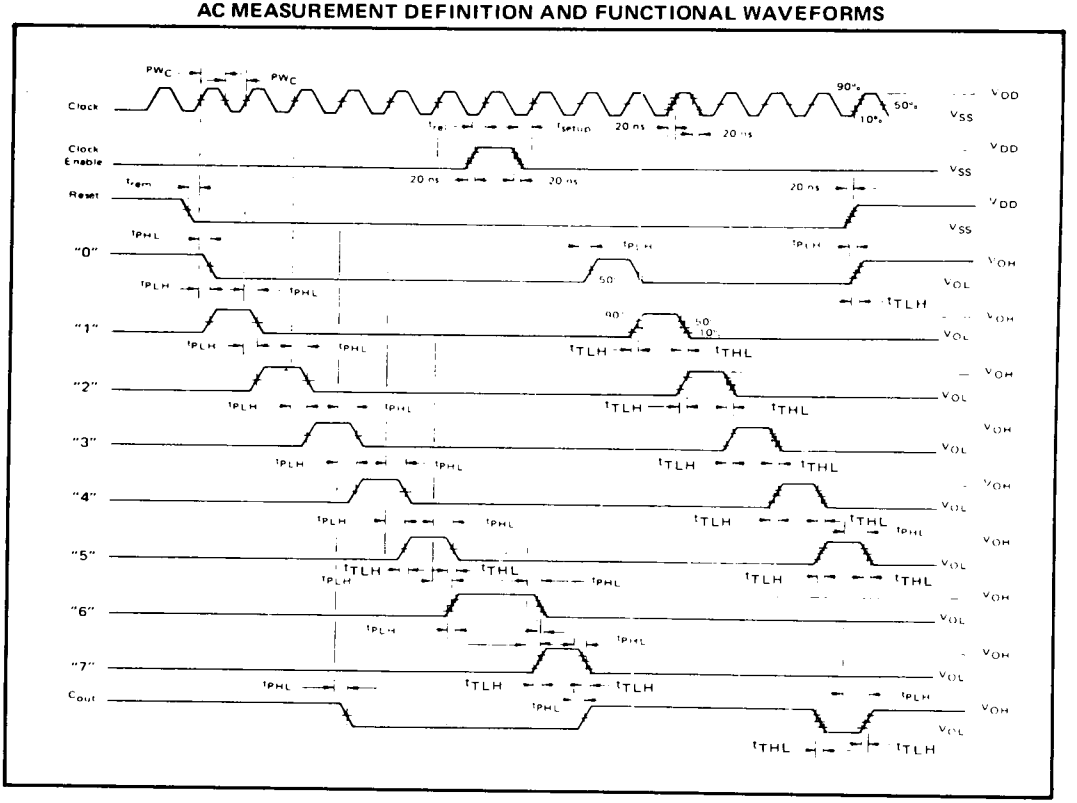
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

ELECTRICAL CHARACTERISTICS (Continued)

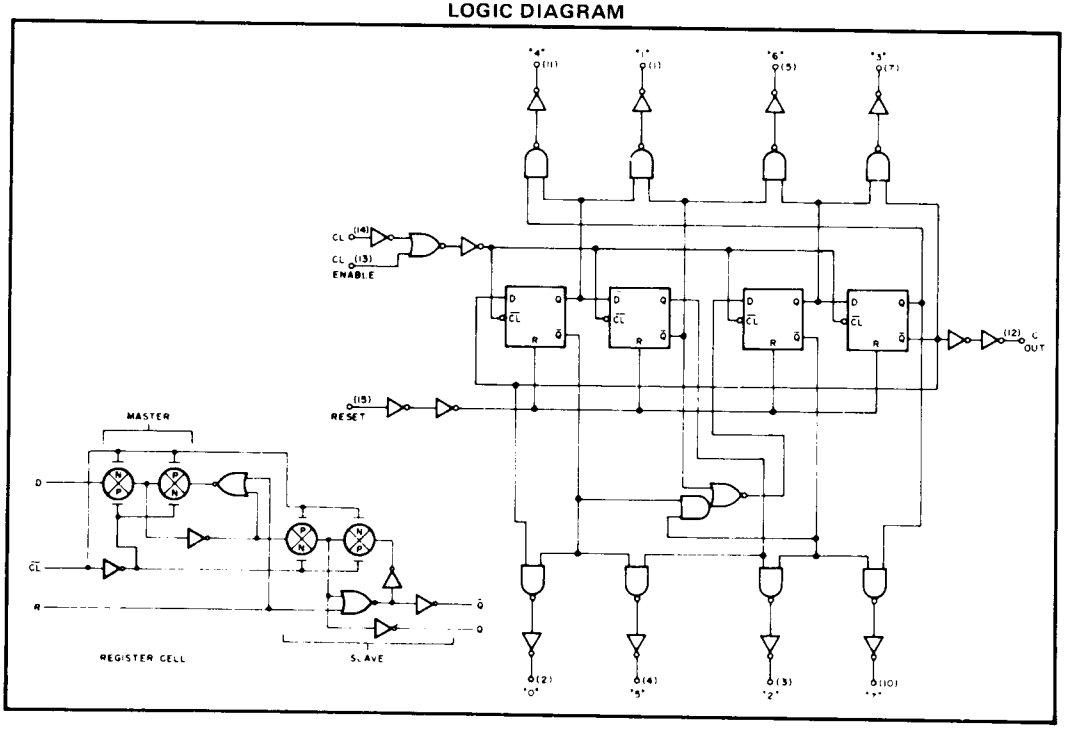
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	600	1200	ns
To Decoded Outputs		10	–	240	480	
		15	–	180	360	
	t_{PLH}, t_{PHL}	5	–	500	1000	ns
To Carry Output		10	–	200	400	
		15	–	150	300	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	250	500	ns
Decoded Outputs		10	–	125	250	
		15	–	90	180	
	t_{TLH}, t_{THL}	5	–	180	360	ns
Carry Output		10	–	90	180	
		15	–	65	130	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	200	400	ns
		10	—	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	5	–	–	
MINIMUM ENABLE SETUP TIME	t_{setup}	5	–	175	350	ns
		10	–	75	150	
		15	–	55	110	
MINIMUM ENABLE REMOVAL TIME	t_{rem}	5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	500	1000	ns
To Decoded Outputs		10	–	200	400	
		15	–	140	280	
	t_{PLH}	5	–	400	800	ns
To Carry Output		10	–	150	300	
		15	–	110	220	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	150	300	ns
		10	–	75	150	
		15	–	60	120	
RESET REMOVAL TIME	t_{rem}	5	–	250	500	ns
		10	–	100	200	
		15	–	80	160	

AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



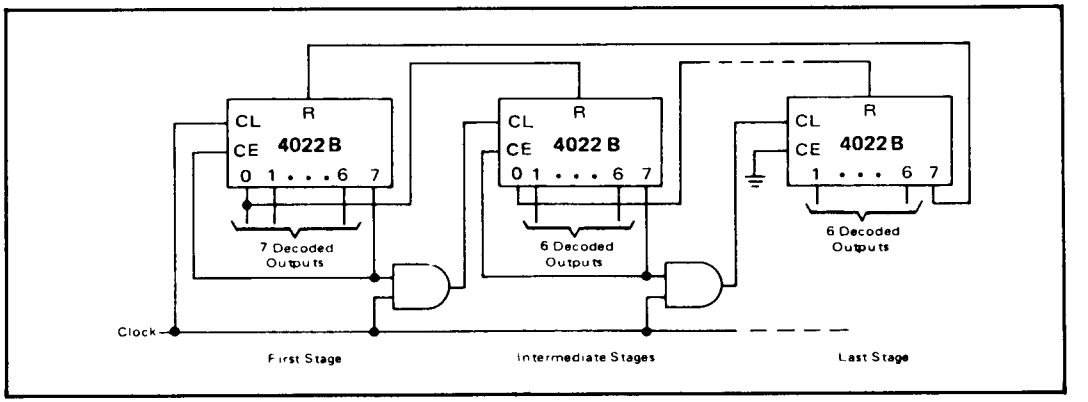
LOGIC DIAGRAM



APPLICATIONS INFORMATION

COUNTER EXPANSION

This figure shows a technique for extending the number of decoded output states for the 4022 B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



DIVIDE-BY-N-COUNTER

When the Nth decoded output is reached (Nth clock pulse) the S-R flip-flop (constructed from the 4001B) generates a reset pulse which clears the 4022B to its zero count. At this time, if the Nth decoded output is greater than or equal to 4, the C_{OUT} line goes high to clock the next counter section. The "0" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "0" output "high" resets the S-R flip-flop to enable the 4022B.

If the Nth decoded output is less than 4, the C_{OUT} line will not go high, and, therefore, cannot be used. In this case, the "0" decoded output may be used to perform the clock function for the next counter.