PACE1753/SOS
SINGLE CHIP, MIL-STD-1750A MEMORY MANAGEMENT UNIT (MMU) CMOS/SOS SPACE PROCESSOR MICROPERIPHERAL

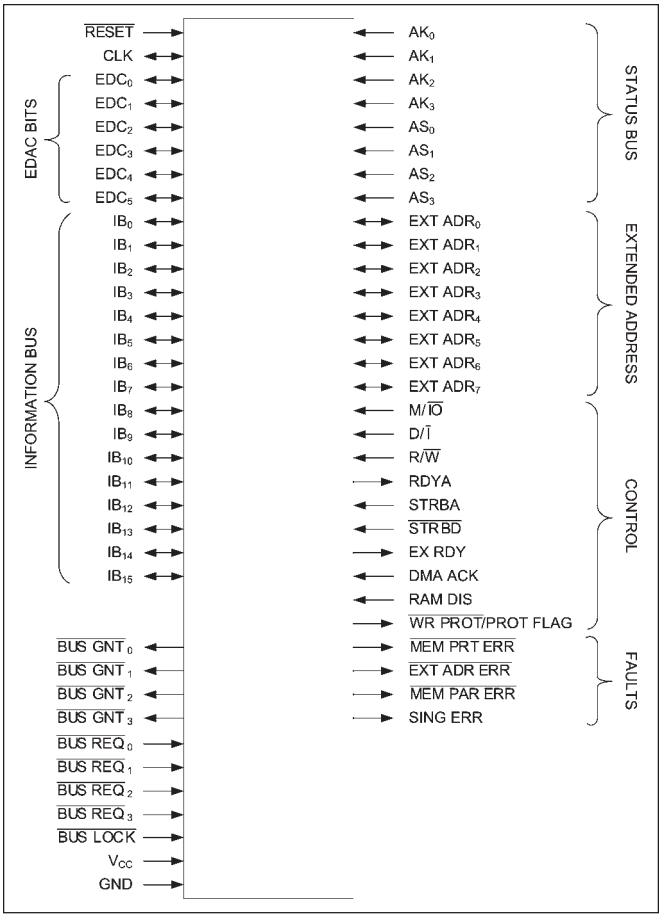
FEATURES

- **Implements the MIL-STD-1750A Instruction Set Architecture for Memory Management and Protection of up to 1 Megaword. All mapping memory (10,240 bits) for both the MMU and BPU functions are included on the chip.**
- **Designed to interface memory to the PACE1750A/AE.**
- **Provides the following additional functions:**
  - **— EDAC, Error Detection and Correction—or parity generation and detection**
  - **— Correct data register—for diagnostics**
  - **— First memory failing address register**
  - **— Illegal address error detection—programmable**
  - **— Multi-Master arbitration**
- **8-bit extended address laches and drivers on chip.**
- **20, 25 and 30 MHz operation over the Military Temperature Range**
- **Single 5V ± 10% Power Supply**
- **Available with Class S manufacturing, screening, and testing.**
- **SOS Insulated substrate latch-up immunity and excellent SEU tolerance.**
- **SOS devices are fully interchangeable with application-proven SMD CMOS P1753 devices.**
- **Available in:**
  - **— 68-Lead Quad Pack (Leaded Chip Carrier) with optional Gull Wing.**

MEMORY MANAGEMENT UNIT AND BLOCK PROTECT UNIT "COMBO" (PACE1753)—FUNCTIONAL DESCRIPTION

The PACE1753 (COMBO) is a support chip for the PACE1750A/AE microprocessor family. It provides the following supporting functions to the system:

1. Memory management and access protection for up to 1M words.
2. Physical memory write protection for up to 1M words memory in pages of 1K words each. Separate protection is provided for the CPU and for DMA in systems which include DMA.
3. Detection of illegal I/O accesses (as defined by MIL-STD-1750A) or access to an unimplemented block of memory. In each case an error flag is generated to the processor.
4. Detection of double errors on the data bus and correction of single errors. An error signal is generated to the processor when a multiple error is detected.
5. RDYA generation. Up to three wait states can be inserted in the address phase of the bus by generating a not-ready, RDYA low signal. The number of wait states required can be programmed in an internal register in the COMBO.
6. Bus arbitration for up to 4 masters. Arbitration is done on a fixed priority basis (i.e. by interconnection of hardware). (In 68 pin package only).



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage Range	0.5V to +7.0V
Input Voltage Range	0.5V to V_{CC} + 0.5V
Storage Temperature Range	–65°C to +150°C
Input Current Range	–30mA to +5mA
Current applied to any output[3]	150mA
Maximum Power Dissipation[2]	1.5W
Lead Temperature Range (soldering 10 seconds)	300°C
Thermal resistance (θ_{JC}): QL and QG packages	8°C/W

Notes

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Must withstand the added power dissipation due to short circuit test e.g., I_{OS}.
3. Duration 1 second or less.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	4.5V to +5.5V
Case Operating Temperature Range	–55°C to +125°C
Operating Maximum Power Dissipation (Outputs Open)	
Device Type 20MHz	0.5W
Device Type 30MHz	0.6W
Device Type 40MHz	0.7W

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Conditions[1]	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage[2]	–0.5	0.8	V		
V_{CD}	Input Clamp Diode Voltage		–1.2	V	V_{CC} = 4.5V, I_{IN} = –18mA	
V_{OH}	Output HIGH Voltage	2.4		V	V_{CC} = 4.5V,	I_{OH} = –8.0mA
		V_{CC} – 0.2		V	V_{IN} = 0.8V, 2.0V	I_{OH} = –300µA
V_{OL}	Output LOW Voltage,[4] except EXT ADR_0 – EXT ADR_7		0.65	V	V_{CC} = 4.5V,	I_{OL} = 8.0mA
			0.2	V	V_{IN} = 0.8V, 2.0V	I_{OL} = 300µA
V_{OL}	Output LOW Voltage,[4] EXT ADR_0 – EXT ADR_7		0.65	V	V_{CC} = 4.5V,	I_{OL} = 20.0mA
			0.2	V	V_{IN} = 0.8V, 2.0V	I_{OL} = 300µA
I_{IH}	Input HIGH Current, except IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		300	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IH}	Input HIGH Current, IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		100	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IL}	Input LOW Current, except IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		–50	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{IL}	Input LOW Current, IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		–50	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{OZH}	Output Three-State Current		50	µA	V_{OUT} = 2.4V, V_{CC} = 5.5V	
I_{OZL}	Output Three-State Current		–50	µA	V_{OUT} = 0.5V, V_{CC} = 5.5V	
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels, Active)		60	mA	V_{IN} < 0.2V or < V_{CC} – 0.2V f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels, Active)		110	mA	V_{IN} = 3.4V, f = 0MHz, All Inputs, Outputs Open, V_{CC} = 5.5V	
I_{CCD}	Dynamic Power Supply Current		90	mA	V_{CC} = 0V to V_{CC}, tr = tf = 2.5 ns, Outputs Open, V_{CC} = 5.5V	F = 20MHz
			100	mA		F = 30MHz
			125	mA		F = 40MHz
I_{OS}	Output Short Circuit Current[3]	–25		mA	V_{OUT} = GND, V_{CC} = 5.5V	
C_{IN}	Input Capacitance		10	pF	Inputs Only	
C_{OUT}	Output/Bi-directional Capacitance		15	pF	Outputs Only (Including I/O Buffers)	

Notes

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.
4. Test may be performed by setting/forcing the parameter limit (voltage) and measuring the appropriate current parameter.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V)

Symbol	Parameter	20 MHz		25MHz		30 MHz		Unit
		Min	Max	Min	Max	Min	Max	
TD/$\overline{I}$ (EXT ADR)$_V$	MMU Cache Hit		27		23		21	ns
T$\overline{STRBD}$ ($\overline{EXT\ ADR\ ERR}$)$_L$	External Address Error		37		33		30	ns
TC (IBD CORR)	Error Correction Read Cycle		32		28		26	ns
IBD$_V$ (SING ERR)$_H$	Error Correction Read Cycle		37		33		31	ns
TC (SING ERR)$_L$	Error Correction Read Cycle		27		23		21	ns
TIBD$_V$ (EDC GEN)$_V$	EDAC or Parity Write Cycle		32		28		26	ns
TSTRBD (EX RDY)$_L$	MMU Cache Miss		27		23		21	ns
TC (EX RDY)$_H$	MMU Cache Miss		27		23		21	ns
TC ($\overline{WR\ PROT}$)$_L$	MMU Cache Miss		36		32		30	ns
T$\overline{STRBD}_H$ ($\overline{WR\ PROT}$)$_H$	MMU Cache Miss		27		23		21	ns
TC ($\overline{GNT1}$)$_H$	Arbiter LOW to HIGH Priority		34		30		28	ns
TC ($\overline{GNT0}$)$_L$	Arbiter LOW to HIGH Priority		34		30		28	ns
TC ($\overline{GNT0}$)$_H$	Arbiter HIGH to LOW Priority		34		30		28	ns
TC ($\overline{GNT1}$)$_L$	Arbiter HIGH to LOW Priority		34		30		28	ns
TC (RDYA)	Address Ready		32		28		26	ns
TFC (IB OUT)$_V$	Clock to IB Out Valid (I/O Read)		40		38		36	ns
TIBD$_{IN}$ ($\overline{MEM\ PAR\ ERR}$)	Parity Mode		36		32		30	ns
TC ($\overline{MEM\ PRT\ ERR}$)	Memory Protect Error		64		60		58	ns
T$\overline{STRBD}$ ($\overline{WR\ PROT}$)	Write Protect Cache Hit		27		23		21	ns
TC ($\overline{WR\ PROT}$)$_L$	Write Protect Cache Miss		37		33		31	ns
T$\overline{STRBD}_H$ ($\overline{WR\ PROT}$)$_H$	Write Protect Cache Miss		27		23		21	ns
TD/$\overline{I}$ (PROT FLAG)	Cache Hit (BPU Protection Error)		52		48		46	ns
TD/$\overline{I}$ (PROT FLAG)	Cache Hit (MMU Key-Lock Error)		42		38		36	ns
TC (PROT FLAG)	Cache Miss (BPU Protection Error)		67		63		61	ns
TC (PROT FLAG)	Cache Hit (MMU Key-Lock Error)		52		48		46	ns
TC (EXT ADR)	Clock to EXT ADR Valid (Miss)		38		34		32	ns

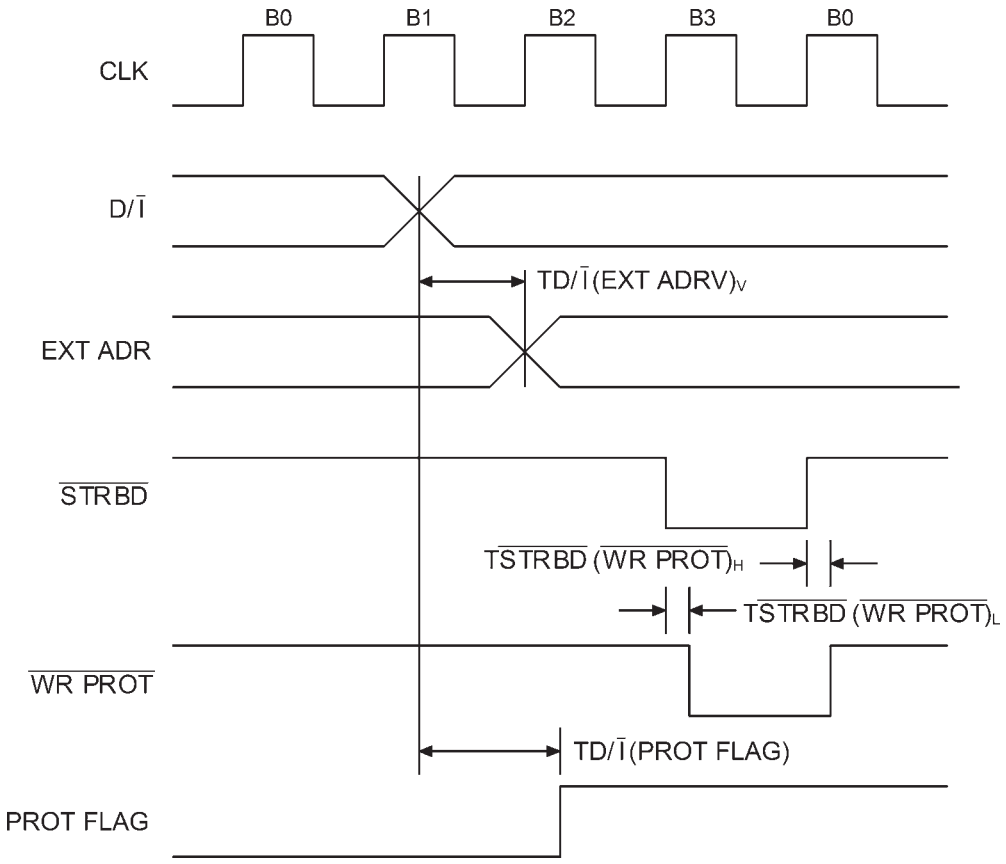
Notes:

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.
4. Pulse width of $\overline{WR\ PROT}$/PROT FLAG shall be ≥ 80% of $\overline{STRBD}$ pulse width.
5. Functional tests shall consist of the same functional tests used when testing the equivalent bulk CMOS, MIL-STD-883 compliant, Class B SMD 5962-89505 device.

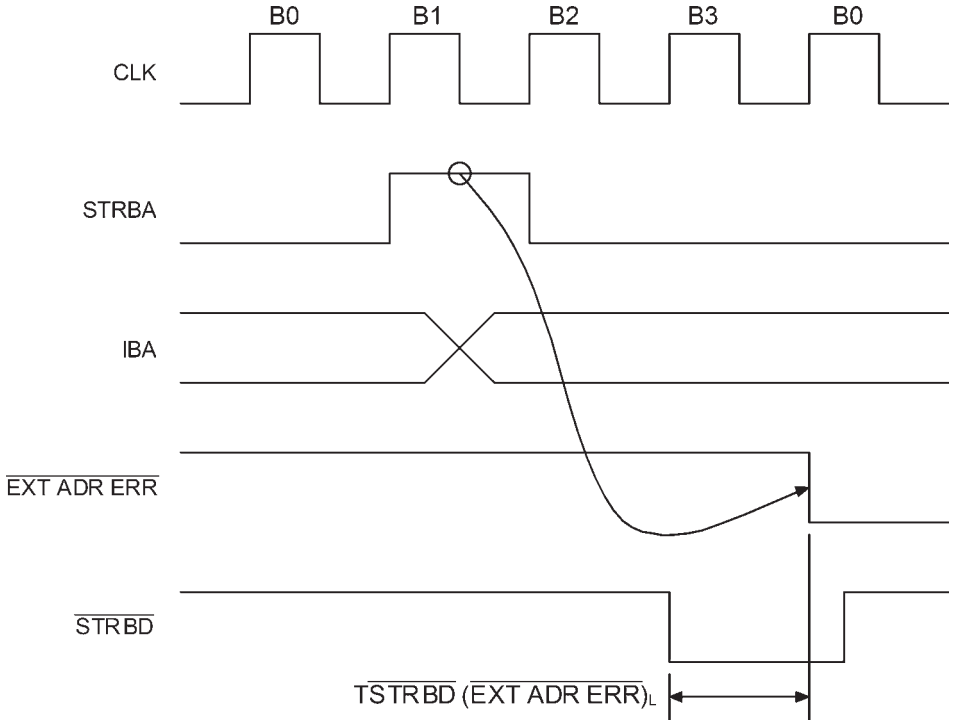
TERMINAL CONNECTIONS - PACKAGES QL AND QG

Case Outlines		U and Y			
Terminal Number	**Terminal Symbol**	**Terminal Number**	**Terminal Symbol**	**Terminal Number**	**Terminal Symbol**
1	GND	24	IB_{12}	47	AS_1
2	EDC_0	25	IB_{13}	48	AS_0
3	EDC_1	26	IB_{14}	49	$\overline{BUS\ REQ}_2$
4	EDC_2	27	IB_{15}	50	AK_3
5	$\overline{RESET}$	28	$\overline{MEM\ PRT\ ERR}$	51	AK_2
6	EDC_3	29	$\overline{MEM\ PAR\ ERR}$	52	$\overline{BUS\ GNT}_1$
7	EDC_4	30	$\overline{EXT\ ADR\ ERR}$	53	AK_1
8	EDC_5	31	RAM DIS	54	AK_0
9	$\overline{BUS\ GNT}_2$	32	SING ERR	55	CLK
10	IB_0	33	DMA ACK	56	STRBA
11	IB_1	34	GND	57	$\overline{STRBD}$
12	IB_2	35	V_{CC}	58	$\overline{BUS\ REQ}_0$
13	IB_3	36	$EXT\ ADR_0$	59	EX RDY
14	IB_4	37	$EXT\ ADR_1$	60	$\overline{WR\ PROT}$/PROT FLAG
15	IB_5	38	$EXT\ ADR_2$	61	R/$\overline{W}$
16	IB_6	39	$EXT\ ADR_3$	62	D/$\overline{I}$
17	IB_7	40	$EXT\ ADR_4$	63	M/$\overline{IO}$
18	$\overline{BUS\ REQ}_3$	41	$EXT\ ADR_5$	64	RDYA
19	IB_8	42	$EXT\ ADR_6$	65	$\overline{BUS\ GNT}_0$
20	IB_9	43	$EXT\ ADR_7$	66	$\overline{BUS\ LOCK}$
21	$\overline{BUS\ GNT}_3$	44	GND	67	$\overline{BUS\ REQ}_1$
22	IB_{10}	45	AS_3	68	V_{CC}
23	IB_{11}	46	AS_2		

MMU Cache Hit

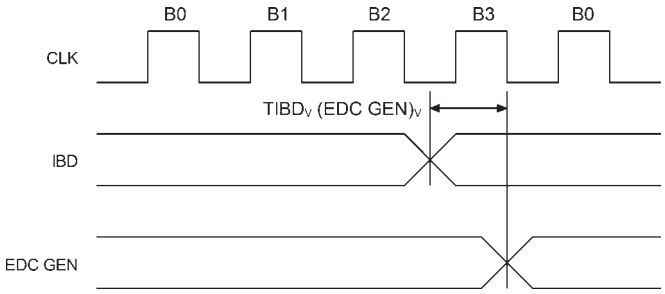


External Address Error

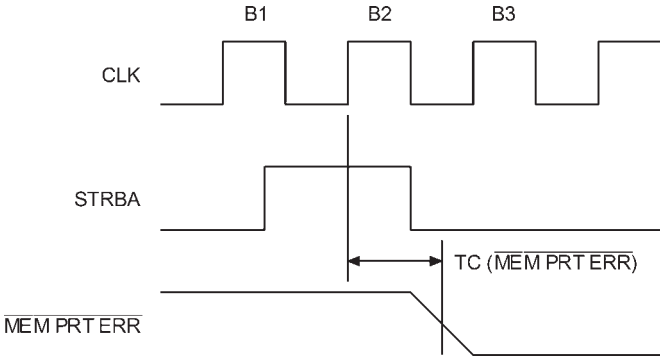


Note:
All time measurements on active signals relate to 1.5V levels.

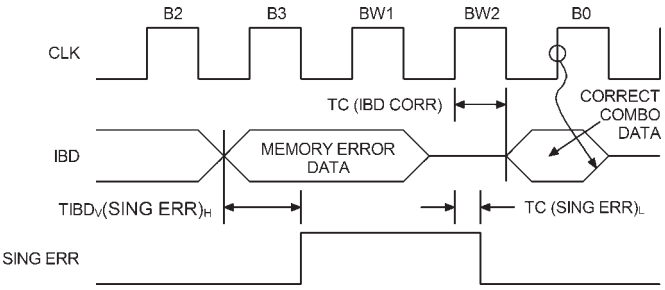
Error Correction (Write Cycle)



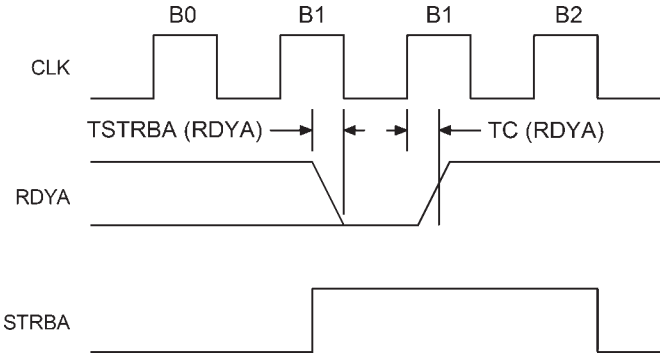
Memory Protect Error



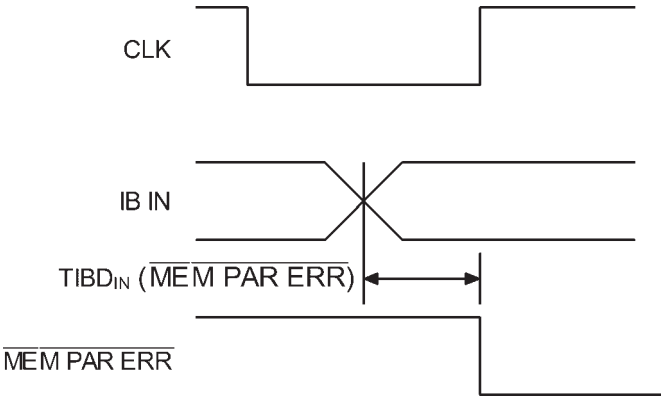
Error Correction (Read Cycle)



Ready Address

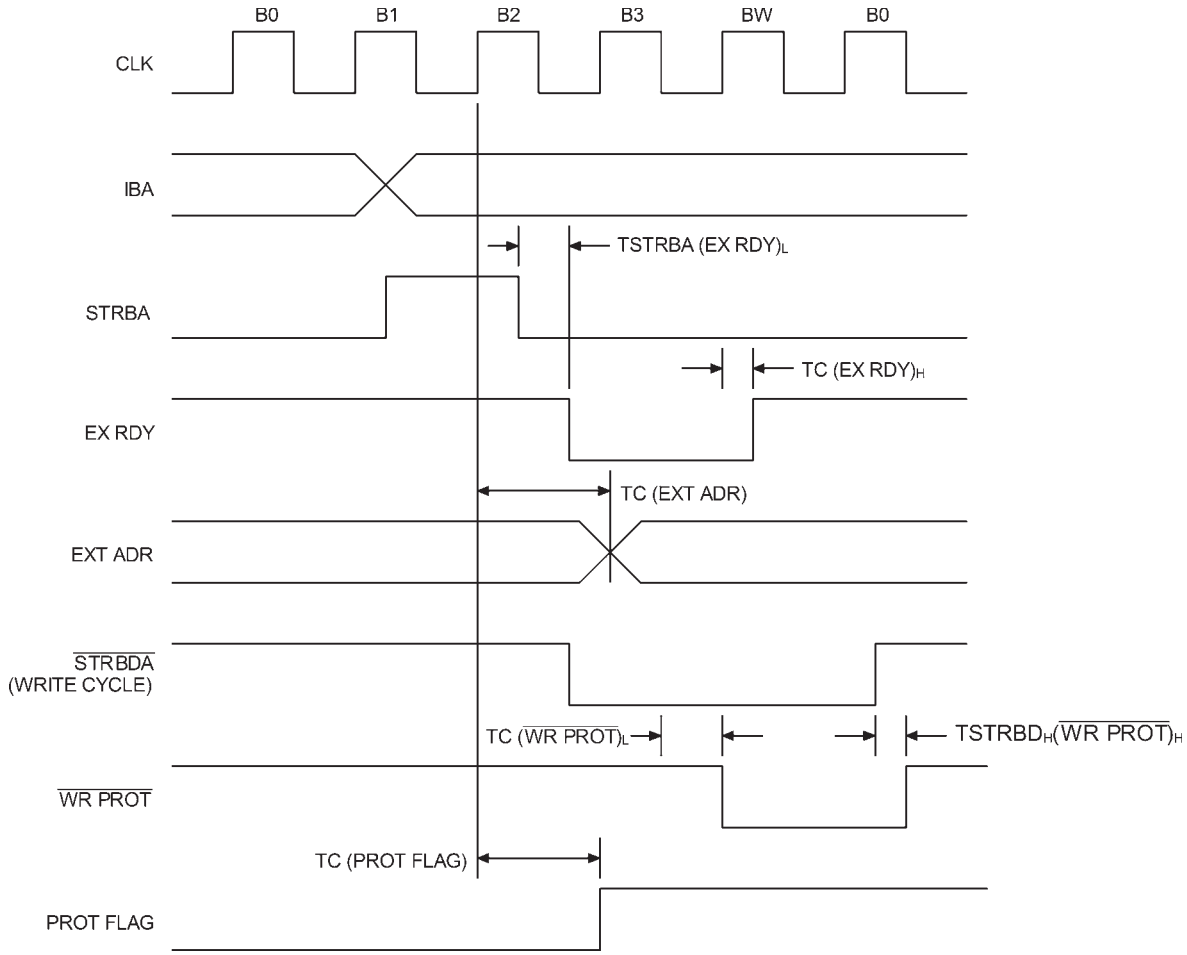


Memory Parity Error

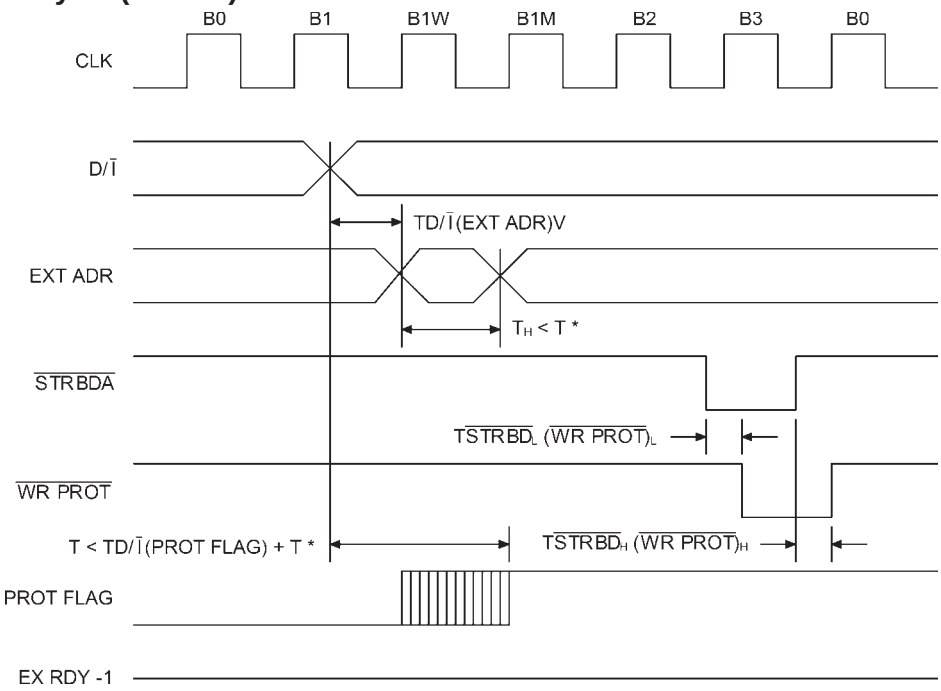


Note:
All time measurements on active signals relate to 1.5V levels.

MMU Cache Miss Cycle (WA = 0)



MMU Cache Miss Cycle (WA > 0)

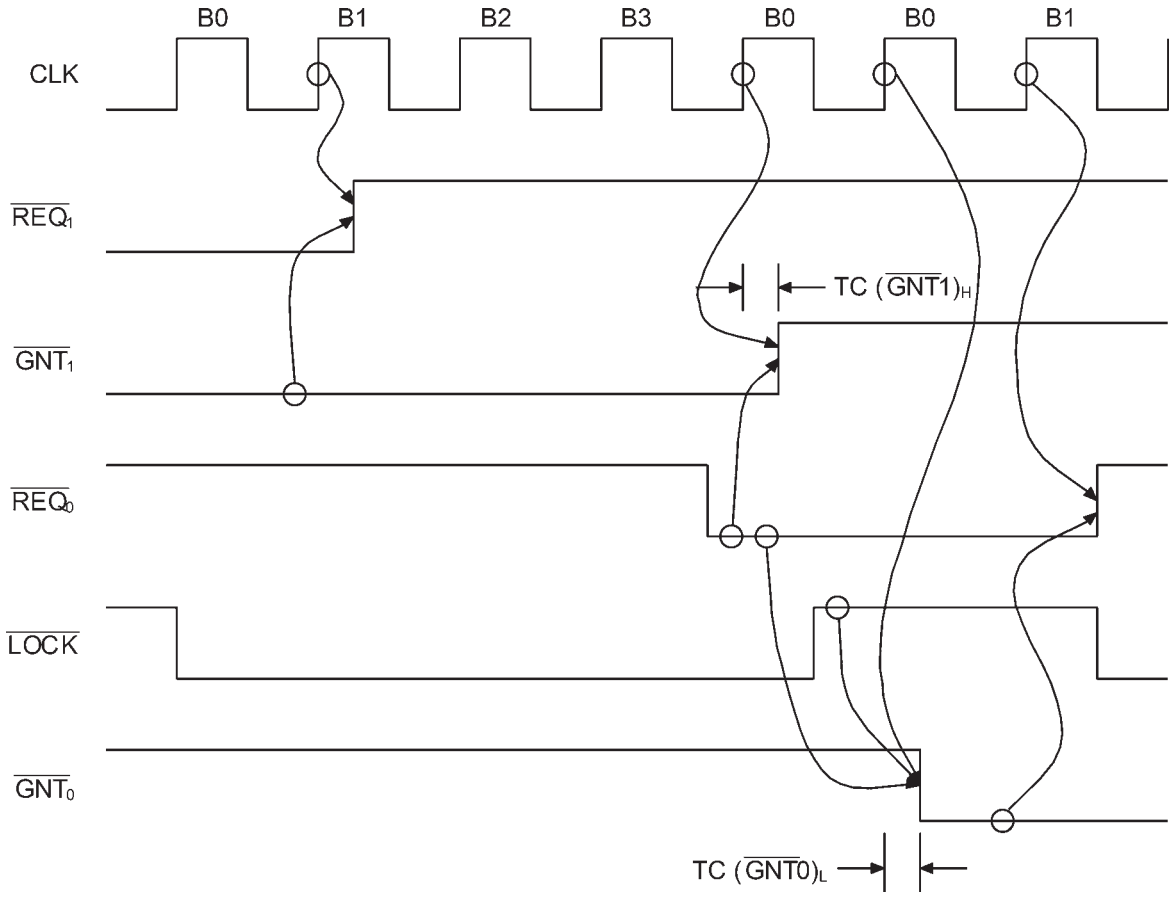


* The WR PROT/PROT FLAG signal is programmed as WR PROT or PROT FLAG. (See BPU Description), T = 1 Clock Period.

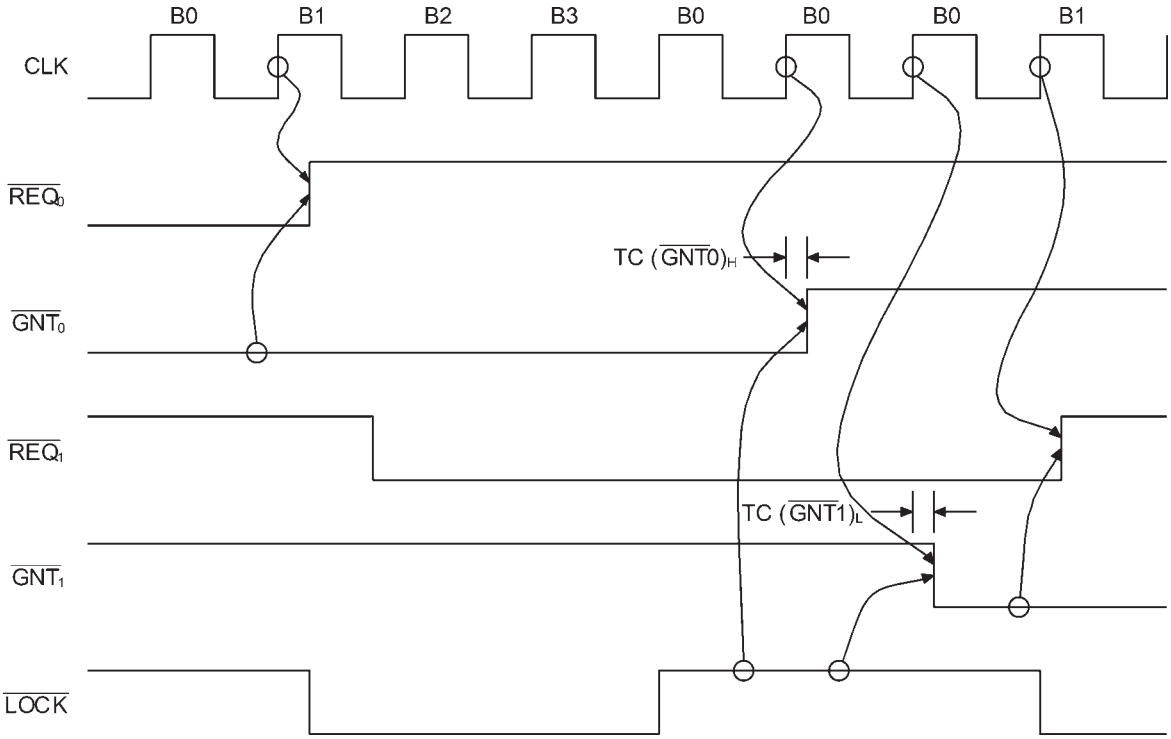
Note:

All time measurements on active signals relate to 1.5V levels.

Low Priority to High Priority Transition



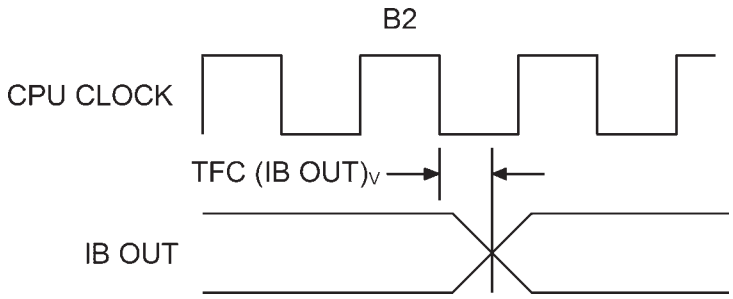
Bus Arbitrator High Priority to Low Priority Transition



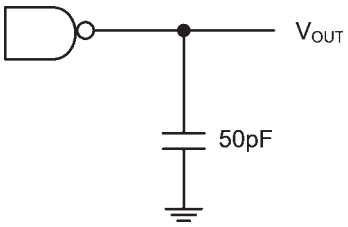
Note:
All time measurements on active signals relate to 1.5V levels.

SWITCHING WAVEFORMS AND TEST CIRCUIT (Continued)

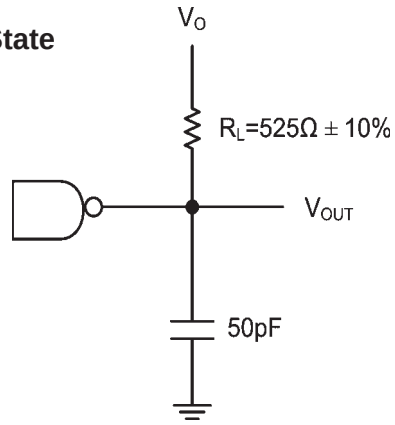
IB Bus Output (0:15)



Standard Output (Non Three-State)



Three-State



Note:
All time measurements on active signals relate to 1.5V levels.

Parameter	V_O	V_{MEA}
TPLZ	≥ 3V	0.5V
TPHZ	0V	V_{CC} – 0.5V
TPXL	$V_{CC}/2$	1.5V
TPXH	$V_{CC}/2$	1.5V

PIN FUNCTIONS

Symbol	Name	Description
$\overline{BUS\ REQ_0}$ - $\overline{BUS\ REQ_3}$	Bus Request[1]	Active LOW inputs that indicate a requirement for the bus from 4 masters on the bus. The master assigned to pin $\overline{BUS}$-$\overline{REQ_0}$ has highest priority; the master assigned to pin $\overline{BUS}$-$\overline{REQ_3}$ has lowest priority.
$\overline{BUS\ LOCK}$	Bus Lock[1]	An active LOW input that indicates that the one master assigned the bus is using the bus. A new master will receive a bus grant only after this signal becomes inactive.
$\overline{BUS\ GNT_0}$ - $\overline{BUS\ GNT_3}$	Bus Grant[1]	Active LOW outputs indicating which master was granted the bus. It remains active during $\overline{BUS\ LOCK}$ unless a higher master request occurs, which resets it. However, the higher master will be granted the bus only after the present master's $\overline{BUS\ LOCK}$ releases the bus.
M/$\overline{IO}$	Memory or I/O	An input signal that indicates whether the current bus cycle is a memory (HIGH) or I/O (LOW) cycle.
D/$\overline{I}$	Data or Instruction	An input signal that indicates whether the current bus cycle access is for data (HIGH) or instruction (LOW).
R/$\overline{W}$	Read or Write	An input signal that indicates the direction of data flow on the bus. A HIGH indicates a memory read or input operation into the master and a LOW indicates a memory write or output operation from the master.
STRBA	Address Strobe	An active HIGH input used to latch the address at the HIGH-to-LOW transition of the strobe.
$\overline{STRBD}$	Data Strobe	An active LOW input used to strobe data in memory and I/O cycles.
CPU-CLK	CPU Clock	A single-phase input clock signal (0-40MHz, 40% to 60% duty cycle.)
$\overline{RESET}$	Reset	An active LOW input that initializes the device.
AK_0 - AK_3	Access Key	Active HIGH inputs used to match the access lock in the MMU page for memory accesses. A mismatch will cause the $\overline{MEM\ PRT\ ERR}$ signal to become active.
AS_0 - AS_3	Address State	Active HIGH inputs that select the page register group in the MMU. In the DMA physical demultiplexed mode, AS(0:1) will receive the 9th and 10th most significant bits of the physical address for use in the BPU function.
EXT ADR_0 - EXT ADR_7	Extended Addresses Bus	A bi-directional active HIGH bus. In CPU cycles, it is an output bus which is used to select one of 256 pages, 4K words each, expanding the direct addressing space to 1M word. In DMA cycles, indicated by DMA-ACK being active, it is also an output bus except when programmed for the physical demultiplexed DMA mode. In this case it becomes an input to receive the 8 most significant bits of the DMA physical address for use in the BPU function.
IB_0 - IB_{15}	Information Bus	An active HIGH bi-directional time multiplexed address/data bus. IB_0 is the most significant bit.
EDC_0 - EDC_5	Detection/Correction Bus	An active HIGH bi-directional bus used for detection of errors on the data bus (IB_0 - IB_{15}) and correction of single errors. When working in parity mode EDC_0 is the parity bit. EDC_0 - EDC_5 are undefined in this case.

PIN FUNCTIONS (Continued)

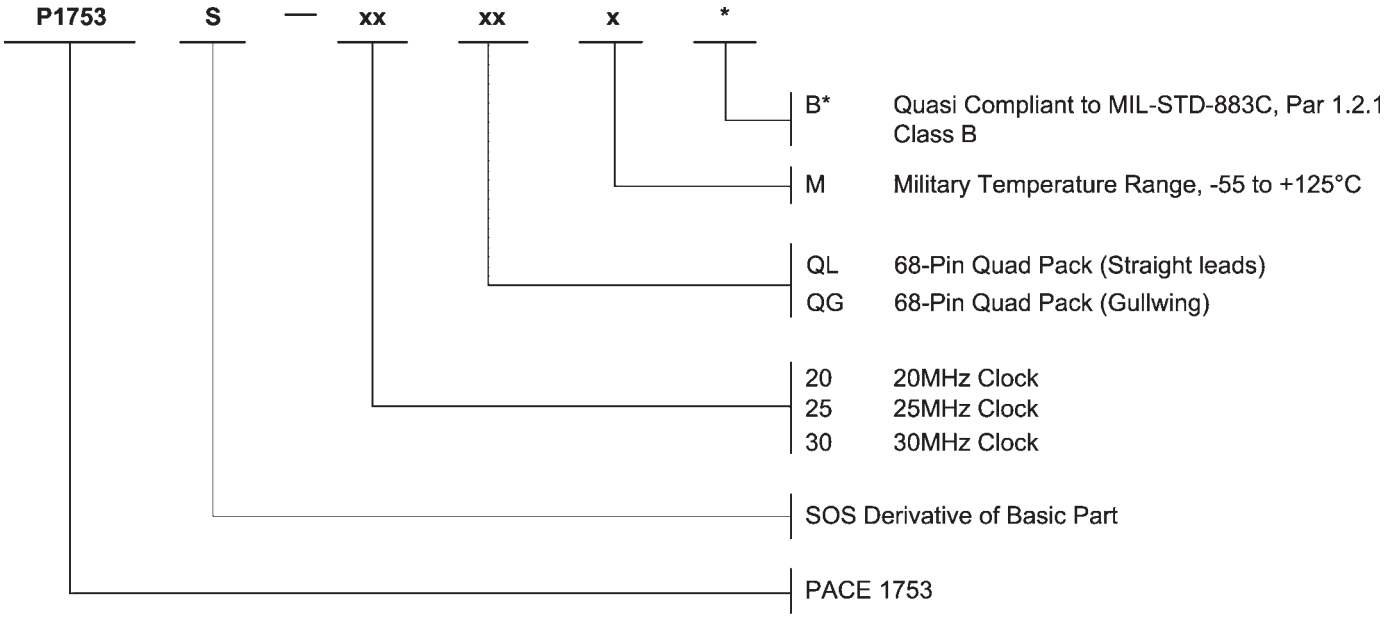
Symbol	Name	Description
$\overline{\text{MEM PRT ERR}}$	Memory Protect Error	An active LOW output generated by the MMU or BPU blocks to signal to the CPU a protected memory violation. The error is generated in one of the following conditions: a mismatch in the access keys in the MMU page, an access to an execution protected page during instruction cycles, an access to a write-protected page during data cycles, or an access to a page write-protected by the BPU.
$\overline{\text{MEM PAR ERR}}$	Memory Parity Error	An active LOW output which signals to the CPU an error on the data bus during a memory cycle. Two detection modes can be selected by programming the control register: EDAC mode (6 Hamming code parity bits) or single bit parity mode (even or odd parity). The signal is inactive when none of the above modes are selected (default after Reset).
$\overline{\text{EXT ADR ERR}}$	External Address Error	An active LOW output which signals to the CPU an unimplemented memory or illegal I/O access.
SING ERR	Single Error	An active HIGH output to signal detection of a single error on the data bus in memory cycles. It is high impedance when the EDAC function is disabled by the program (default state after Reset).
RAM DIS	RAM-Disable	An active HIGH input from the P1754 device which enables the corrected data on the data bus when the EDAC function is enabled. An internal one clock delay is generated before the data is output on the bus to allow external memory to disconnect itself from the bus.
EX RDY	Data Ready	An active HIGH output that indicates that no wait states are requested. It becomes inactive for one clock (inserting one wait state) whenever a memory page different than the current one is accessed (causing a miss).
RDYA	Address Ready	An active HIGH output that indicates that no wait states are requested when STRBA is active. Wait states are inserted when this signal becomes inactive during STRBA. Up to three wait states can be inserted by programming an internal register. Three wait states are inserted after Reset (default).
$\overline{\text{WR PROT}}$/ PROT FLAG	Write Protected/ Protection Flag	Either an active LOW output (following $\overline{\text{STRBD}}$ timing) during legal memory write cycles, when no protection error occurs, or an active HIGH level indicating a protection error in a write cycle. Each mode can be selected by programming the control register. Default mode after Reset is write-protected.
DMA ACK	DMA Acknowledge	An active HIGH input from the DMA controller which indicates a DMA cycle. Used to select the DMA table in the BPU memory for protection. For example, this could allow the DMA channel to update the program which could be write-protected from the processor. In the physical DMA mode, it will cause the Extended Address Lines (EXT ADR_{0-7}) to become inputs, providing BPU protection of the DMA transfers.

Note:

1. Used for Bus Arbitration; only available on 68-lead devices.

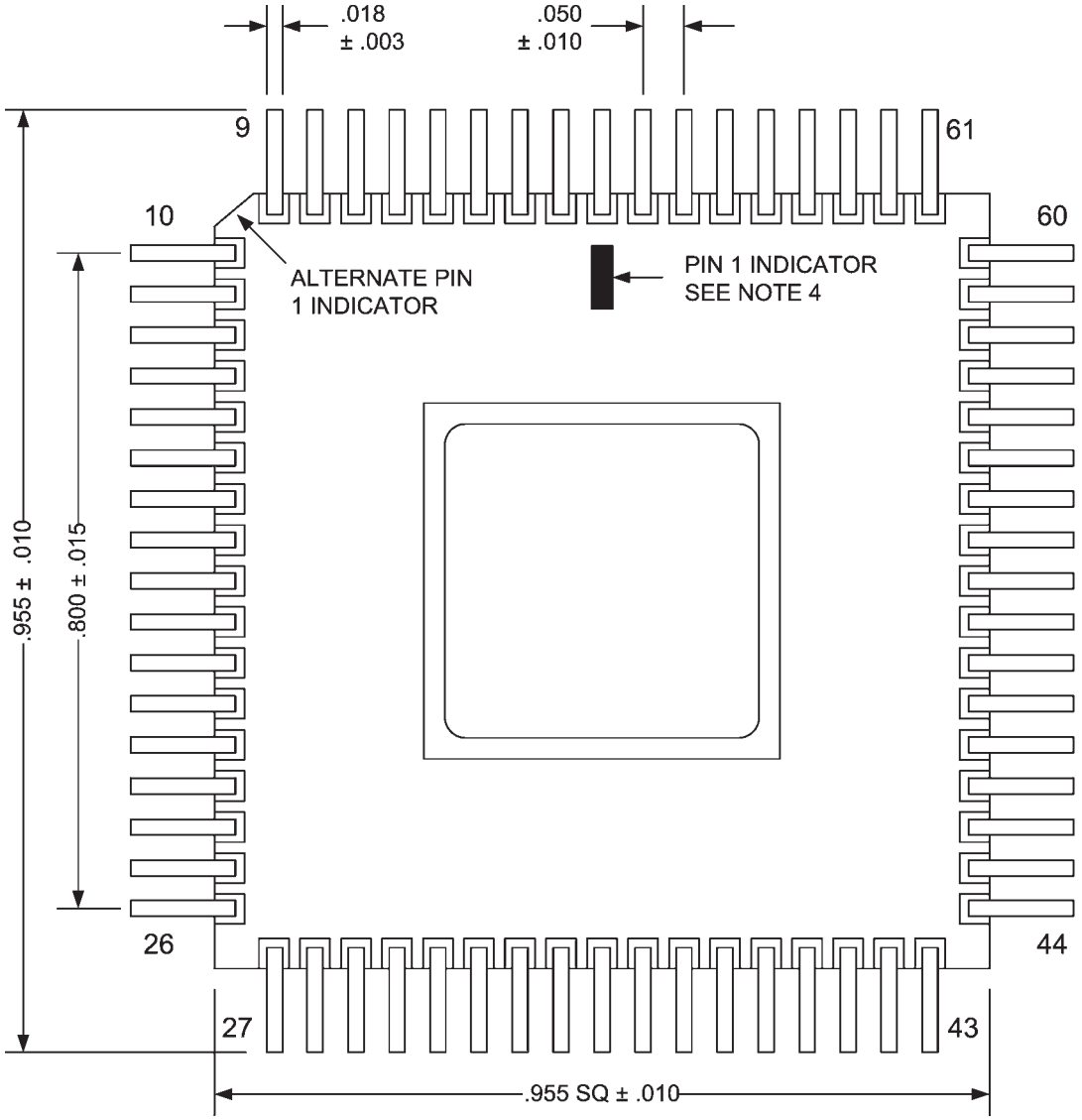
Standardized Military Drawing Part Number	Pyramid Semiconductor CAGE Number	Pyramid Semiconductor Part Number
5962-8950501UX	3DTT2	P1753-20QLMB
5962-8950501YX	3DTT2	P1753-20QGMB
5962-8950501ZX	3DTT2	P1753-20PGMB
5962-8950502UX	3DTT2	P1753-30QLMB
5962-8950502YX	3DTT2	P1753-30QGMB
5962-8950502ZX	3DTT2	P1753-30PGMB
5962-8950503UX	3DTT2	P1753-40QLMB
5962-8950503YX	3DTT2	P1753-40QGMB
5962-8950503ZX	3DTT2	P1753-40PGMB
5962-8950504TX	3DTT2	P1753-20GMB
5962-8950504XX	3DTT2	P1753-20CMB
5962-8950505TX	3DTT2	P1753-30GMB
5962-8950505XX	3DTT2	P1753-30CMB
5962-8950506TX	3DTT2	P1753-40GMB
5962-8950506XX	3DTT2	P1753-40CMB

ORDERING INFORMATION

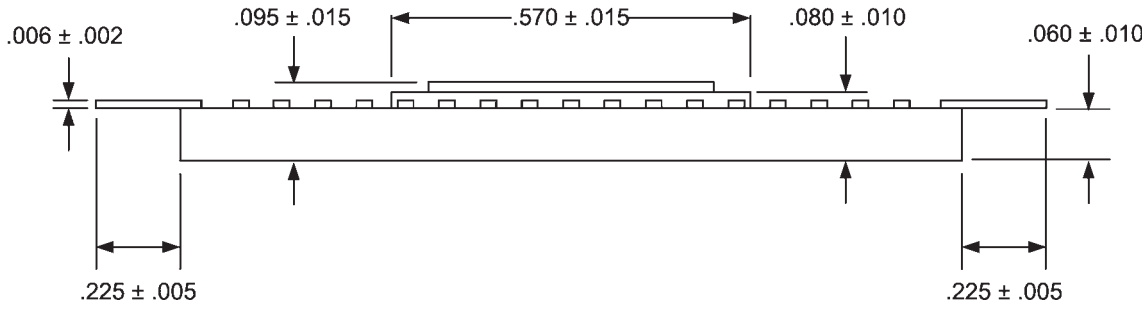


CASE OUTLINE 1:

68 Lead Quad Pack with Straight Leads (Ordering Code QL)



Inches	mm
.002	0.05
.003	0.08
.006	0.15
.010	0.25
.015	0.38
.018	0.45
.050	1.27
.060	1.52
.080	2.03
.095	2.41
.225	5.72
.570	14.48
.800	20.32
.955	24.25

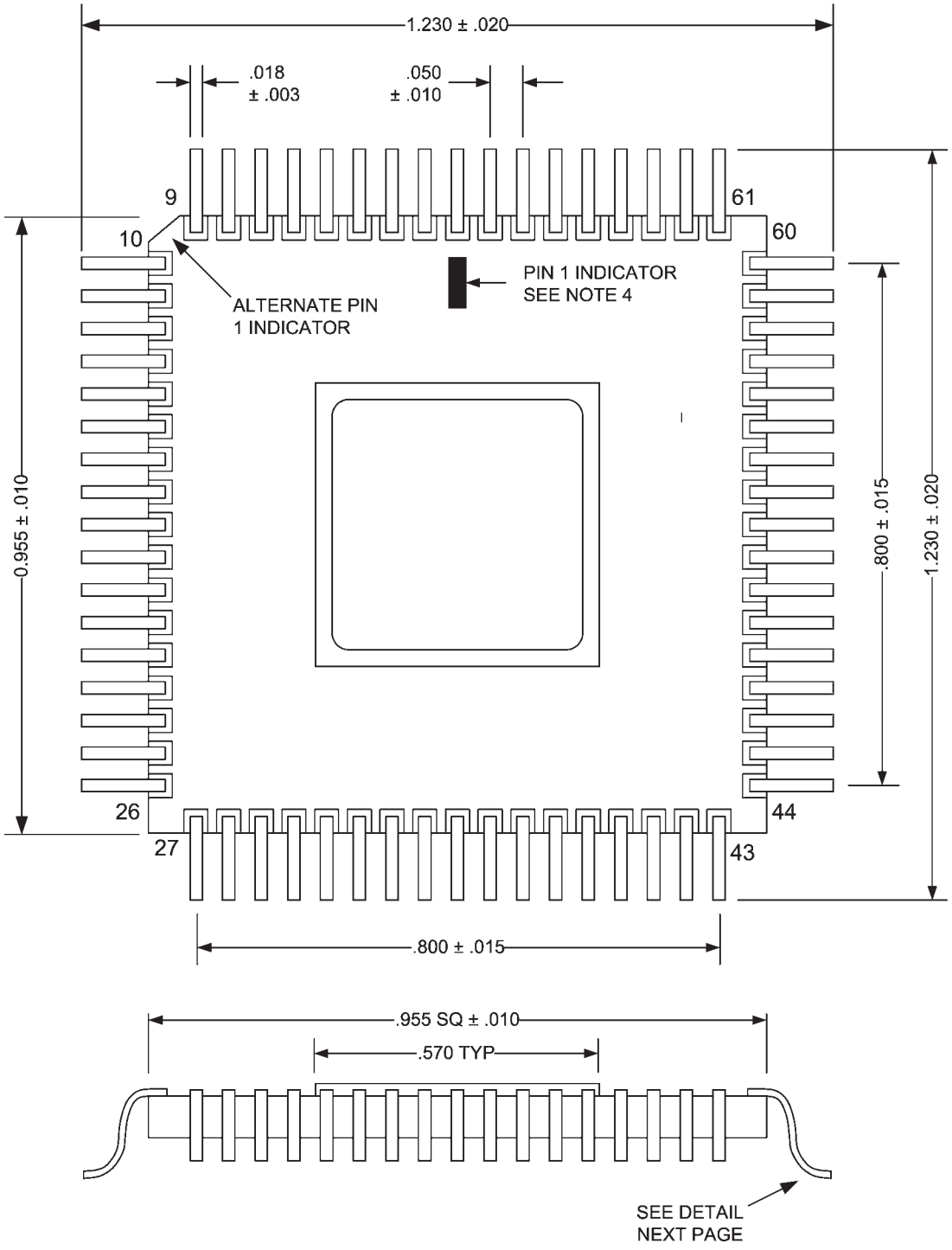


NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Pin 1 indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5) Corners indicated as notched may be either notched or square.

CASE OUTLINE 2:

68 Lead Quad Pack with Gullwing Leads (Ordering Code QG)



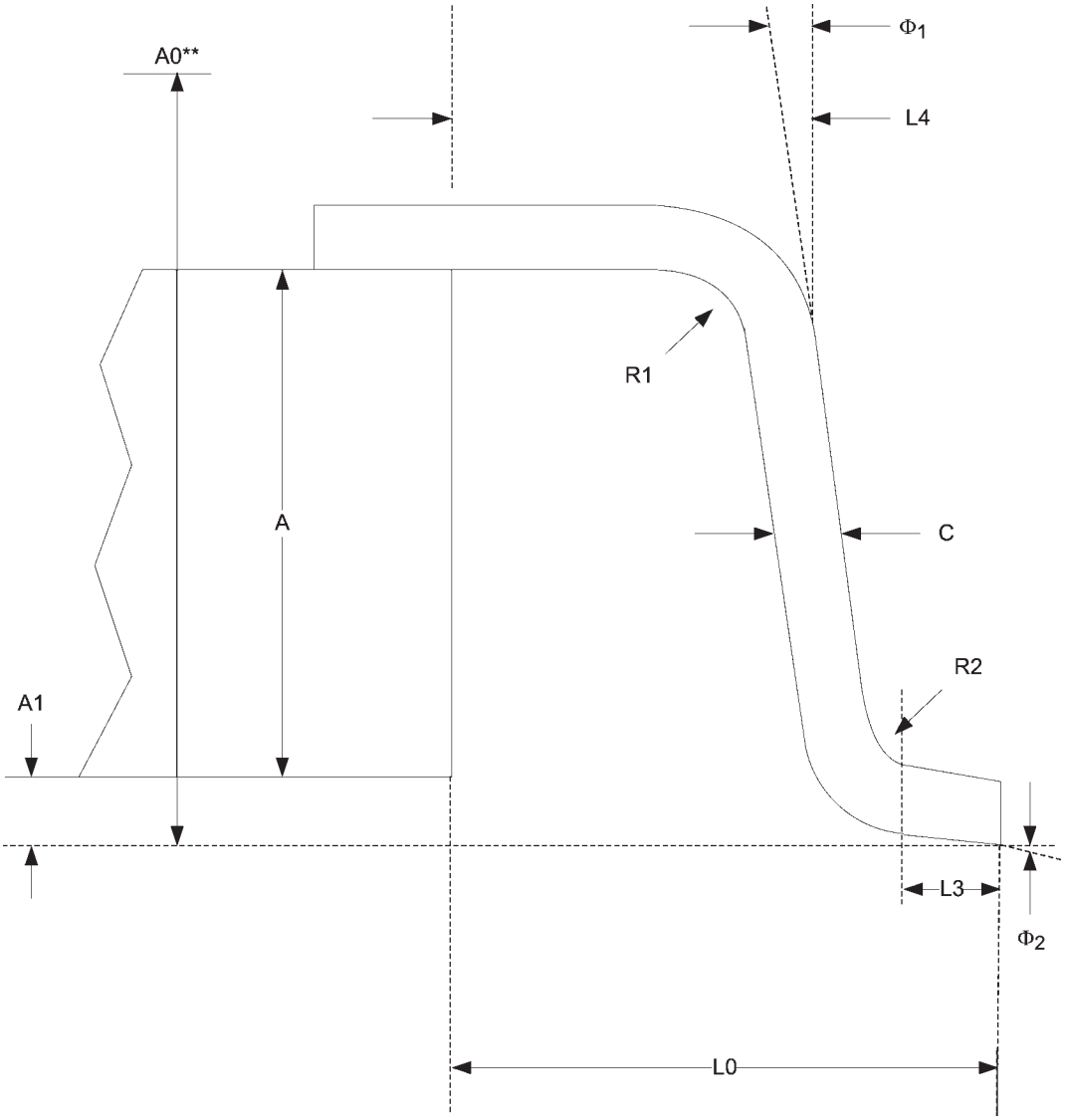
Inches	mm
.003	0.08
.010	0.25
.015	0.38
.018	0.45
.020	0.51
.050	1.27
.570	14.48
.800	20.32
.955	24.25
1.230	31.26

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Pin 1 indicator can either be rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5) Corners indicated as notched my be either notched or square (with radius).
6) Case 2 is derived from Case 1 by forming the leads to the shown gullwing configuration.

LEAD FORM DETAIL

Symbol	INCHES	
	Min	Max
A	0.048	0.090
A1	0.011	0.031
B	0.016	0.021
C	0.004	0.008
e1	0.050 BSC	
D	1.210	1.250
D1	0.945	0.965
D2	0.800 BSC	
E	1.210	1.250
E1	0.945	0.965
E2	0.800 BSC	
L*	0.270 Nominal	
L0	0.120	0.210
L3	0.040	0.050
L4	0.086	0.109
R1	0.018	0.020
R2	0.018	0.020
Φ_1	4°	8°
Φ_2	-1°	7°
A0**		0.141



* Lead length in the straight lead configuration, prior to leadforming (used for all test and in-process WIP operations).

** Measured from the highest of the top of the leads or the top of the lid.

REVISIONS

DOCUMENT NUMBER: MICRO-8
DOCUMENT TITLE: PACE1753/SOS CMOS MMU/COMBO

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
ORIG	May-89	RKK	New Data Sheet
A	Jul-04	JDB	Added Pyramid logo
B	Aug-05	JDB	Re-created electronic version