To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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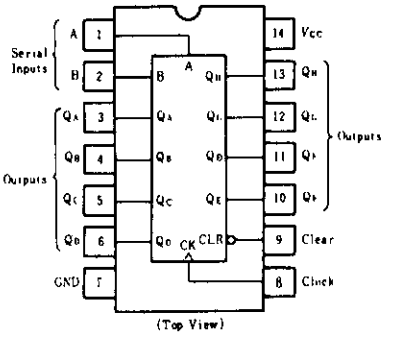
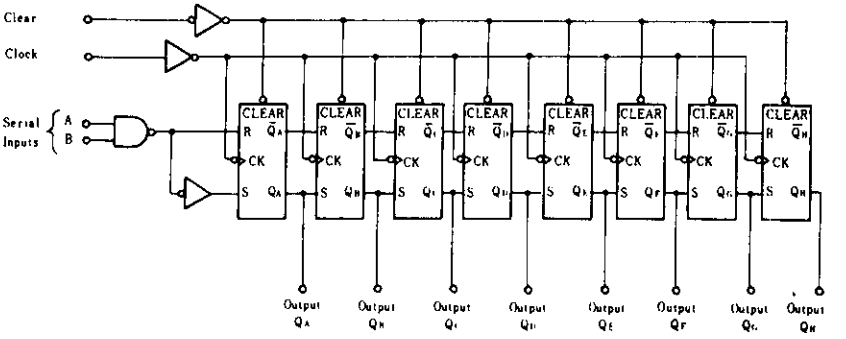
HD74LS164 ●8-Bit Parallel-Out Serial-In Shift Registers

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will them determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■FUNCTION TABLE

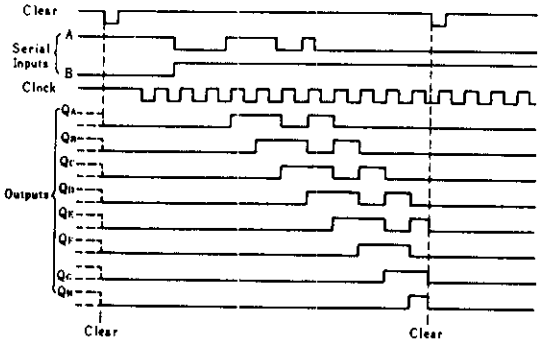
Inputs				Outputs		
Clear	Clock	A	B	Q_A	Q_B ·····	Q_H
L	×	×	×	L	L	L
H	L	×	×	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	×	L	Q_{An}	Q_{Gn}
H	↑	×	L	L	Q_{An}	Q_{Gn}

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. Q_{A0}, Q_{B0}, Q_{H0}; the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
4. Q_{An}, Q_{Gn}; the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_{w(CK)}$	20	—	—	ns
Clear pulse width	$t_{w(CLR)}$	20	—	—	ns
Data setup time	t_{su}	15	—	—	ns
Data hold time	t_h	5	—	—	ns

■TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0		–	V
	V_{IL}		–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$	2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=4mA$	–	–	0.4	V
		$I_{OL}=8mA$	–	–	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$	–		20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$	–		–0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$			0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$	–20	–	100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$	–	16	27	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$	–	–	–1.5	V

* V_{CC}=5V, Ta=25°C

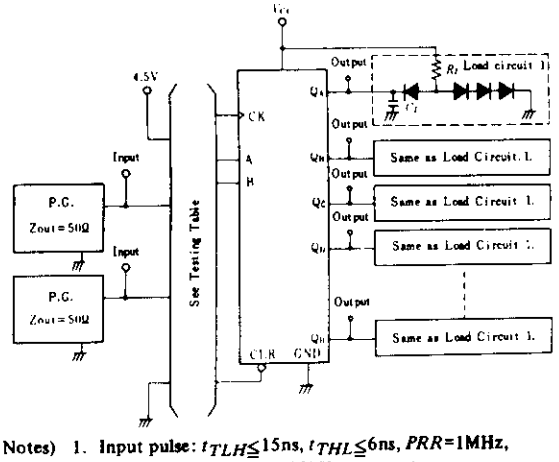
** I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary grounded, then 4.5V applied to clear.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	25	36		MHz
Propagation delay time	t_{PHL}	Clear	Q		–	24	36	ns
	t_{PLH}	Clock	Q		–	17	27	ns
	t_{PHL}	Clock	Q		–	21	32	ns

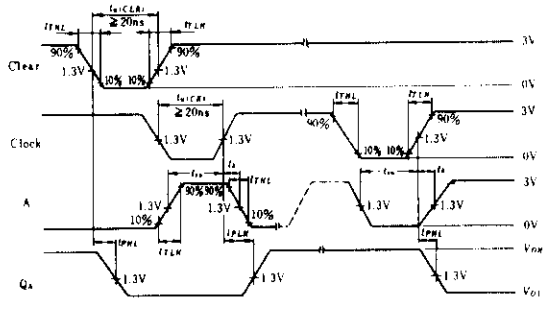
■TESTING METHOD

1) Test Circuit



Notes) 1. Input pulse: $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, PRR=1MHz, (Clock, Clear), PRR=500kHz (A or B)
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074 Ⓗ

Waveform

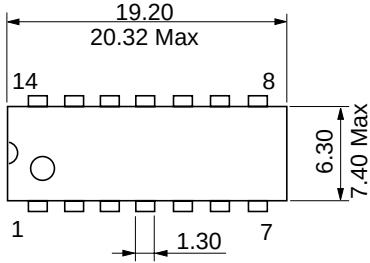


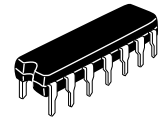
Notes) Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the timing chart.

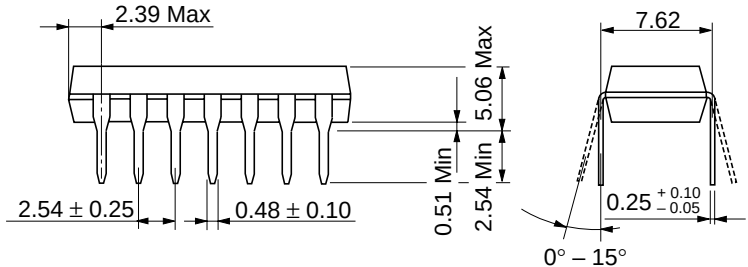
2) Testing Table

Item	From input to output	Inputs				Outputs							
		CLR	CK	A	B	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H
f_{max}		4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PLH}	Clear→Q	IN	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PHL}	CK → Q	4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

Unit: mm

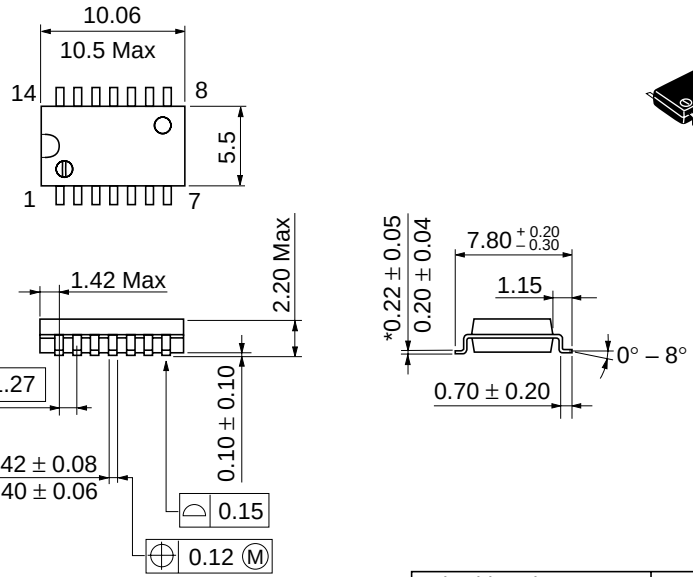


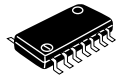




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

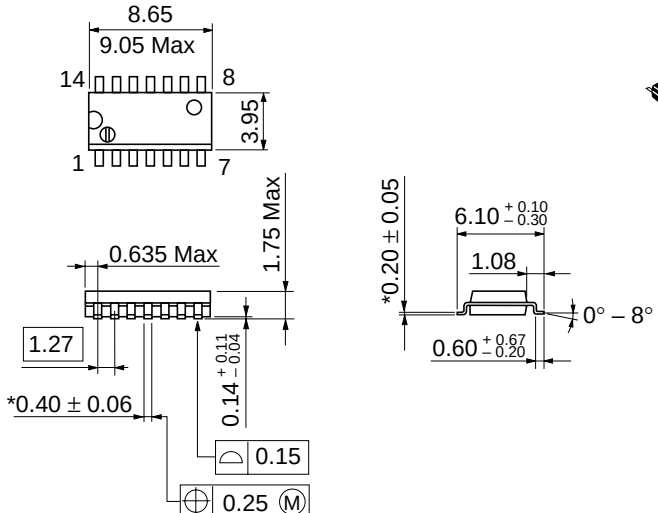




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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